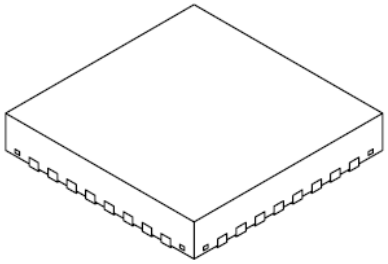
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC7739FTG

System power IC

1. Overview

TC7739FTG is a system power IC which incorporates 2 channels of step-down DCDC converter, 4 channels of LDO, and 1 channel of load switch. Each output voltage can be set various output settings through the I^2C bus.



P-VQFN32-0505-0.50-001

Weight: 0.07g (typ.)

2. Features

- AVCC input voltage range: 4.5V to 5.5V
- DCDC converter (CH1 and CH2)

	Power voltage range	Output voltage (*1)	Output current
CH1	3.6V to 5.5V	1.05V	2A
CH2	4.3V to 5.5V	3.3V	2A
	4.0V to 5.5V	3.3V	300mA

  - Synchronous Current Mode Buck Converters
  - Output current 2A and more
  - Operation frequency: 2 MHz(CH1),1.5 MHz(CH2)
  - Output voltage accuracy: ±1%@Ta=25°C
±2%@Ta=-40°C to 85°C
  - Output voltage ripple: 20mVp-p or less (recommended components use)
  - Built in Discharge circuit
  - Built in Soft Start function
  - Load regulation 0.5%
  - Line regulation 0.5%
  - Built in Over Voltage Protection (OVP)
  - Built in Under Voltage Protection (UVP)
  - Built in Over Current Limitation (OCL)
  - Widely current range support by PFM/PWM auto switching

- LDO(CH3 to CH6)

	Power supply voltage range	Output voltage (*1)	Output current
CH3	1.630V to 2.057V	1.15V	0.7A
CH4	1.630V to 2.057V	1.50V	0.6A
CH5	1.95V to 5.50V	1.80V	0.2A
CH6	3.60V to 5.50V	3.30V	0.06A

  - Output voltage accuracy: ±1%@Ta=25°C
±2%@Ta=-40°C to 85°C
  - Built in Discharge circuit
  - Built in Soft Start function
  - Load regulation 0.5%
  - Line regulation 0.5%
  - Built in Over Voltage Protection (OVP)
  - Built in Under Voltage Protection (UVP)
  - Built in Over Current Limitation (OCL)

- Load switch (CH7)
  - Rds(on): 62mΩ(Typ.)
  - Built in Discharge circuit
  - Built in Soft Start function
  - Built in Under Voltage Protection (UVP)
  - Built in Over Current Limitation (OCL)

- Reset voltage output function
  - Detection voltage: 3.6V±90mV
  - Recovery voltage: 3.7V±93mV
  - Output delay time after detecting voltage: 10μs(Typ.)
  - Output delay time after recovering voltage: 60μs(Typ.)
- Output parameters can be changed by I^2C control.
- Other system protection: Thermal Shutdown (TSD), Under Voltage Lock Out (UVLO)
- Package: P-VQFN32-0505-0.50-001
- Application: Tablet PC, portable devices

* 1: Modifiable through I^2C.

3. Block diagram and application circuit

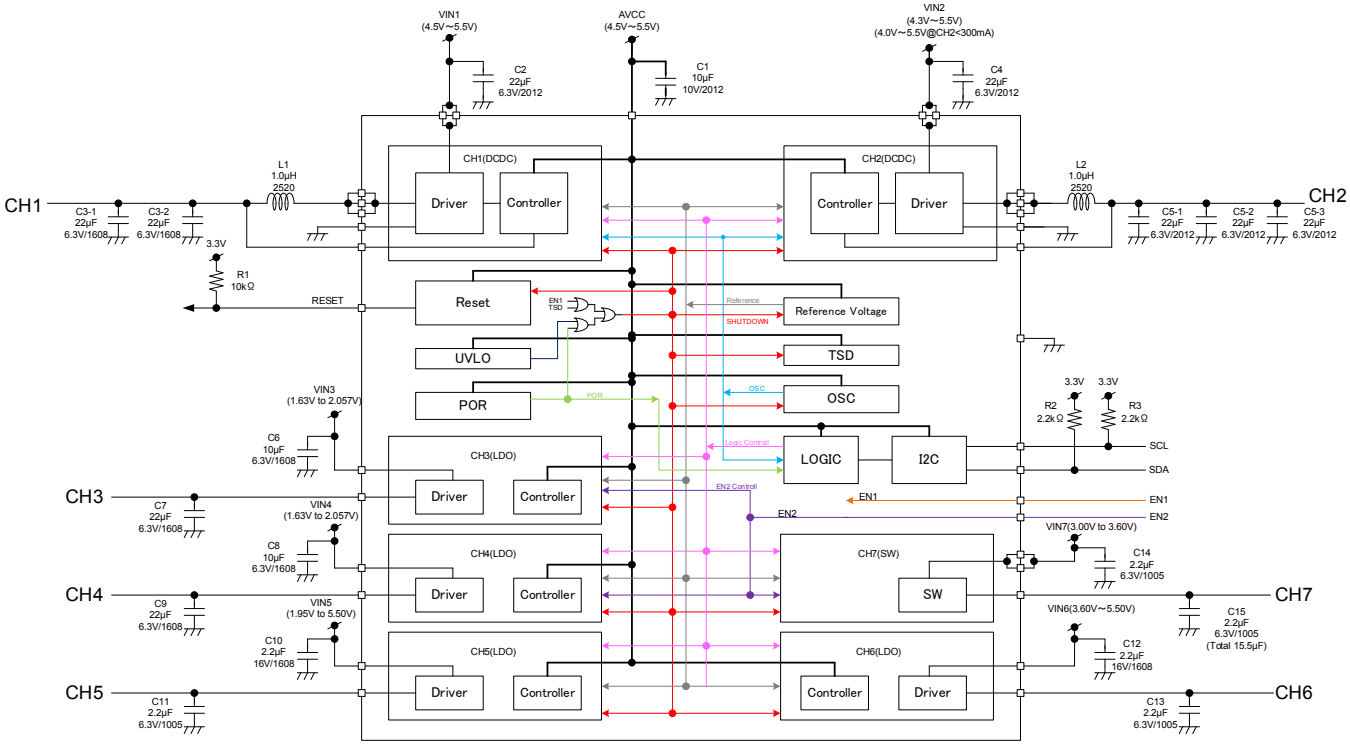


Figure 3.1 Block diagram and application circuit

Note

- Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes. The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits
- GND wiring: GND and heatsink part wires of the device must run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.
- Careful attention should be paid to the layout of the output, VDD (VM) and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.
- In this IC, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (each power supply, LX, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.
- The logic input pins (EN1 and EN2) must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

4. Pin layout (Top View)

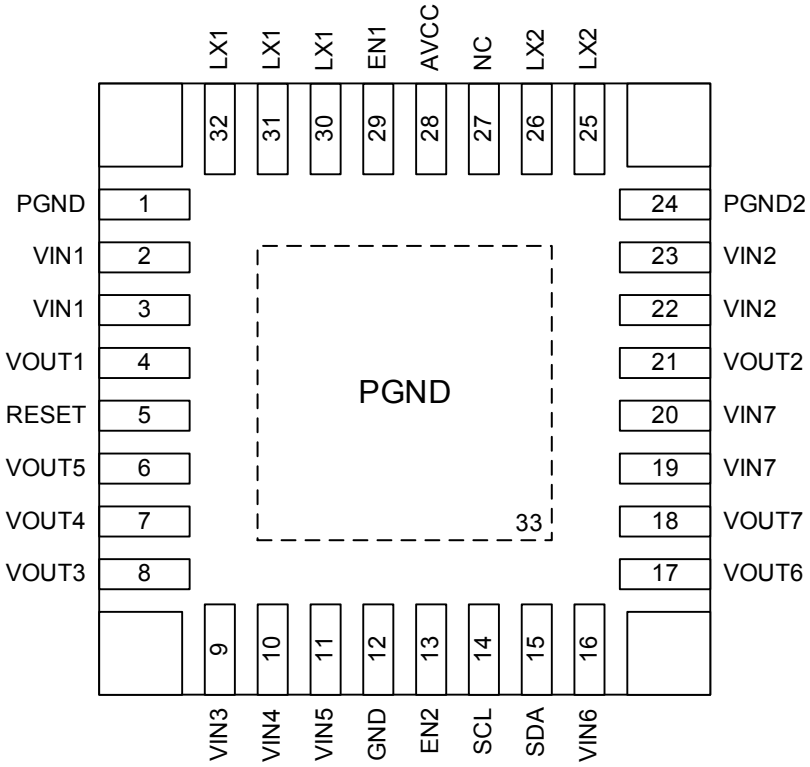


Figure 4.1 Pin layout

5. Pin description

Table 5.1 Pin description

Pin No.	Pin name	I/O	Function
1	PGND	P	Power GND pin
2	VIN1	P	Power supply input pin for CH1 output
3	VIN1	P	Power supply input pin for CH1 output
4	VOUT1	I	CH1 feedback pin
5	RESET	O	RESET circuit signal output pin
6	VOUT5	O	CH5 output pin
7	VOUT4	O	CH4 output pin
8	VOUT3	O	CH3 output pin
9	VIN3	P	Power supply input pin for CH3 output
10	VIN4	P	Power supply input pin for CH4 output
11	VIN5	P	Power supply input pin for CH5 output
12	GND	P	GND pin of logic system and signal system
13	EN2	I	ON/OFF control pin for CH3,CH4,and CH7
14	SCL	I	I^2C communication clock pin
15	SDA	I/O	I^2C communication data input /output pin
16	VIN6	P	Power supply input pin for CH6 output
17	VOUT6	P	Power supply input pin for CH6 output
18	VOUT7	P	Power supply input pin for CH7 output
19	VIN7	P	Power supply input pin for CH7 output
20	VIN7	P	Power supply input pin for CH7 output
21	VOUT2	I	CH2 feedback pin
22	VIN2	P	Power supply input pin for CH2 output
23	VIN2	P	Power supply input pin for CH2 output
24	PGND2	P	Power GND pin
25	LX2	I/O	DC/DC switching pin (for CH2)
26	LX2	I/O	DC/DC switching pin (for CH2)
27	NC	I/O	Unused pin (GND connection and open process are necessary because it is used for testing.)
28	AVCC	P	Power supply input pin for internal circuit
29	EN1	I	ON/OFF control pin for CH1,CH2,CH5,and CH6
30	LX1	I/O	DC/DC switching pin (for CH1)
31	LX1	I/O	DC/DC switching pin (for CH1)
32	LX1	I/O	DC/DC switching pin (for CH1)
33	PGND	P	Power GND pin

Notes: I= Input, O=Output, P=Power

6. State diagram

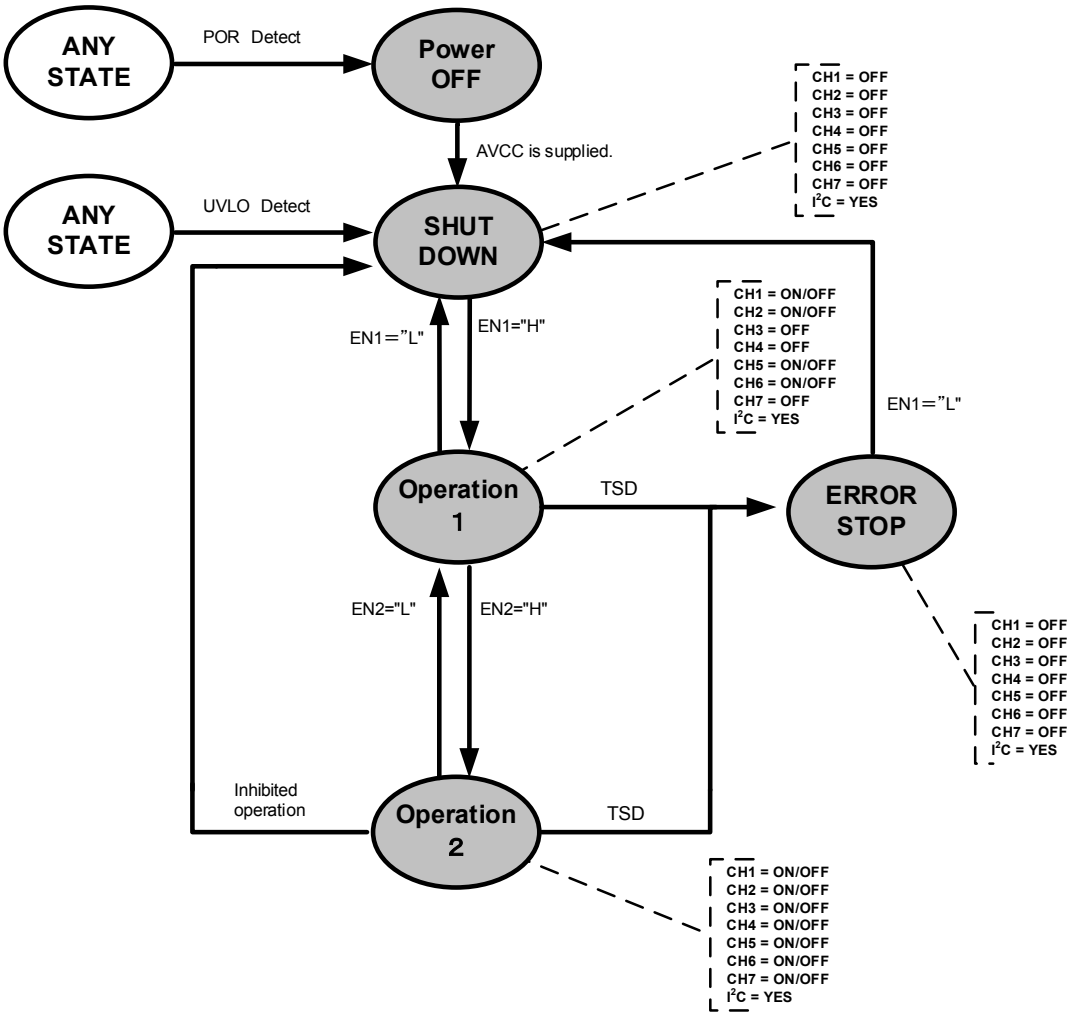


Figure 6.1 State diagram

Mode description

POWER OFF **:** It is the mode in which the main power supply (AVCC) is not supplied.
If the AVCC reaches below POR detection voltage (2.5V target), it will shift to this mode.

SHUTDOWN **:** It is the mode in which the AVCC is supplied and the POR is de-asserted.
Operating circuits are POR, RESET, UVLO, and I2C circuit. It will shift to this mode when the UVLO is detected in this operation.

Operation1 **:** It is the mode in which CH1, 2, 5, and 6 is turned on by inputting EN1=”H.”
It will shift to ERRORSTOP when detecting TSD.
When the individual channel protection function is operating, only target channel is processed.

Operation2 **:** It is the mode in which all channels (CH1 to 7) are turned on by inputting EN1=EN2=”H.”
It will shift to ERRORSTOP when detecting TSD.
When the individual channel protection function is operating, only target channel is processed.
It is inhibited operation that EN1="L" is input from this state, and is shifted to the SHUTDOWN state.

ERRORSTOP **:** In the state of the Operation1 or 2, when detecting TSD, it shifts to this mode. All channels (CH1 to 7) stop operations though I2C communication can be received.
When inputting EN1=”L,” it will shift to SHUTDOWN mode. Then EN2 and EN1 need to be input “L” simultaneously (The combination of EN=”L” and EN2=”H” is inhibited operation).

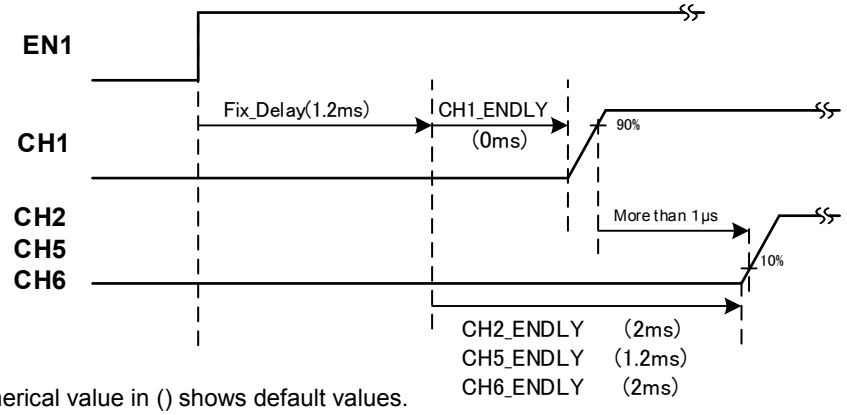
7. Power supply sequence

7.1. Sequence

EN1 signal can control CH1, CH2, CH5, and CH6 outputs.
EN2 signal can control CH3, CH4, and CH7 outputs.

7.1.1. Startup sequence by EN1 signal

Each channel starts the startup sequence after the Fix_Delay (1.2 ms) when receiving EN1="H."



Numerical value in () shows default values.

Figure 7.1 Startup sequence by EN1 signal

7.1.2. Turn off sequence by EN1 signal

(1) Normal sequence
CH1, CH2, CH5, and CH6 immediately start the turn off sequence when receiving EN1="L."

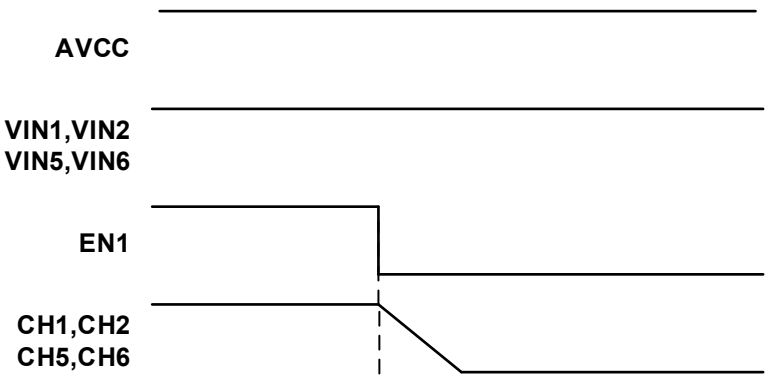


Figure 7.2 Turn off sequence by EN1 signal

(2) Turn off sequence at the AVCC voltage drop.
In the state of EN1="H," when the AVCC voltage is dropping below the UVLO detection voltage, CH1, CH2, CH5 and CH6 start the turn off operation.
In addition, since the RESET pin voltage is set "L" in the state of which the AVCC voltage is dropping below the RESET detection voltage, the normal sequence starts when EN signal is "L." However, when the AVCC voltage is dropping below the UVLO detection voltage in the same state, the turn off sequence starts without waiting for the Delay time.

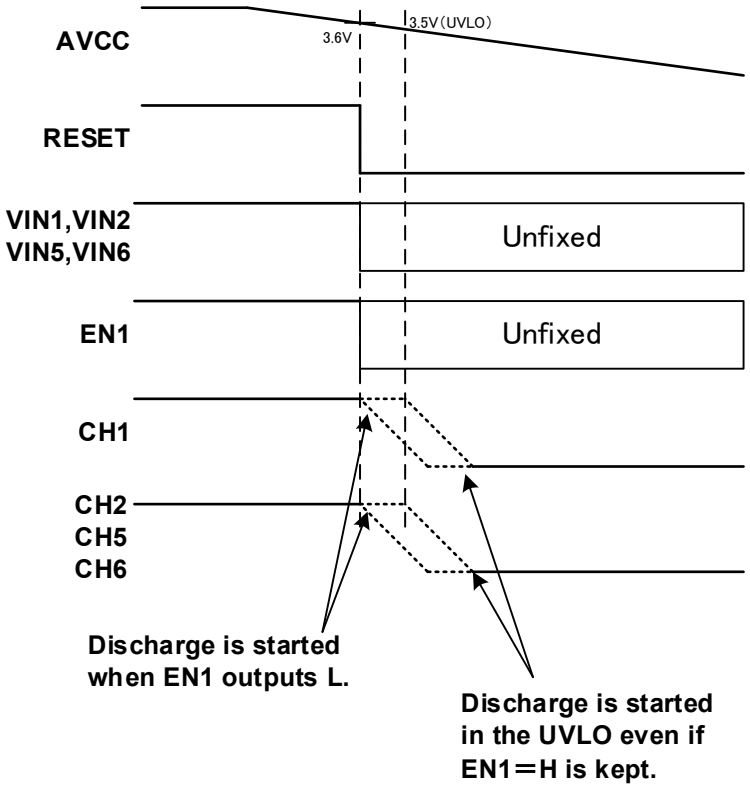
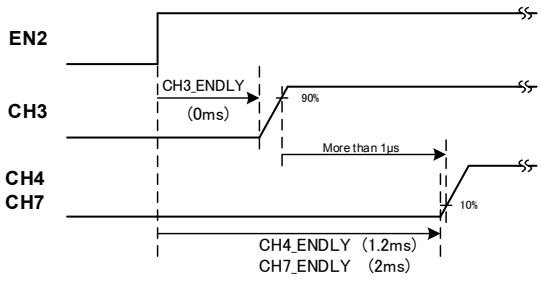


Figure 7.3 Turn off sequence by AVCC voltage drop

7.1.3. Startup sequence of EN2 signal

Each channel starts the startup sequence when receiving EN2="H."

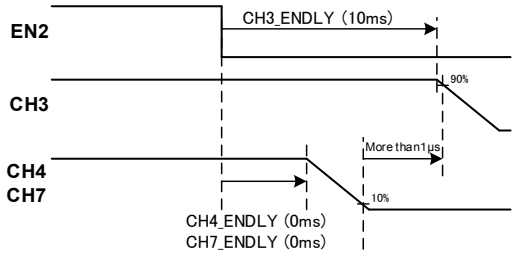


Numerical value in () shows default values.

Figure 7.4 Startup sequence by EN2 signal

7.1.4. Turn off sequence by EN2 signal

(1) Normal sequence
Each channel immediately starts the turn off sequence when receiving EN2=”L.”



Numerical value in () shows default values.

Figure 7.5 Turn off sequence by EN2 signal

(2) Turn off sequence by AVCC voltage drop
In the state of EN2="H," when the AVCC voltage is dropping below the UVLO detection voltage, CH3, Ch4, and CH7 start the turn off operation.
In addition, since the RESET pin voltage is set "L" in the state of which the AVCC voltage is dropping below the RESET detection voltage, the normal sequence starts when EN2 signal is "L." However, when the AVCC voltage is dropping below the UVLO detection voltage in the same state, the turn off sequence starts without waiting for the Delay time.

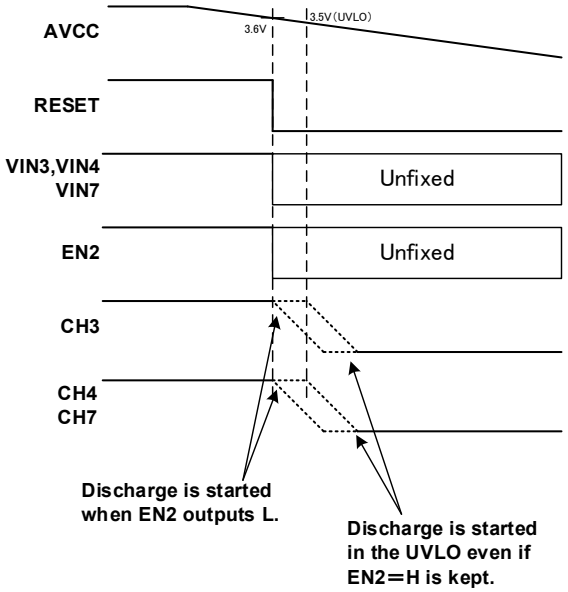
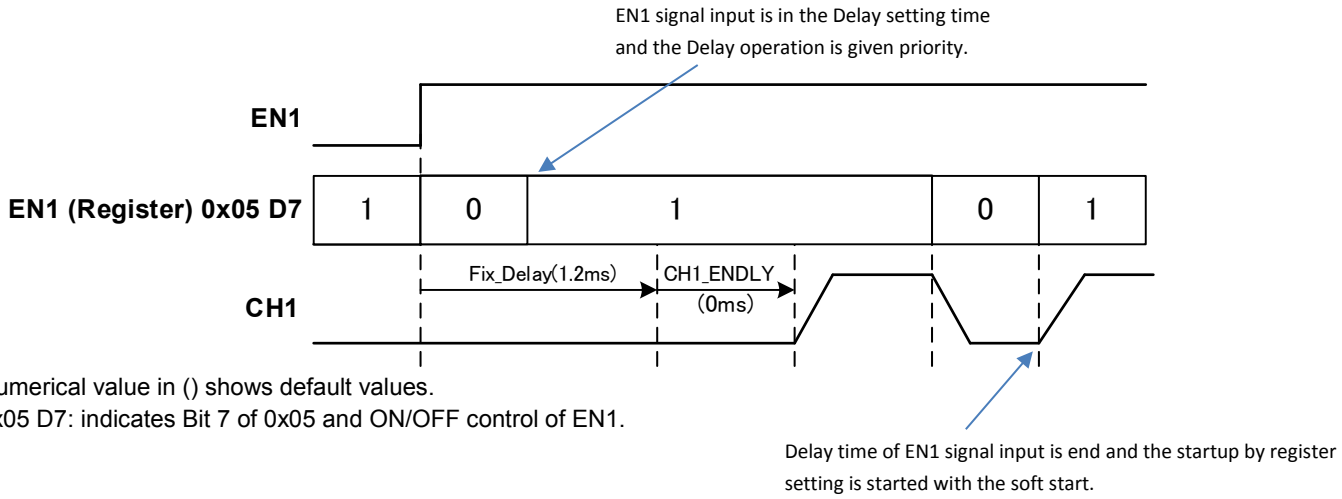


Figure 7.6 Turn off sequence by AVCC voltage drop

7.1.5. Enable control by register setting

In the case of startup by EN1 signal, the enable control by the register setting does not operate during Fix_Delay, and ENDLY period.
Since the normal startup sequence is given priority, the enable control is ON after completion of the Fix_Delay, and ENDLY period.
When the enable control is ON by register setting after completion of the startup by EN signal, perform immediately the startup (soft start operation) without performing ENDLY.

Example: Register control for CH1



Numerical value in () shows default values.
0x05 D7: indicates Bit 7 of 0x05 and ON/OFF control of EN1.

Figure 7.7 Enable control by register setting (0x05)

8. Functions

8.1. DCDC (CH1 and CH2)

This is DCDC Buck converter. The oscillation frequency is 2MHz (CH1) and 1.5MHz (CH2).The PWM or PFM operation can be switched according to the load state, and kept high efficiency even in the light load state.

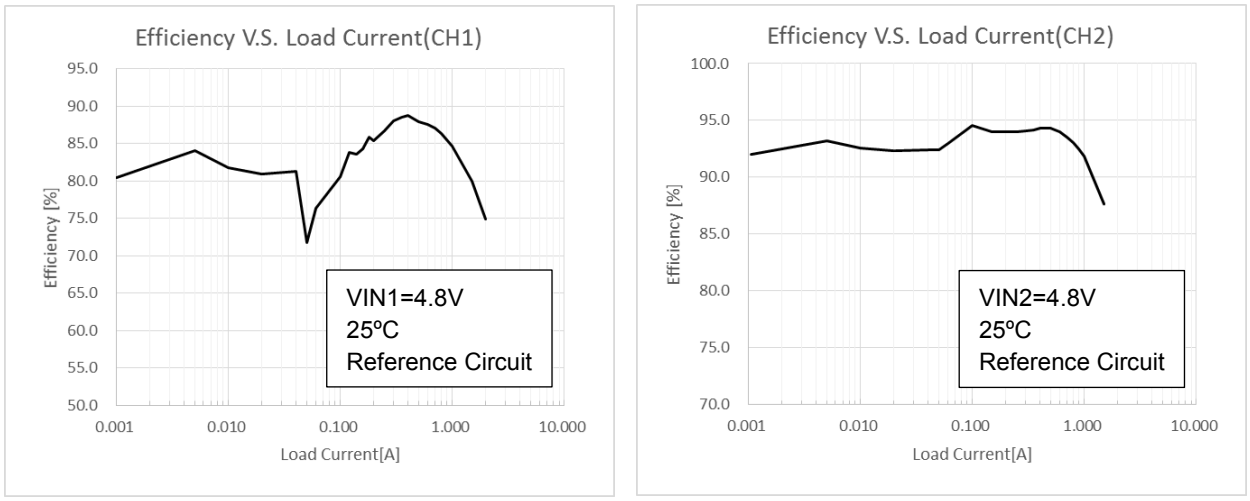


Figure 8.1 Electrical power efficiency characteristics of CH1 and CH2 (Reference value)

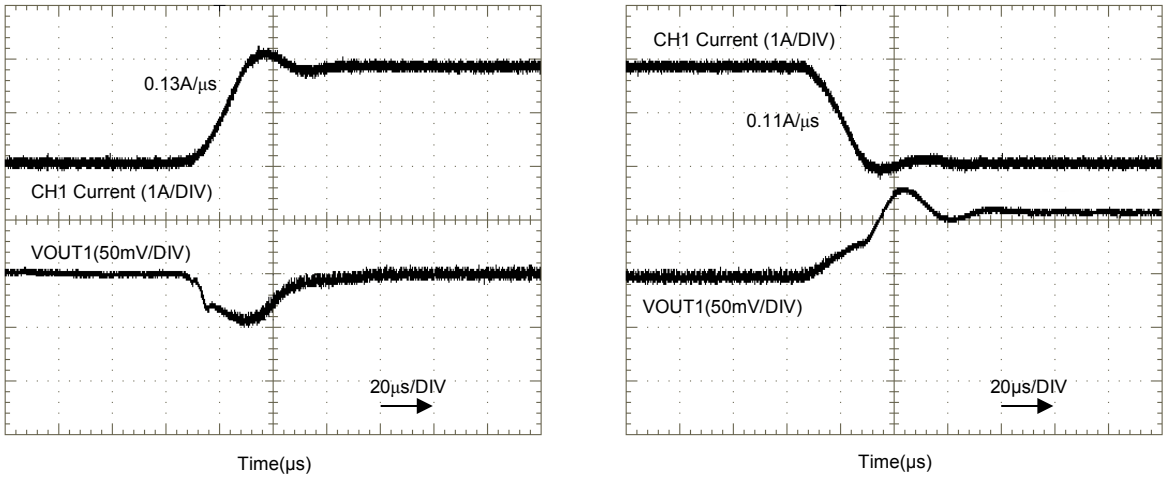


Figure 8.2 Load transient characteristics of CH1(Reference value)

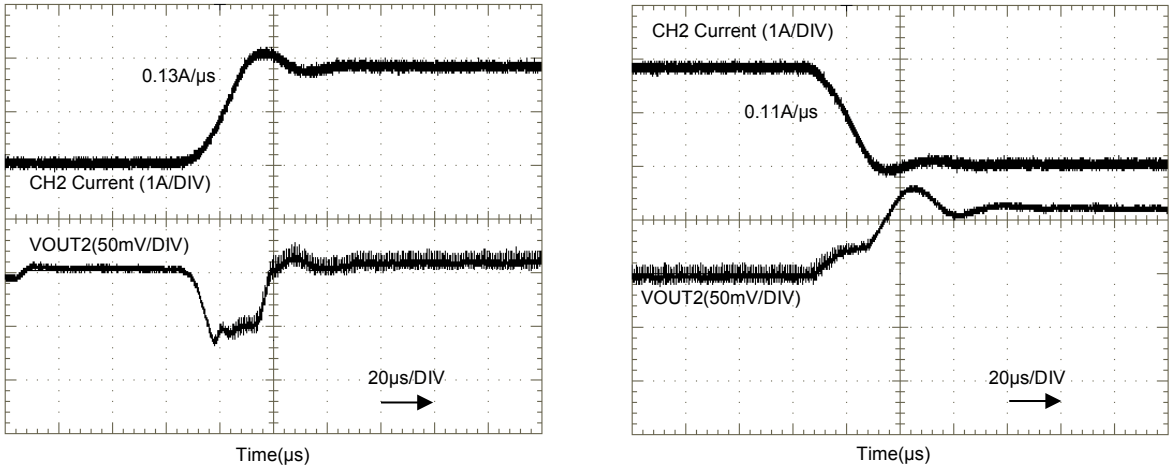


Figure 8.3 Load transient characteristics of CH2(Reference value)

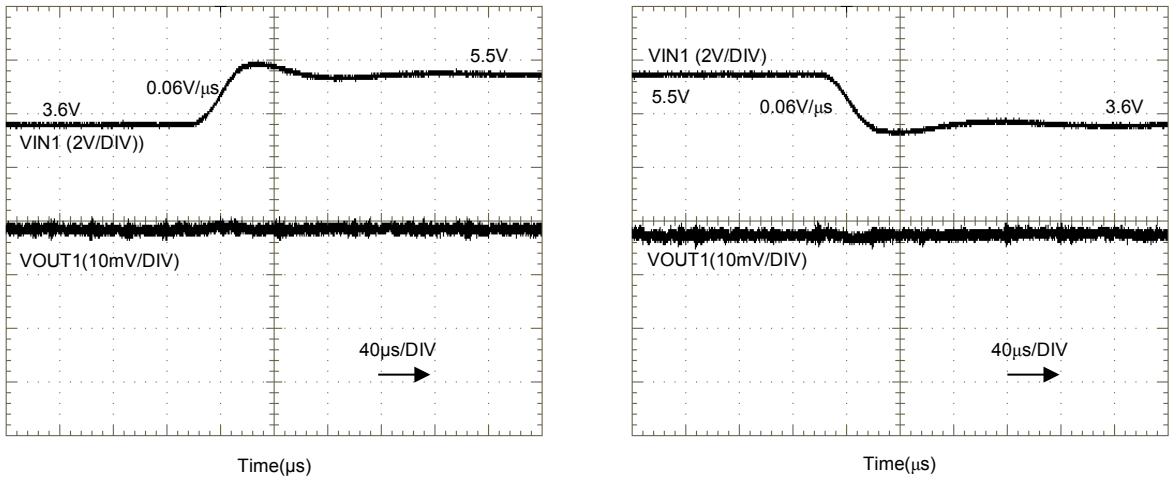


Figure 8.4 Line transient characteristics of CH1 vs VIN1 (Reference value)

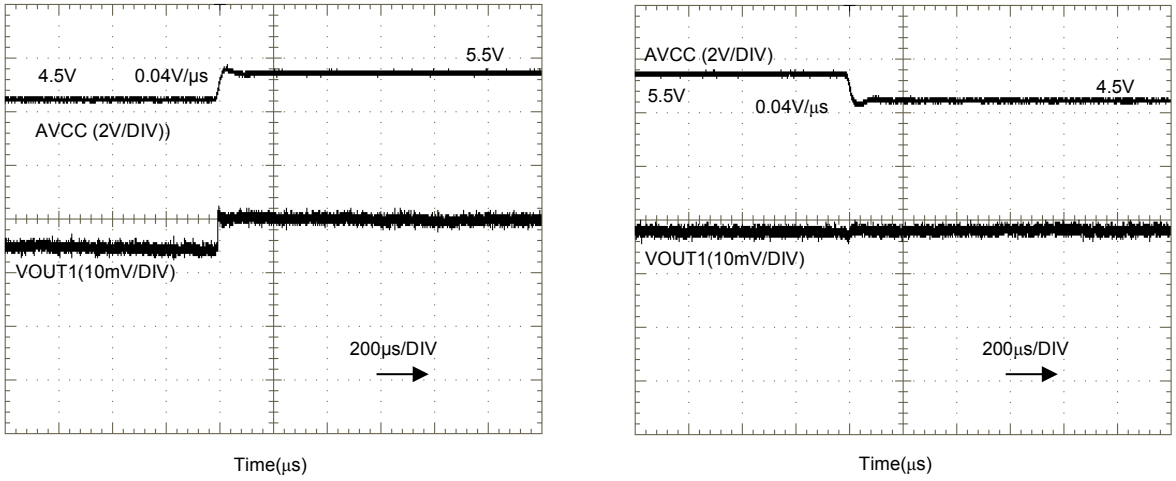


Figure 8.5 Line transient characteristics of CH1 vs AVCC (Reference value)

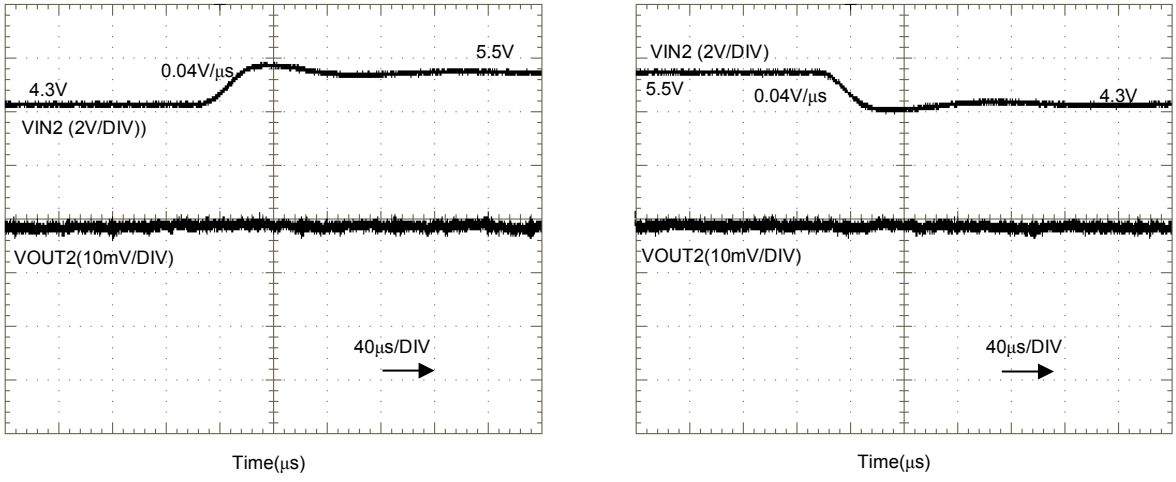


Figure 8.6 Line transient characteristics of CH2 vs VIN2 (Reference value)

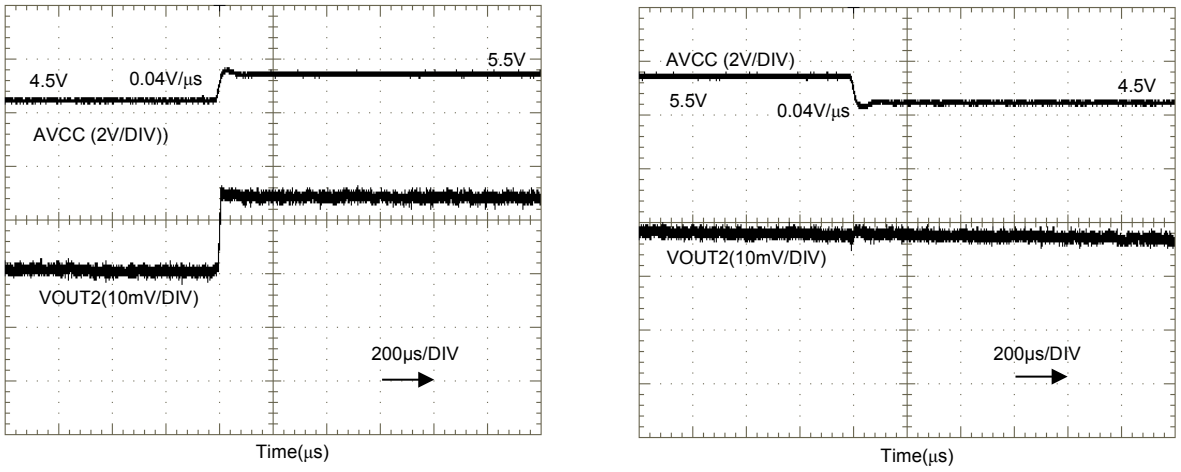


Figure 8.7 Line transient characteristics of CH2 vs AVCC (Reference value)

As the protection functions, this convertor builds in OVP (Over Voltage Protection), UVP (Under Voltage Protection), and OCL (Output Current Limitation). According to the register setting (0x01 [bit4 and bit0]), OVP and UVP can select the latch or Hiccup operation. The default operation is the latch operation.
OVP stops switching if the voltage reaches over the control voltage. When the latch operation is selected by the register setting, the switching is stopped and held after passing regulation time in the state of voltage more than the control voltage. When the Hiccup operation is selected, it returns the normal operation after returning normal voltage.
As for UVP, the OCL operates previously on the function of protection. When the output current is over the OCL current, the output voltage is dropping and the UVP is detected. The UVP latches off when the latch operation is selected. When the Hiccup operation is selected, it returns the normal operation after returning normal voltage.

Note: When OVP and UVP is detected in the case that the Hiccup operation is selected, error information is held after it returns. To returning normal operation, the following operations are required; ON or OFF of the register (0X05), re-startup of the EN signal, and deleting of error information by returning of AVCC power supply.

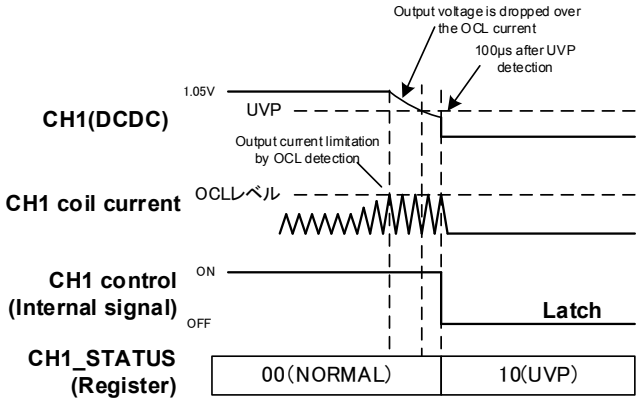


Figure 8.8 Operation at the UVP function latch (Example: CH1)

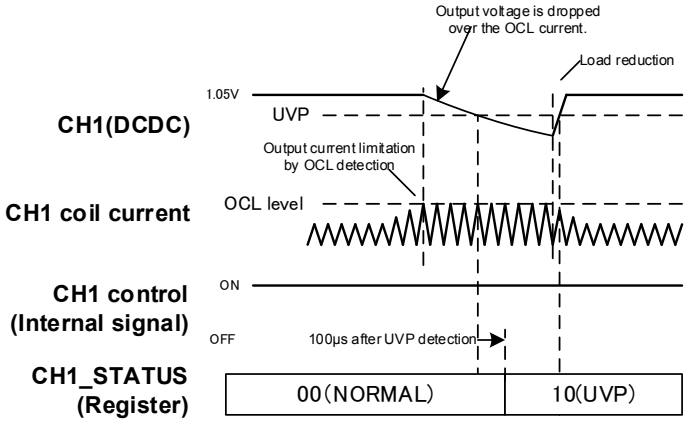


Figure 8.9 Operation at the UVP function Hiccup (Example: CH1)

8.2. LDO (CH3 to CH6)

This is a low dropout regulator.
As the protection functions, this regulator builds in OVP (Over Voltage Protection), UVP (Under Voltage Protection), and OCL (Output Current Limitation). OVP and UVP stop outputting after passing the regulation time, and latch. To returning normal operation, the following operations are required; ON or OFF of the register (0X05), re-startup of the EN signal, and deleting of error information by returning of AVCC power supply.
In addition, output current is controlled with the fold-back characteristic at the overload output.

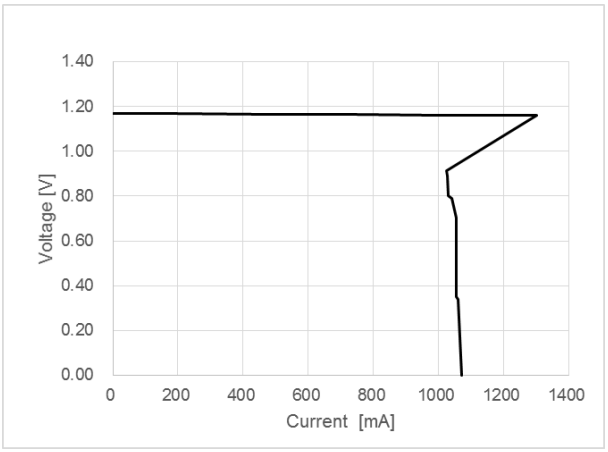


Figure 8.10 Output voltage vs output current characteristics of CH3 (Reference value)

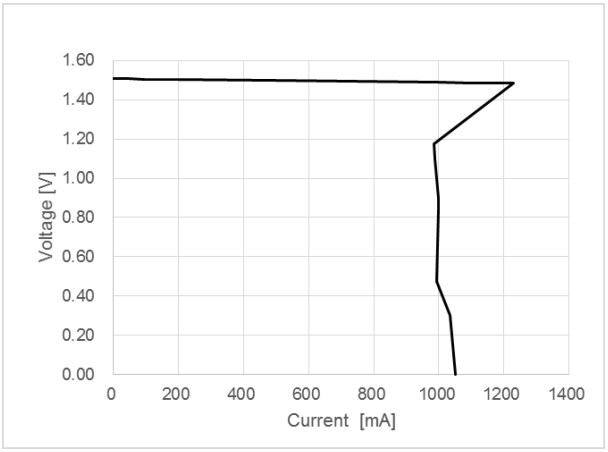


Figure 8.11 Output voltage vs output current characteristics of CH4 (Reference value)

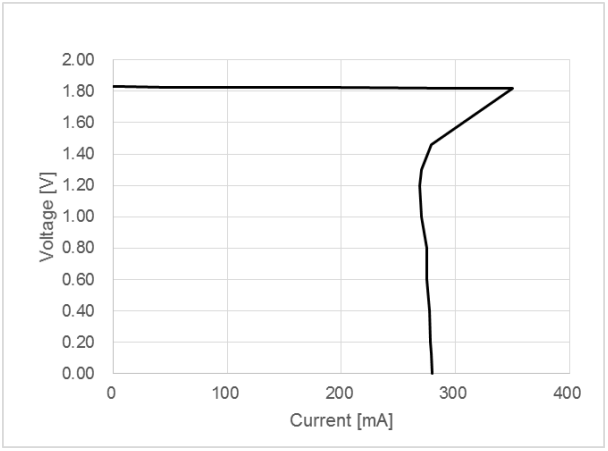


Figure 8.12 Output voltage vs output current characteristics of CH5 (Reference value)

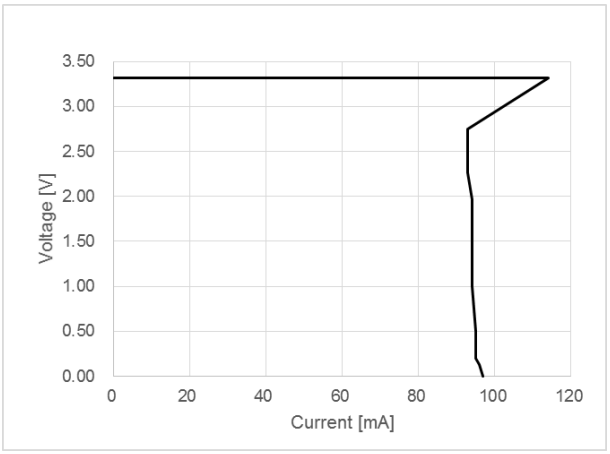


Figure 8.13 Output voltage vs output current characteristics of CH6 (Reference value)

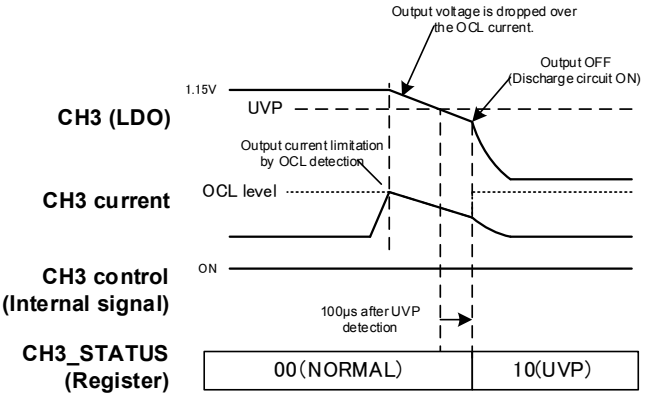


Figure 8.14 Operation at UVP function (Example: CH3)

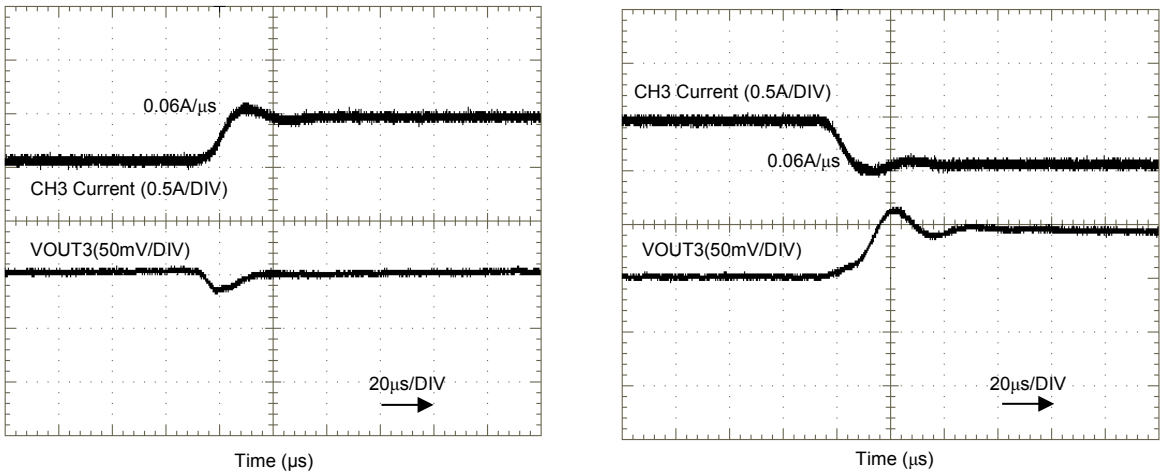


Figure 8.15 Load transient characteristics of CH3 (Reference value)

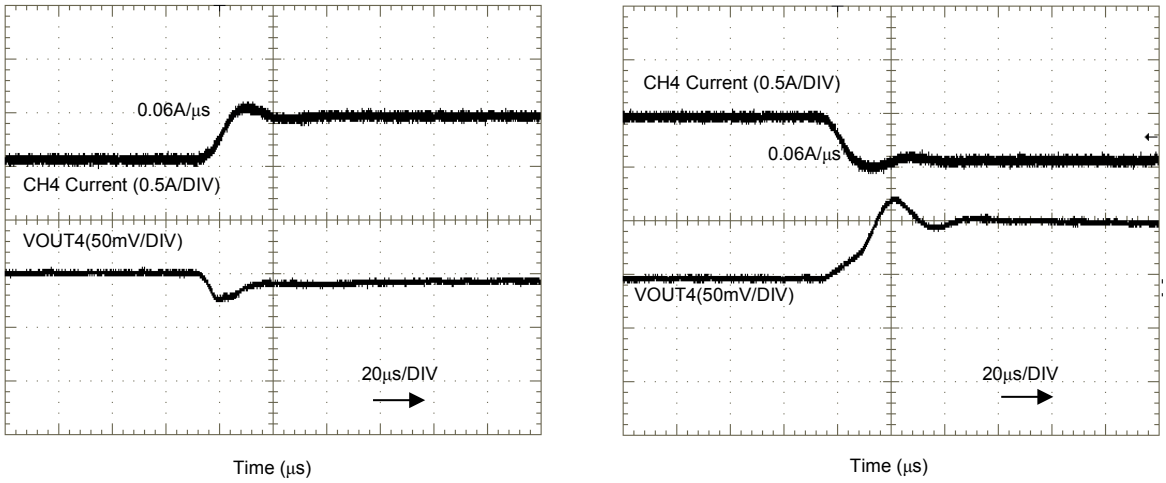


Figure 8.16 Load transient characteristics of CH4 (Reference value)

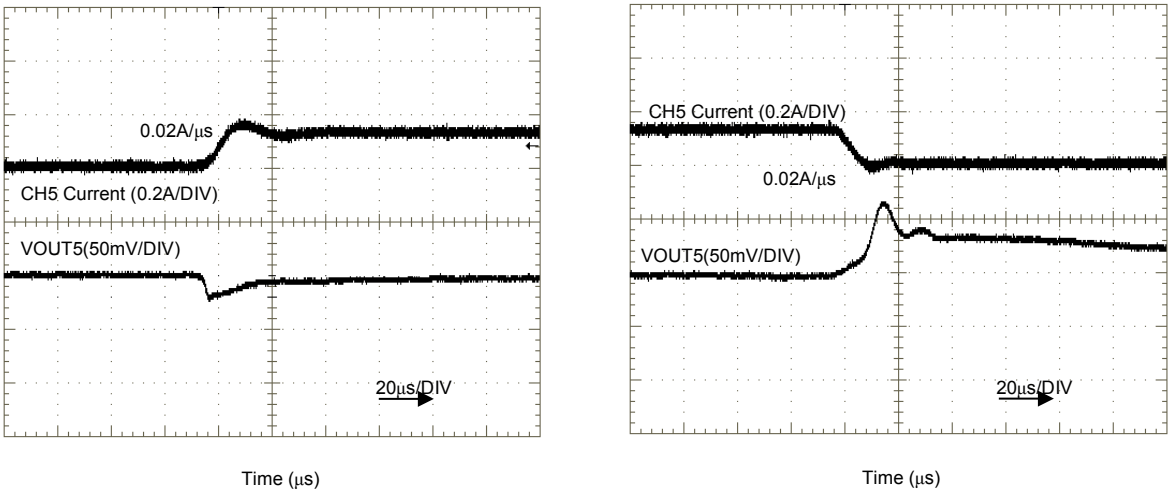


Figure 8.17 Load transient characteristics of CH5 (Reference value)

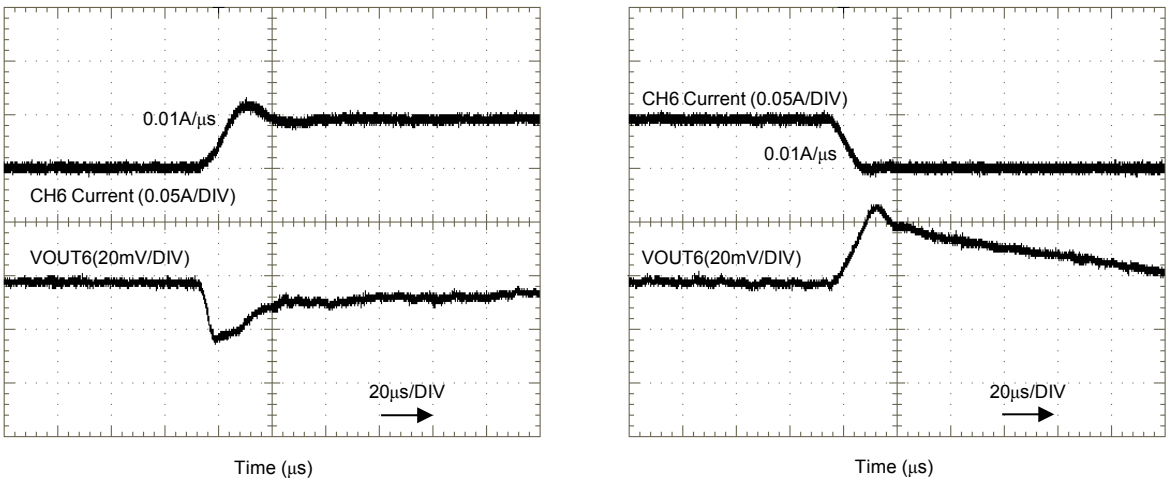


Figure 8.18 Load transient characteristics of CH6 (Reference value)

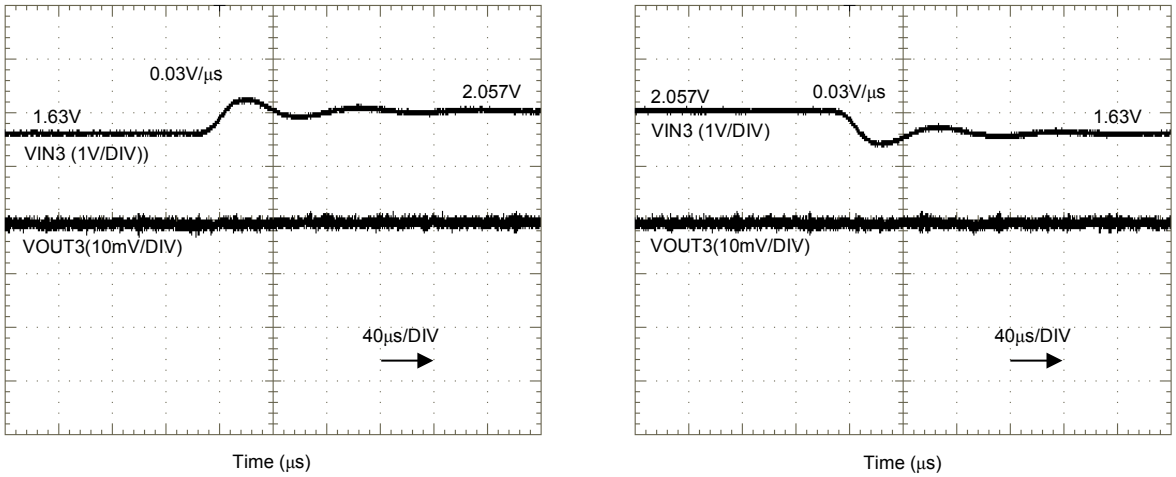


Figure 8.19 Line transient characteristics of CH3 vsVIN3 (Reference value)

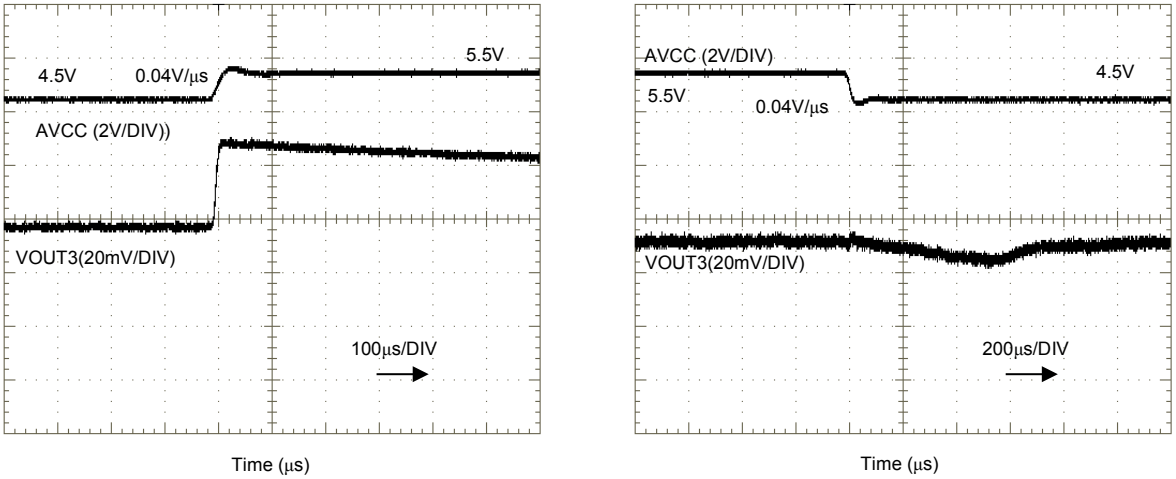


Figure 8.20 Line transient characteristics of CH3 vs AVCC (Reference value)

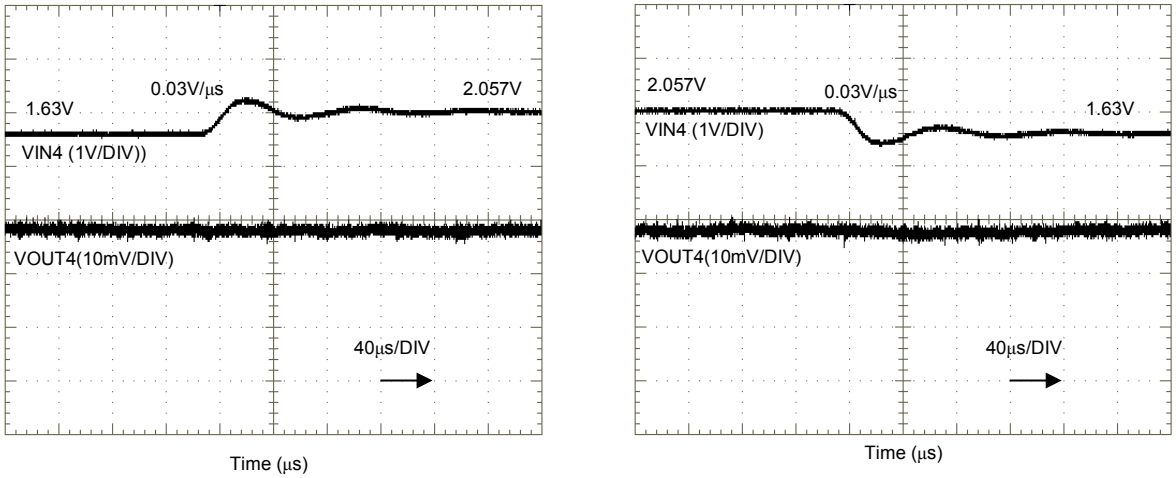


Figure 8.21 Line transient characteristics of CH4 vs VIN4 (Reference value)

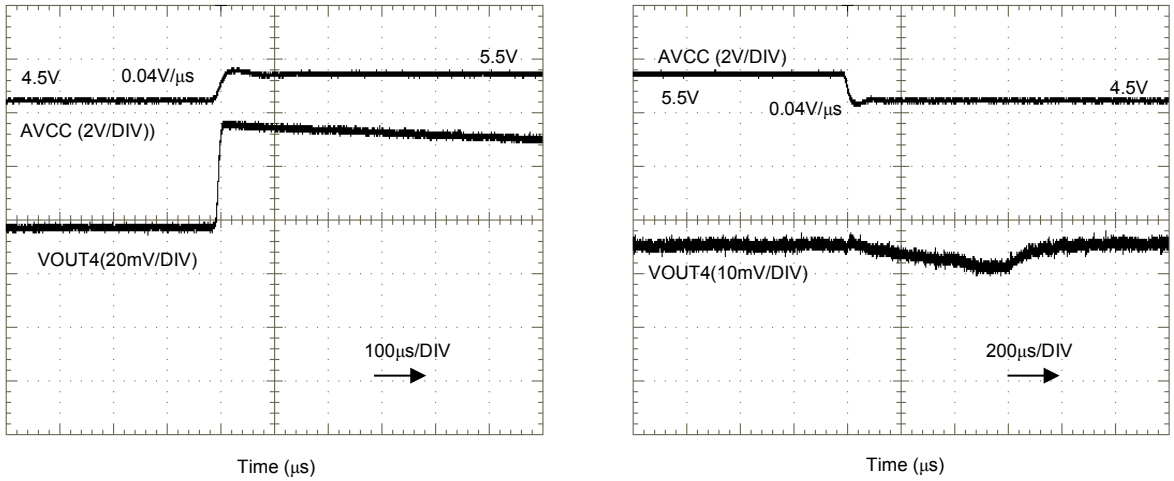


Figure 8.22 Line transient characteristics of CH4 vs AVCC (Reference value)

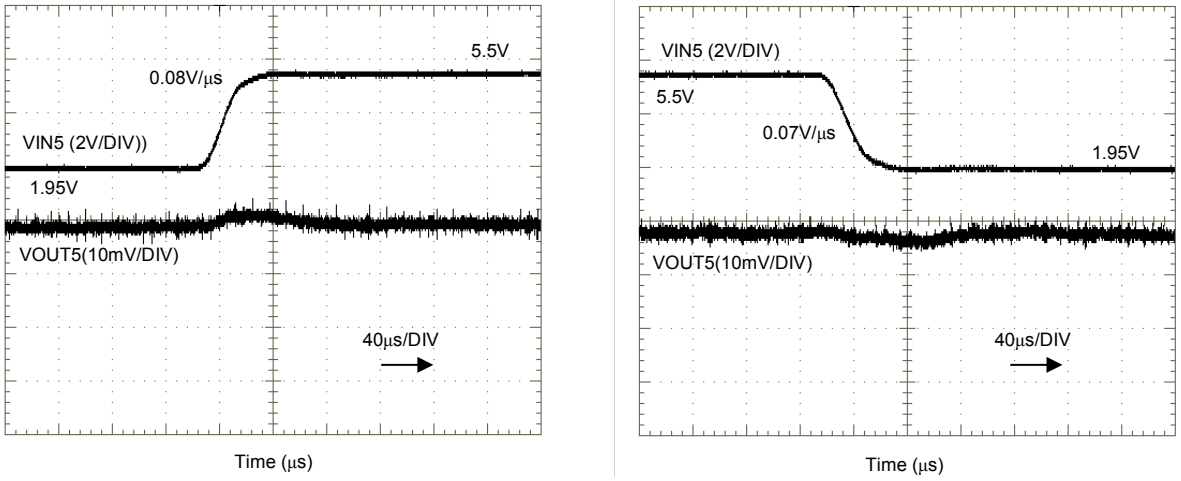


Figure 8.23 Line transient characteristics of CH5 vs VIN5 (Reference value)

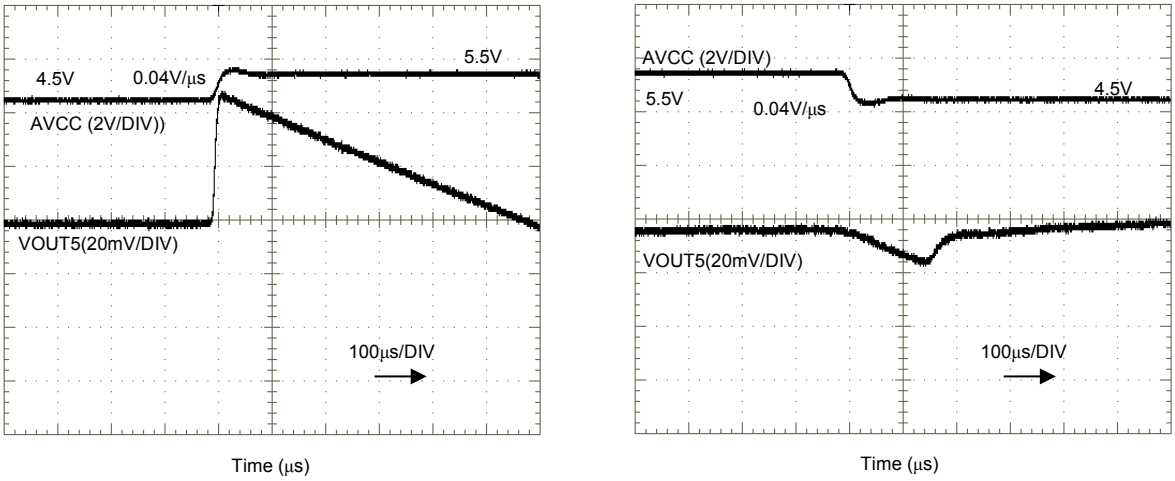


Figure 8.24 Line transient characteristics of CH5 vs AVCC (Reference value)

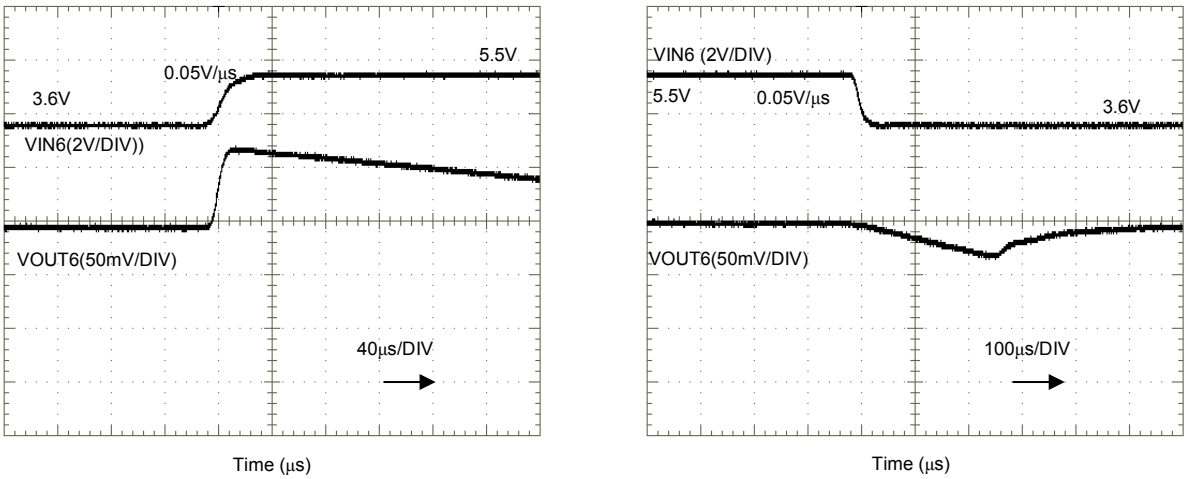


Figure 8.25 Line transient characteristics of CH6 vsVIN6 (Reference value)

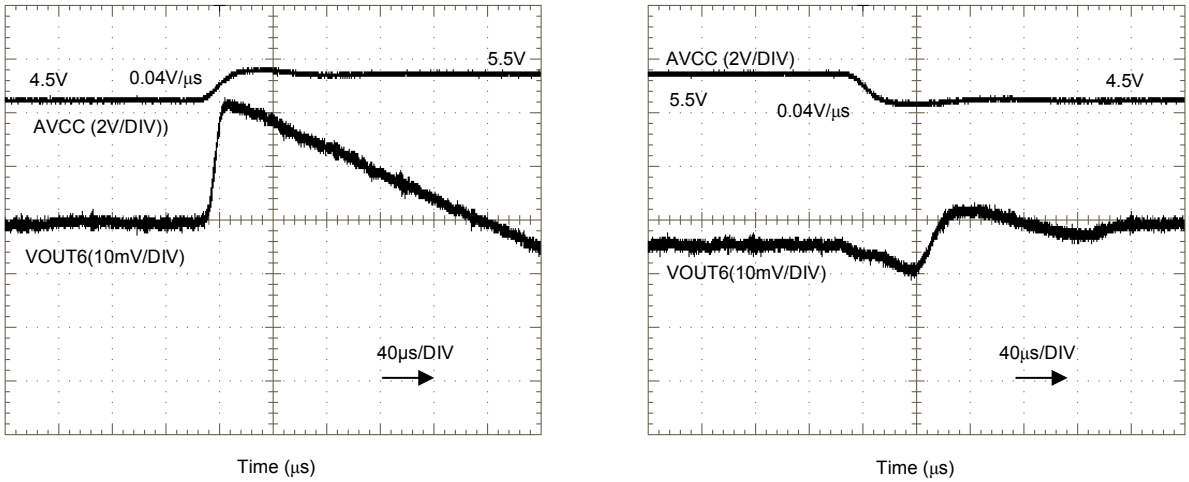


Figure 8.26 Line transient characteristics of CH6 vs AVCC (Reference value)

8.3. Load switch (CH7)

This is a load switch. ON or OFF are controlled by EN2 pin.
The load switch which builds in the soft start function, starts output voltage with monitoring CH7 output voltage. Therefore, it can be controlled with the default soft start time without depending on the output capacity value. As the protection functions, this regulator builds in UVP (Under Voltage Protection), and OCL (Output Current Limitation). UVP stops outputting after passing the regulation time, and latches. To returning normal operation, the following operations are required; ON or OFF of the register (0X05), re-startup of the EN signal, and deleting of error information by returning of AVCC power supply.
As for UVP, the OCL operates previously on the function of protection. When the output current is over the OCL current, the output voltage is dropping and the UVP is detected. Then it latches OFF after passing regulation time.

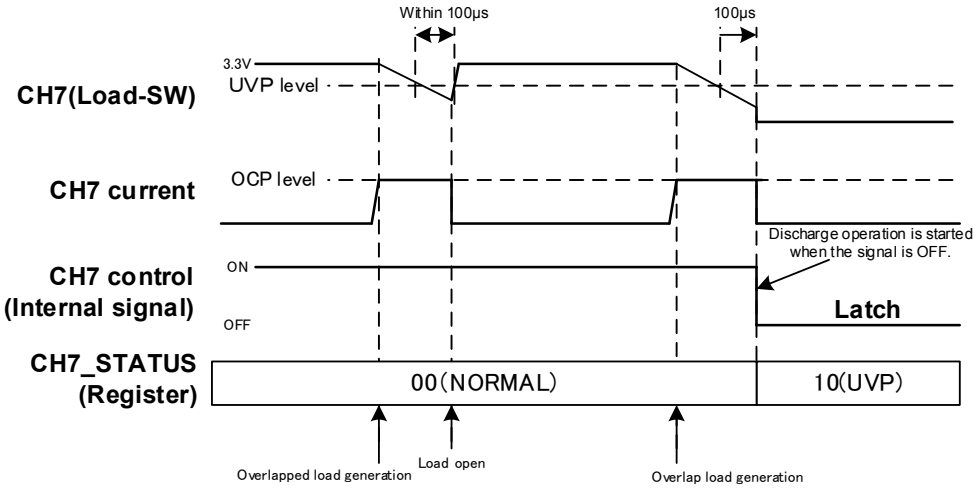


Figure 8.27 Operation at CH7 over load

8.4. Soft start

The soft start function is built in all channels (from CH1 to CH7).
The soft start time except CH7 can be set in the register.
The protection functions (UVP and OVP) of each channel are invalid during operating soft start.

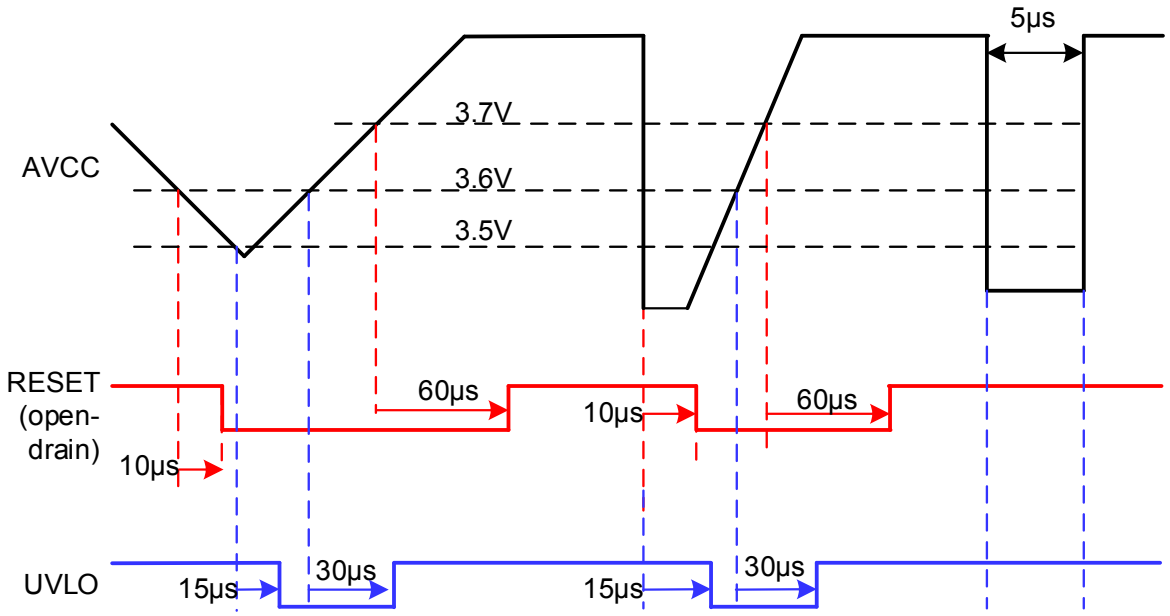
Table 8.1 Soft start time of each channel

CH1_SS	CH1 Soft start time setting (Max): SS[7:6]=00: 600μs **SS[7:6]=01: 800μs (default)** SS[7:6]=10: 1.0ms SS[7:6]=11: 1.2ms
CH2_SS	CH2 Soft start time setting (Max): SS[5:4]=00: 600μs SS[5:4]=01: 800μs **SS[5:4]=10: 1.0ms (default)** SS[5:4]=11: 1.2ms
CH3_SS	CH3 Soft start time setting (Max): SS[3:2]=00: 600μs **SS[3:2]=01: 800μs (default)** SS[3:2]=10: 1.0ms SS[3:2]=11: 1.2ms
CH4_SS	CH4 Soft start time setting (Max): SS[1:0]=00: 600μs SS[1:0]=01: 800μs **SS[1:0]=10: 1.0ms (default)** SS[1:0]=11: 1.2ms
CH5_SS	CH5 Soft start time setting (Max): SS[7:6]=00: 600μs SS[7:6]=01: 800μs **SS[7:6]=10: 1.0ms (default)** SS[7:6]=11: 1.2ms
CH6_SS	CH6 Soft start time setting (Max): SS[5:4]=00: 600μs SS[5:4]=01: 800μs **SS[5:4]=10: 1.0ms (default)** SS[5:4]=11: 1.2ms
CH7_SS	CH7 Soft start time setting: 500μs(Typ.) fixed

8.5. Reset signal generation circuit

This IC incorporates the RESET circuit for monitoring the voltage state of the AVCC power supply. After detecting less than the reference voltage (3.6V Typ.), “L” is output to the RESET pin voltage after passing regulation time. After detecting more than the reference voltage (3.7V Typ.), “Hi-z” is output to the RESET pin voltage after passing regulation time.
The regulation time can be set in the register (0x11).
The detection and returning voltage of the UVLO are set lower 100 mV (Typ.) than that of the RESET.

In addition, the signal is not output when the change of the power-down or power-up time is within the mask setting time.



*All values in the figure are typical values.

Figure 8.28 Relation between RESET circuit operation and UVLO

9. Protection functions

This IC incorporates whole system protection functions (TSD and UVLO) and each channel protection functions (OVP, UVP, and OCL).

Table 9.1 Protection functions

Circuit	CH	Protection functions		
		Over Current Limitation (OCL)	Over Voltage Protection (OVP)	Under Voltage Protection (UVP)
DCDC	CH1	Available (Hiccup to UVP)	Available (Latch / Hiccup)	Available (Latch / Hiccup)
	CH2	Available (Hiccup to UVP)	Available (Latch / Hiccup)	Available (Latch / Hiccup)
LDO	CH3	Available (Drooping to UVP)	Available(Latch)	Available(Latch)
	CH4	Available (Drooping to UVP)	Available(Latch)	Available(Latch)
	CH5	Available (Drooping to UVP)	Available(Latch)	Available(Latch)
	CH6	Available (Drooping to UVP)	Available(Latch)	Available(Latch)
SW	CH7	Available (Latch OFF)	Not available	Available(Latch)

- The Latch or Hiccup operation can be switched by the register setting. The initial state is Latch operation. When the Hiccup operation is selected, it returns automatically.
- Although the OCL of the DCDC and LDO are the Hiccup operation, if the current flows over limitation voltage, the output voltage is dropping and the UVP is detected.

9.1. TSD

In the case that IC temperature exceeds 150°C (Typ.), it moves to "ERROR STOP" state, and all outputs are stopped and the shutdown state is held. In order to reset the shutdown state, the EN1 signal should be set to "L" once, and input "H" again, or the AVCC power supply should be reset.

9.2. Input UVLO

This IC incorporates the UVLO circuit to monitor the voltage state of the AVCC power supply and to control internal circuit operation. After detecting below the reference voltage (3.5V Typ.), it moves to the power off state. After detecting more than the reference voltage (3.6V Typ.), it moves to the shutdown state. In order to prevent the error operation by noise, it masks and does not react to the change within 5μs

9.3. Over Voltage Protection (OVP)

The channels from CH1 to CH6 incorporate the OVP circuit to monitor the overvoltage. After detecting the state which is over the reference voltage (120% Typ.) for the regulation time (100μs Typ.), the output is stopped and the state is held.
In order to return, the register (0x05) should be ON or OFF, the EN signal should be restarted, and the error information should be deleted by the restart of AVCC power supply. The detection voltage can be set in the register (0x0F and 0x10).

Note: CH1 and CH2 can be set the Hiccup operation by the register setting (0x01). In the case of detecting also OVP at the Hiccup operation, although the output is stopped, the normal operation is returned when the output voltage is less than the OVP detecting voltage. However, since the information of the OVP detection remains in the STATUS register (0x0B), in order to clear the STATUS register information, the register (0x05) should be ON or OFF, the EN signal should be restarted, and the AVCC power supply should be restarted.

9.4. Under Voltage Protection (UVP)

The channels from CH1 to CH7 incorporate the UVP circuit to monitor the under voltage.
In the channels from CH1 to CH6, after detecting the voltage less than the reference voltage (70% Typ.) for the regulation time (100μs Typ.), the output is stopped and the state is held. In order to return, the register (0x05) should be ON or OFF, the EN signal should be restarted, and the error information should be deleted by the restart of AVCC power supply. The detecting voltage of channels from CH1 to CH6 can be set by the register (0x0D and 0x0E).
In the CH7, after detecting voltage less than the reference voltage (2.3V Typ.) for the regulation time (100μs Typ.), the output is stopped and the state is held. In order to return, the register (0x05) should be ON or OFF, the EN signal should be restarted, and the error information should be deleted by the restart of AVCC power supply.

Note: CH1 and CH2 can be set the Hiccup operation by the register setting (0x01). In the case of detecting also UVP at the Hiccup operation, although the output is stopped, the normal operation is returned when the output voltage is more than the UVP detecting voltage. However, since the information of the UVP detection remains in the STATUS register (0x0B), in order to clear the STATUS register information, the register (0x05) should be ON or OFF, the EN signal should be restarted, and the AVCC power supply should be restarted.

9.5. Output Over Current Limitation (OCL)

The channels from CH1 to CH7 incorporate the OCL circuit to limit the output current in the case of the overcurrent output. This function limits the output current automatically when the output current is more than the reference current. In this state, if the current returns to less than the reference value, the normal operation is returned automatically. Although the error stop does not performed with this function, if the current flows more than the reference value, the output voltage is dropped by the operation of this function. As the result, the UVP is detected and the output stop may be latched.

10. External components selection

In this product, the characteristics are verified using the following components.
Refer to the following list, and select suitable external components.

Table 10.1 External components selection

Parts No.	Notes	Value	Voltage-resistant	Thermal Characteristics	Size	Name of components	Maker
R1	Pull up resistance for the reset output	10kΩ	—	—	—	—	—
R2	Pull up resistance for I^2C (SDA)	2.2kΩ	—	—	—	—	—
R3	Pull up resistance for I^2C (SCL)	2.2kΩ	—	—	—	—	—
C1	Input capacitor for AVCC	10μF	10V	X5R	2012	GRM21BR61A106ME19L	Murata
C2	Input capacitor for CH1 (1.05V)	22μF	6.3V	X5R	2012	GRM21BR60J226ME39L	Murata
C3-1	Output capacitor for CH1 (1.05V)	22μF	6.3V	X5R	1608	GRM188R60J226MEA0D	Murata
C3-2	Output capacitor for CH1 (1.05V)	22μF	6.3V	X5R	1608	GRM188R60J226MEA0D	Murata
C4	Input capacitor for CH2 (3.3V)	22μF	6.3V	X5R	2012	GRM21BR60J226ME39L	Murata
C5-1	Output capacitor for CH2 (3.3V)	22μF	6.3V	X5R	2012	GRM21BR60J226ME39L	Murata
C5-2	Output capacitor for CH2 (3.3V)	22μF	6.3V	X5R	2012	GRM21BR60J226ME39L	Murata
C5-3	Output capacitor for CH2 (3.3V)	22μF	6.3V	X5R	2012	GRM21BR60J226ME39L	Murata
C6	Input capacitor for CH3(1.15V)	10μF	6.3V	X5R	1608	GRM188R60J106ME47D	Murata
C7	Output capacitor for CH3 (1.15V)	22μF	6.3V	X5R	1608	GRM188R60J226MEA0D	Murata
C8	Input capacitor for CH4 (1.5V)	10μF	6.3V	X5R	1608	GRM188R60J106ME47D	Murata
C9	Output capacitor for CH4 (1.5V)	22μF	6.3V	X5R	1608	GRM188R60J226MEA0D	Murata
C10	Input capacitor for CH5 (1.8V)	2.2μF	16V	X5R	1608	GRM188R61C225KE15D	Murata
C11	Output capacitor for CH5 (1.8V)	2.2μF	6.3V	X5R	1608	GRM155R60J225ME95E	Murata
C12	Input capacitor for CH6 (1.8V)	2.2μF	16V	X5R	1608	GRM188R61C225KE15D	Murata
C13	Output capacitor for CH6 (1.8V)	2.2μF	6.3V	X5R	1608	GRM155R60J225ME95E	Murata
C14	Input capacitor for CH7 (SW)	2.2μF	6.3V	X5R	1608	GRM155R60J225ME95E	Murata
C15	Output capacitor for CH7 (SW)	2.2μF	6.3V	X5R	1608	GRM155R60J225ME95E	Murata
L1	Inductor for CH1	1.0μH	—	—	2520	MDT250-CR1R0M	Toko
L2	Inductor for CH2	1.0μH	—	—	2520	MDT250-CR1R0M	Toko

11. I²C Operation

TC7739FTG sets each function with the I²C interface. The slave operation and fast mode (400kHz) compliant with I²C standard are supported. The single write operation, continuous write operation, single read operation, and continuous read operation can be performed. The slave address of the TC7739FTG is fixed to 0b1100100. The stretch function is not used.
Manufacturer ID: Address (0x00) = 0xAC (10101100)

11.1. I²C IF

Table 11.1 Chip address

	MSB							LSB
ADD	1	1	0	0	1	0	0	R/$\overline{W}$

11.2. I²C write mode

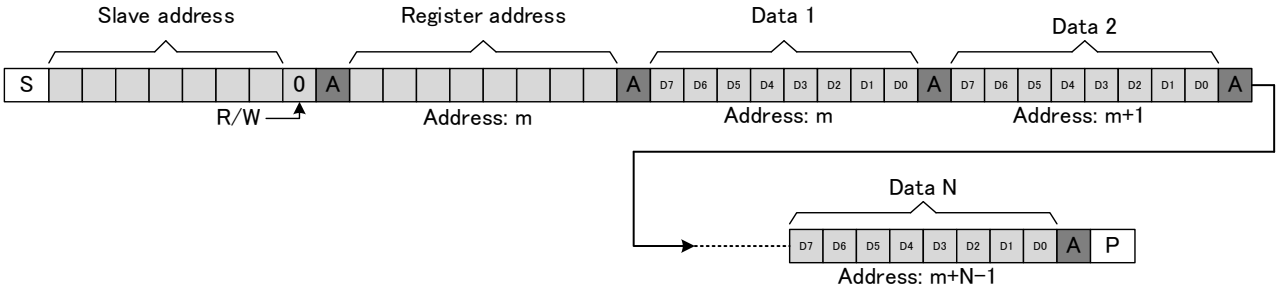


Figure 11.1 Write mode format

11.3. I²C read mode

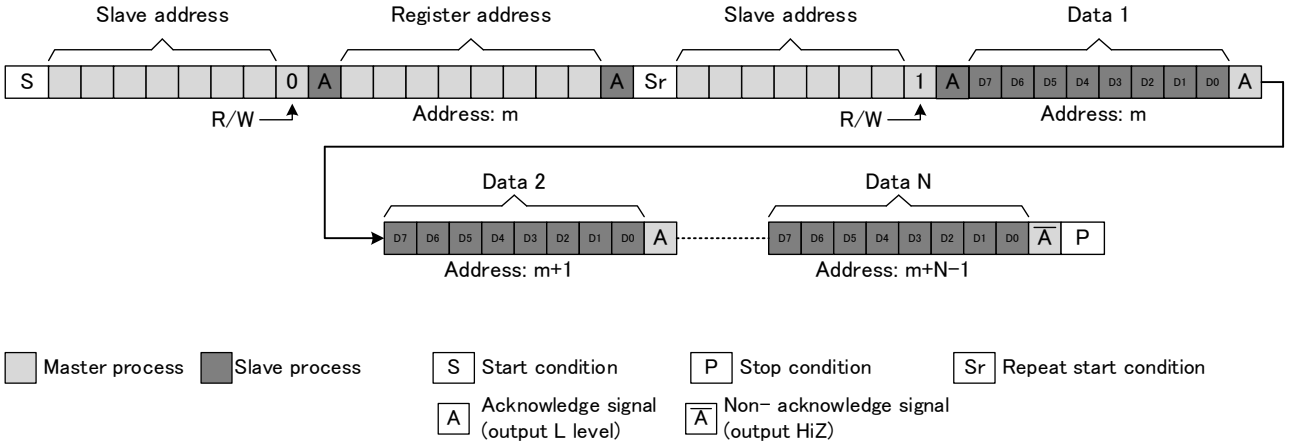


Figure 11.2 read mode format

12. Register map

Table 12.1 I^2C register and function

Address	Register Name	R/W	Function
0x00	Manufacturer_ID	R/W	Manufacturer ID
0x01	BUCK_REG	R/W	CH1 and CH2 setting
0x02	LDO_REG1	R/W	CH3 and CH4 setting
0x03	LDO_REG2	R/W	CH5 and CH6 setting
0x04	DISCHARGE	R/W	CH1 to CH6 Discharge operation setting
0x05	Enable	R/W	CH1 to CH7 ON/OFF setting
0x06	SS_Time1	R/W	CH1 to CH4 soft start time setting
0x07	SS_Time2	R/W	CH5 to CH6 soft start time setting
0x08	ENDLY_Time1	R/W	CH1 to CH4 startup Delay time setting
0x09	ENDLT_Time2	R/W	CH5 to CH7 startup Delay time setting
0x0A	DISENDLY_Time	R/W	CH3,4,6,7 shutdown Delay time setting
0x0B	STATUS_REG1	R	CH1 to CH4 state output
0x0C	STATUS_REG2	R	CH5 to CH7 state output
0x0D	UV_SETTING1	R/W	CH1 to CH4 UVP voltage setting
0x0E	UV_SETTING2	R/W	CH5 and 6 UVP voltage setting
0x0F	OV_SETTING1	R/W	CH1 to CH4 OVP voltage setting
0x10	OV_SETTING2	R/W	CH5 and 6 OVP voltage setting

12.1. Register description 1 (0x00 to 0x03)

Table 12.2 0x00 to 0x03

Address	Register name	Bit	Bit name	Default	R/W	Description
0x00	Manufacturer_ID	7:0	Manufacturer_ID	0xAC	R	manufacturer ID
0x01	BUCK_REG	7:5	CH1_SEL	0x01	RW	CH1 Output voltage setting (default: 1.05V) SEL[3:1]=000: 1.04V **SEL[3:1]=001: 1.05V (default)** SEL[3:1]=010: 1.06V SEL[3:1]=011: 1.07V SEL[3:1]=100: 1.08V SEL[3:1]=101: 1.09V SEL[3:1]=110: 1.10V SEL[3:1]=111: 1.11V
		4	CH1_Latchup	0x00	RW	Processing when CH1 protection operation is detected. **0: Latch operation (default)** 1: Return automatically
		3:1	CH2_SEL	0x02	RW	CH2 Output voltage setting (default: 3.3V) SEL[3:1]=000: 3.28V SEL[3:1]=001: 3.29V **SEL[3:1]=010: 3.3V(default)** SEL[3:1]=011: 3.31V SEL[3:1]=100: 3.32V SEL[3:1]=101: 3.33V SEL[3:1]=110: 3.34V SEL[3:1]=111: 3.36V
		0	CH2_Latchup	0x00	RW	Processing when CH2 protection operation is detected. **0: Latch operation (default)** 1: Return automatically
0x02	LDO_REG1	7:5	CH3_SEL	0x02	RW	CH3 Output voltage setting (default: 1.15V) SEL[3:1]=000: 1.13V SEL[3:1]=001: 1.14V **SEL[3:1]=010: 1.15V(default)** SEL[3:1]=011: 1.16V SEL[3:1]=100: 1.17V SEL[3:1]=101: 1.18V SEL[3:1]=110: 1.19V SEL[3:1]=111: 1.20V
		4	Reserved	0x00	R	—
		3:1	CH4_SEL	0x00	RW	CH4 Output voltage setting (default: 1.50V) **SEL[3:1]=000: 1.50V(default)** SEL[3:1]=001: 1.51V SEL[3:1]=010: 1.52V SEL[3:1]=011: 1.53V SEL[3:1]=100: 1.35V SEL[3:1]=101: 1.36V SEL[3:1]=110: 1.37V SEL[3:1]=111: 1.38V
		0	Reserved	0x00	R	—
0x03	LDO_REG2	7:5	CH5_SEL	0x02	RW	CH5 Output voltage setting (default: 1.80V) SEL[3:1]=000: 1.78V SEL[3:1]=001: 1.79V **SEL[3:1]=010: 1.80V(default)** SEL[3:1]=011: 1.81V SEL[3:1]=100: 1.82V SEL[3:1]=101: 1.83V SEL[3:1]=110: 1.85V SEL[3:1]=111: 1.86V
		4	Reserved	0x00	R	—
		3:1	CH6_SEL	0x02	RW	CH6 Output voltage setting (default: 3.3V) 000: 3.28V 001: 3.29V **010: 3.3V(default)** 011: 3.31V 100: 3.32V 101: 3.33V 110: 3.34V 111: 3.36V
		0	Reserved	0x00	R	—

12.2. Register description 2 (0x04 to 0x07)

Table 12.3 0x04 to 0x07

Address	Register name	Bit	Bit name	Default	R/W	Description
0x04	DISCHARGE	7	Reserved	0x00	R	—
		6	DISCH1	0x01	RW	0: CH1 Discharge processing OFF **1: CH1 Discharge processing ON(default)**
		5	DISCH2	0x01	RW	0: CH2 Discharge processing OFF **1: CH2 Discharge processing ON(default)**
		4	DISCH3	0x01	RW	0: CH3 Discharge processing OFF **1: CH3 Discharge processing ON(default)**
		3	DISCH4	0x01	RW	0: CH4 Discharge processing OFF **1: CH4 Discharge processing ON(default)**
		2	DISCH5	0x01	RW	0: CH5 Discharge processing OFF **1: CH5 Discharge processing ON(default)**
		1	DISCH6	0x01	RW	0: CH6 Discharge processing OFF **1: CH6 Discharge processing ON(default)**
		0	DISCH7	0x01	RW	0: CH7 Discharge processing OFF **1: CH7 Discharge processing ON(default)**
0x05	Enable (Note1)	7	EN1	0x01	RW	0: CH1 OFF (Protection information is reset.) **1: CH1 ON (Startup from the soft start without performing ENDLY) (default)**
		6	EN2	0x01	RW	0: CH2 OFF (Protection information is reset.) **1: CH2 ON (Startup from the soft start without performing ENDLY) (default)**
		5	EN3	0x01	RW	0: CH3 OFF (Protection information is reset.) **1: CH3 ON (Startup from the soft start without performing ENDLY) (default)**
		4	EN4	0x01	RW	0: CH4 OFF (Protection information is reset.) **1: CH4 ON (Startup from the soft start without performing ENDLY) (default)**
		3	EN5	0x01	RW	0: CH5 OFF (Protection information is reset.) **1: CH5 ON (Startup from the soft start without performing ENDLY) (default)**
		2	EN6	0x01	RW	0: CH6 OFF (Protection information is reset.) **1: CH6 ON (Startup from the soft start without performing ENDLY) (default)**
		1	EN7	0x01	RW	0: CH7 OFF (Protection information is reset.) **1: CH7 ON (Startup from the soft start without performing ENDLY) (default)**
		0	EN347 (Note2)	0x01	RW	0: CH3,4,7 OFF (Protection information is reset.) **1: CH3,4,7 ON (Startup from the soft start without performing ENDLY) (default)**
0x06	SS_Time1	7:6	CH1_SS	0x01	RW	CH1 Soft start time setting (MAX): SS[7:6]=00: 600µs **SS[7:6]=01: 800µs (default)** SS[7:6]=10: 1.0ms SS[7:6]=11: 1.2ms
		5:4	CH2_SS	0x02	RW	CH2 Soft start time setting (MAX): SS[5:4]=00: 600µs SS[5:4]=01: 800µs **SS[5:4]=10: 1.0ms (default)** SS[5:4]=11: 1.2ms
		3:2	CH3_SS	0x01	RW	CH3 Soft start time setting (MAX): SS[3:2]=00: 600µs **SS[3:2]=01: 800µs (default)** SS[3:2]=10: 1.0ms SS[3:2]=11: 1.2ms
		1:0	CH4_SS	0x02	RW	CH4 Soft start time setting (MAX): SS[1:0]=00: 600µs SS[1:0]=01: 800µs **SS[1:0]=10: 1.0ms (default)** SS[1:0]=11: 1.2ms
0x07	SS_Time2	7:6	CH5_SS	0x02	RW	CH5 Soft start time setting (MAX): SS[7:6]=00: 600µs SS[7:6]=01: 800µs **SS[7:6]=10: 1.0ms (default)** SS[7:6]=11: 1.2ms
		5:4	CH6_SS	0x02	RW	CH6 Soft start time setting (MAX): SS[5:4]=00: 600µs SS[5:4]=01: 800µs **SS[5:4]=10: 1.0ms (default)** SS[5:4]=11: 1.2ms
		3:0	Reserved	0x00	R	—

Note1: The Delay time setting is enabled immediately after inputting “H” to the input pins (EN1 pin input and EN2 pin input). Then this register is masked after passing the Delay time. (Refer to 7.1.5 Enable control by register setting.)

Note2: If Either of EN347 and EN3, EN4, and EN7 is ”0,” it seems to be ”0” and operates. (AND processing)

12.3. Register description 3 (0x08 to 0x0A)

Table 12.4 0x08 to 0x0A

Address	Register name	Bit	Bit name	Default	R/W	Description
0x08	ENDLY_Time1	7:6	CH1_ENDLY	0x00	RW	Delay time at CH1 ON (Time to add to Fix Delay started from EN1="H") **ENDLY[7:6]=00: 0μs (default)** ENDLY[7:6]=01: 600μs ENDLY[7:6]=10: 1.2ms ENDLY[7:6]=11: 2.0ms
		5:4	CH2_ENDLY	0x02	RW	Delay time at CH2 ON (Time to add to Fix Delay started from EN1="H") ENDLY[5:4]=00: 0μs ENDLY[5:4]=01: 600μs ENDLY[5:4]=10: 1.2ms **ENDLY[5:4]=11: 2.0ms (default)**
		3:2	CH3_ENDLY	0x00	RW	Delay time at CH3 ON (counting from EN2="H") **ENDLY[3:2]=00: 0μs (default)** ENDLY[3:2]=01: 600μs ENDLY[3:2]=10: 1.2ms ENDLY[3:2]=11: 2.0ms
		1:0	CH4_ENDLY	0x02	RW	Delay time at CH4 ON (counting from EN2="H") ENDLY[1:0]=00: 0μs ENDLY[1:0]=01: 600μs **ENDLY[1:0]=10: 1.2ms (default)** ENDLY[1:0]=11: 2.0ms
0x09	ENDLT_Time2	7:6	CH5_ENDLY	0x02	RW	Delay time at CH5 ON (Time to add to Fix Delay started from EN1="H") ENDLY[7:6]=00: 0μs ENDLY[7:6]=01: 600μs **ENDLY[7:6]=10: 1.2ms (default)** ENDLY[7:6]=11: 2.0ms
		5:4	CH6_ENDLY	0x02	RW	Delay time at CH6 ON (Time to add to Fix Delay started from EN1="H") ENDLY[5:4]=00: 0μs ENDLY[5:4]=01: 600μs ENDLY[5:4]=10: 1.2ms **ENDLY[5:4]=11: 2.0ms (default)**
		3:2	CH7_ENDLY	0x02	RW	Delay time at CH7 ON (counting from EN2="H") ENDLY[3:2]=00: 0μs ENDLY[3:2]=01: 600μs ENDLY[3:2]=10: 1.2ms **ENDLY[3:2]=11: 2.0ms (default)**
		1:0	Reserved	0x00	R	—
0x0A	DISENDLY_Time	7:6	CH3_DISENDLY	0x02	RW	Delay time at CH3 OFF (counting from EN2="L") DISENDLY[7:6]=00: 0μs DISENDLY[7:6]=01: 5ms **DISENDLY[7:6]=10: 10ms (default)** DISENDLY[7:6]=11: 20ms
		5:4	CH4_DISENDLY	0x00	RW	Delay time at CH4 OFF (counting from EN2="L") **DISENDLY[7:6]=00: 0μs (default)** DISENDLY[7:6]=01: 5ms DISENDLY[7:6]=10: 10ms DISENDLY[7:6]=11: 20ms
		3:2	Reserved	0x00	R	—
		1:0	CH7_DISENDLY	0x00	RW	Delay time at CH7 OFF (counting from EN2="L") **DISENDLY[7:6]=00: 0μs (default)** DISENDLY[7:6]=01: 5ms DISENDLY[7:6]=10: 10ms DISENDLY[7:6]=11: 20ms

12.4. Register description 4 (0x0B to 0x0E)

Table 12.5 0x0B to 0x0E

Address	Register name	Bit	Bit name	Default	R/W	Description
0x0B	STATUS_REG1	7:6	CH1_STATUS	0x00	R	CH1 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
		5:4	CH2_STATUS	0x00	R	CH2 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
		3:2	CH3_STATUS	0x00	R	CH3 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
		1:0	CH4_STATUS	0x00	R	CH4 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
0x0C	STATUS_REG2	7:6	CH5_STATUS	0x00	R	CH5 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
		5:4	CH6_STATUS	0x00	R	CH6 Operation state 00: Normal 01: Reserved 10: UVP 11: OVP
		3:2	CH7_STATUS	0x00	R	CH7 Operation state 00: Normal 01: Reserved 10: UVP
		1:0	Reserved	0x00	R	—
0x0D	UV_SETTING1	7:6	CH1_UV	0x01	RW	CH1 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
		5:4	CH2_UV	0x01	RW	CH2 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
		3:2	CH3_UV	0x01	RW	CH3 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
		1:0	CH4_UV	0x01	RW	CH4 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
0x0E	UV_SETTING2	7:6	CH5_UV	0x01	RW	CH5 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
		5:4	CH6_UV	0x01	RW	CH6 UVP voltage setting 00: off **01: 70% (default)** 10: 80% 11: 90%
		3:0	Reserved	0x00	R	—

12.5. Register description 5 (0x0F to 0x11)

Table 12.6 0x0F to 0x11

Address	Register name	Bit	Bit name	Default	R/W	Description
0x0F	OV_SETTING1	7:6	CH1_OV	0x02	RW	CH1 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
		5:4	CH2_OV	0x02	RW	CH2 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
		3:2	CH3_OV	0x02	RW	CH3 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
		1:0	CH4_OV	0x02	RW	CH4 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
0x10	OV_SETTING2	7:6	CH5_OV	0x02	RW	CH5 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
		5:4	CH6_OV	0x02	RW	CH6 OVP voltage setting 00: off 01: 110% **10: 120% (default)** 11: 130%
		3:0	Reserved	0x00	R	—

13. Electric characteristic

13.1. Absolute maximum ratings

Table 13.1 Absolute maximum ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Power supply pin voltage	AVCC, VIN1, VIN2,VIN3, VIN4, VIN5,VIN6 and VIN7	-0.3 to 6.0	V
Applied voltage for each pin	LX1,LX2	-0.3 to 6.0	V
	EN1,EN2,RESET,SDA,SCL	-0.3 to AVCC+0.3V	V
	Except the above	-0.3 to 6.0	V
Power dissipation	P_D (Note1,2)	3	W
Operating temperature	T_{opr}	-40 to 85	°C
Operating Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55 to 150	°C

* The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these ratings is exceeded during operation, electrical characteristics of the device may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause breakdown of and damage to and/or degradation of any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Note1: When mounting to the board (board condition:74mm×74mm×1.6mm, 4 layers, double-sided glass epoxy board)

Note2: When Ta exceeds 25°C, power dissipation decreases by the reciprocal of saturation heat resistance (1/ Rth(j-a) per 1°C.

13.2. Operation condition

Table 13.2 Operation condition

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power supply voltage	AVCC	—	4.5	4.8	5.5	V
	VIN1	—	3.6	4.8	5.5	V
	VIN2	Vout=3.3V, Iout=2A	4.3	4.8	5.5	V
		Vout=3.3V, Iout<300mA	4.0	—	5.5	V
	VIN3	—	1.630	1.983	2.057	V
	VIN4	—	1.630	1.983	2.057	V
	VIN5	—	1.95	4.85	5.50	V
	VIN6	—	3.6	4.8	5.5	V
	VIN7	—	3	—	3.6	V

13.3. Consumption current

Table 13.3 Consumption current

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Consumption current at operation (CH1/CH2 oscillation)	I_{SW}	EN1=EN2=AVCC, All channels: ON AVCC current in the test mode measurement (open loop), No-load	—	2.5	—	mA
Quiescent operation current	Iq	EN1=EN2=AVCC, All channels: ON AVCC current in the case of stopping DCDC switching	—	2.1	—	mA
Comsumption current at shutdown	Ishut	EN1=EN2=0V	—	80	—	μA

13.4. Protection function

Table 13.4 Protection function

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C).

Item	Symbol	Condition	Min	Typ.	Max	Unit
Threshold at POR rising	POR_RISING	AVCC rising	2.5	—	2.9	V
POR hysteresis voltage	POR_FALLING	AVCC falling	—	100	—	mV
Threshold at UVLO rising	UVLO_RISING	AVCC rising	3.51	3.60	3.69	V
Threshold at UVLO falling	UVLO_FALLING	AVCC falling	3.41	3.50	3.59	V
Delay time at UVLO rising	t_{R_UVLO}	—	15	30	50	μs
Delay time at UVLO falling	t_{F_UVLO}	—	5	15	30	μs
TSD detection temperature	—	—	—	150	—	ºC
TSD hysteresis temperature	—	Temperature to be returned after TSD detection	—	25	—	ºC
Threshold at Reset rising	RESET_RISING	AVCC rising	3.607	3.700	3.793	V
Threshold at Reset falling	RESET_FALLING	AVCC falling	3.51	3.60	3.69	V
Delay time at Reset rising	t_{R_RESET}	—	30	60	95	μs
Delay time at Reset falling	t_{F_RESET}	—	3	10	20	μs
UVLO detection voltage to Reset detection voltage	$V_{HYS\_UVLO\_RESET}$	—	25	100	170	mV

13.5. Logic input and output

Table 13.5 Logic input and output

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
H level voltage of EN pin input	V_{ENH}	EN1,EN2 pins	1.2	—	AVCC	V
L level voltage of EN pin input	V_{ENL}	EN1,EN2 pins	0	—	0.4	V
EN1 enable delay time	—	—	1.0	1.2	1.4	ms
EN pin input current	I_{EN}	VEN=2V	—	0	2	μA
RESET pin output current	I_{OLRST}	RESET pin voltage = 0.4V AVCC = 3V	2	—	—	mA
RESET pin leak current	I_{LKRST}	—	—	0	0.5	μA

13.6. CH1 DCDC converter (1.05V/ Iout=max_2.0A)

Table 13.6 CH1 DCDC converter (1.05V/ Iout=max_2.0A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN1	keep Vout = 1.05V	3.6	4.8	5.5	V
Consumption current (Shutdown)	—	V_{EN} = 0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable, no switching,VIN1 current	—	1	—	μA
Output voltage	Vout	Register value = default, Ta = 25°C	-1%	1.05	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	1.05	2%	V
		DCM ripple	1.029	1.050	1.071	V
Soft start time	Tss	Code=01	0.6	0.7	0.8	ms
H side ON resistance	$R_{DS(ON),H}$	VIN1=4.8V	—	120	—	mΩ
L side ON resistance	$R_{DS(ON),L}$	VIN1=4.8V	—	45	—	mΩ
Current limitation	I_{OC}	—	2.0	2.4	3.9	A
Oscillation frequency	Fsw	—	—	2.0	—	MHz
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	50	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	PWM mode	—	0.5	—	%

13.7. CH2 DCDC converter (3.3V/ Iout=max_2.0A)

Table 13.7 CH2 DCDC converter (3.3V/ Iout=max_2.0A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input Voltage	PVIN2	keep Vout = 3.3V	4.3	4.8	5.5	V
		Vout=3.3V, Iout<300mA	4.0	—	5.5	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable, no switching, VIN2 current	—	1	—	μA
Output voltage	Vout	Register value = default, Ta=25°C	-1%	3.3	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	3.3	2%	V
		DCM ripple	3.234	3.300	3.366	V
Soft start time	Tss	Code=10	0.8	0.9	1	ms
H side ON resistance	$R_{DS(ON),H}$	VIN2=4.8V	—	130	—	mΩ
L side ON resistance	$R_{DS(ON),L}$	VIN2=4.8V	—	110	—	mΩ
Current limitation	I_{OC}	—	2.0	2.4	3.9	A
Oscillation frequency	Fsw	—	—	1.5	—	MHz
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	50	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	PWM mode	—	0.5	—	%

13.8. CH3 LDO(1.15V/ Iout=max_0.5A)

Table 13.8 CH3 LDO(1.15V/ Iout=max_0.5A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN3	keep Vout=1.15V	1.630	1.983	2.057	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable	—	100	180	μA
Output voltage	Vout	Register value = default, Ta=25°C	-1%	1.15	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	1.15	2%	V
Soft start time	Tss	Code=01	0.6	0.7	0.8	ms
Voltage difference between input and output	V_{DROP}	Iout=0.5A	—	80	115	mV
Current limitation	I_{OC}	—	0.7	1.3	1.7	A
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	20	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	Iload=0 to 0.5A	—	0.5	—	%

13.9. CH4 LDO(1. 50V/ Iout=max_0.5A)

Table 13.9 CH4 LDO(1. 50V/ Iout=max_0.5A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN4	keep Vout=1.50V	1.630	1.983	2.057	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable	—	100	180	μA
Output voltage	Vout	Register value = default, Ta=25°C	-1%	1.50	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	1.50	2%	V
Soft start time	Tss	Code=10	0.8	0.9	1.0	ms
Voltage difference between input and output	V_{DROP}	Iout=0.5A	—	80	115	mV
Current limitation	I_{OC}	—	0.6	1.3	2.3	A
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	20	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	Iload=0 to 0.5A	—	0.5	—	%

13.10. CH5 LDO(1. 80V/ Iout=max_0.15A)

Table 13.10 CH5 LDO(1.80V/ Iout=max_0.15A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN5	keep Vout=1.80V	1.95	4.85	5.50	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable	—	100	180	μA
Output voltage	Vout	Register value = default, Ta=25°C	-1%	1.80	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	1.80	2%	V
Soft start time	Tss	Code=10	0.8	0.9	1.0	ms
Voltage difference between input and output	V_{DROP}	Iout=100mA	—	80	115	mV
Current limitation	I_{OC}	—	0.2	0.4	1.1	A
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	150	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	Iload=0 to 0.1A	—	0.5	—	%

13.11. CH6 LDO(3.3V/ Iout=max_0.05A)

Table 13.11 CH6 LDO(3.3V/ Iout=max_0.05A)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN6	keep Vout=3.3V	3.6	4.8	5.5	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	Enable	—	100	180	μA
Output voltage	Vout	Register value = default, Ta=25°C	-1%	3.3	1%	V
		Register value = default, Ta=-40 to 85°C	-2%	3.3	2%	V
Soft start time	Tss	Code=10	0.8	0.9	1.0	ms
Voltage difference between input and output	V_{DROP}	Iout=60mA	—	30	55	mV
Current limitation	I_{OC}	—	0.06	0.12	0.18	A
Threshold of OVP detection voltage	Vovp	OVP detect, code=10	—	120	—	%
OVP detection time	Tovpdly	—	50	100	—	μs
Threshold of UVP detection voltage	Vuvp	UVP detect, code=01	—	70	—	%
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	150	—	Ω
Line regulation	—	—	—	0.5	—	%
Load regulation	—	—	—	0.5	—	%

13.12. CH7 Load Switch(Iout=max_600mA)

Table 13.12 CH7 Load Switch(Iout=max_600mA)

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	PVIN7	—	3.0	3.3	3.6	V
Consumption current (Shutdown)	—	V_{EN}=0V	—	0	1	μA
Consumption current (Quiescent)	—	V_{EN}=2V	—	15	—	μA
Output voltage	Vout	—	—	3.3	—	V
Soft start time	Tss	Cout=15.5uF	—	500	800	μs
ON resistance	$R_{DS(ON)}$	VIN7=3.3V	—	62	100	mΩ
Current limitation	I_{OC}	—	0.60	0.75	0.90	A
Threshold of UVP detection voltage	Vuvp	—	—	2.3	—	V
UVP detection time	Tuvpdly	—	50	100	—	μs
Discharge resistance	Rdis	EN=0V	—	75	—	Ω

13.13. I^2C

DC characteristic

Table 13.13 DC characteristic

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
H level voltage of SDA and SCL pin input	V_{IHI2C}	—	1.2	—	—	V
L level voltage of SDA and SCL pin input	V_{ILI2C}	—	—	—	0.4	V
SDA output sink current	IOL	SDA Voltage=0.4V	2	—	—	mA

AC characteristic

Table 13.14 AC characteristic

(Unless otherwise specified, AVCC=4.8V, and Ta=25°C)

Item	Symbol	Condition	Min	Typ.	Max	Unit
Operation clock frequency	f_{SCL}	C_L=400pF	—	—	400	kHz
Hold time of repetitive start conditions	$t_{HD:STA}$	C_L=400pF	0.6	—	—	μs
Setup time of repetitive start conditions	$t_{SU:STA}$	C_L=400pF	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	C_L=400pF	0	—	0.9	μs
Data setup time	$t_{SU;DAT}$	C_L=400pF	100	—	—	ns
SCL signal Low period	t_{LOW}	C_L=400pF	1.3	—	—	μs
SCL signal High period	t_{HIGH}	C_L=400pF	0.6	—	—	μs
Free time of the bus between stop and start condition	tBUF	C_L=400pF	1.3	—	—	μs
Rising time of SDA signal and SCL signal.	tr	C_L=400pF	20	—	300	ns
Falling time of SDA signal and SCL signal.	tf	C_L=400pF	20	—	300	ns

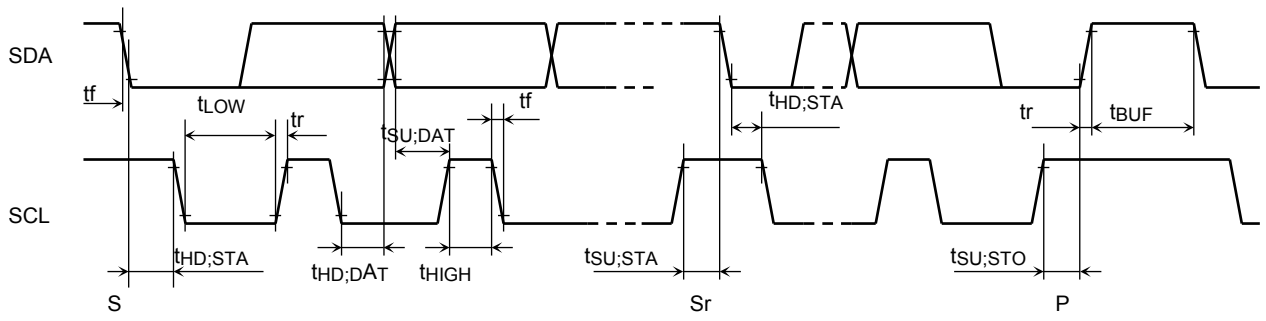
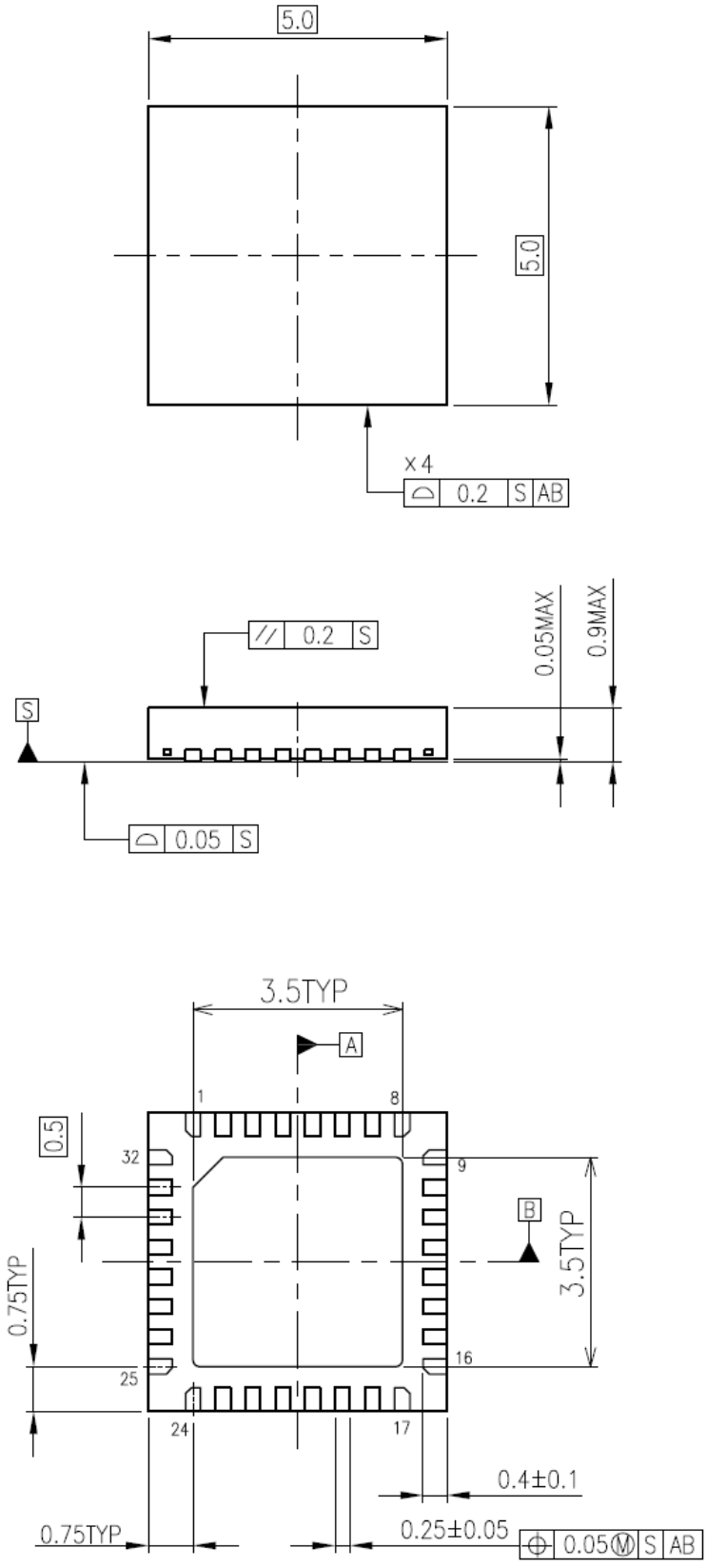


Figure 13.1 AC characteristic

14. Package dimensions

Unit: mm



Weight: 0.07g (typ.)

Figure 14.1 Package dimensions(P-VQFN32-0505-0.50-001)

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