TB6641FG/FTG
Usage considerations

Summary

The TB6641FG/FTG is a full-bridge driver IC for a DC motor providing output transistors that employ a MOS structure.

Low ON-resistance MOSFETs and a PWM control help the TB6641FG/FTG exhibit lower heat generation thus efficient motor drive.

Furthermore, the TB6641FG/FTG has two inputs, IN1 and IN2, which allow for selection of the four operation modes; forward (clockwise), reverse (counter-clockwise), short brake, and stop modes.

Contents

1. Power Supply Voltage

(1) Operating Power Supply Voltage Range

The absolute maximum voltage rating of the TB6641FG/FTG is 50 V. However, when it is actually used, the operating supply voltage range should be 10 V to 45 V.

(2) Power-ON/Power-OFF

Since a single VM is adopted as its power supply and the undervoltage lockout circuit is incorporated, the TB6641FG/FTG has no special procedures for turning on and off itself. However, unstable power supplies result in abnormal IC operations. Therefore, it is recommended to run the motor after confirming the powered VM becomes stable under the condition that both the IN1 and IN2 are in Low states.
It is likewise recommended to turn off the TB6641FG/FTG after the motor movement is completely stopped.

2. Output Current

Note that the absolute maximum output current rating of the TB6641FG/FTG varies with the VM. OUT1 and OUT2 should be kept under 4.5 A when VM is 36 V or less, and they should be kept under 4.0 A when VM is more than 36 V.
Also, the usage conditions such as the ambient temperature, presence or absence of a heatsink, board layout and IC mount technique have effect on increase and decrease of the available average output current. The TB6641FG/FTG should be used with the absolute maximum output current rating of 4.0 A, or with the average output current of 4.5 A or less when Tj is 150°C or less.

3. Control Inputs

Even if there are pulse inputs to IN1, IN2, PWM and VREF, they never seep into VM as long as when the VM power supply is turned off. Therefore the TB6641FG/FTG will never be turned on.

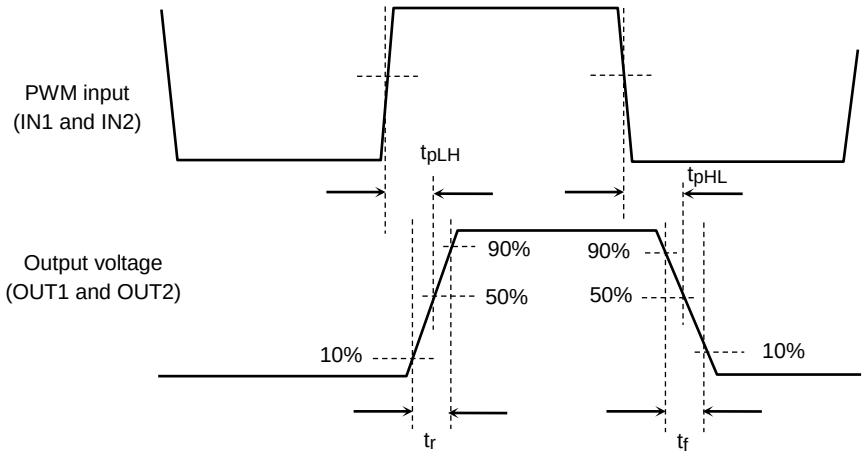
Before releasing the TSD and ISD circuits, keep driving the IN1 and IN2 Low for 1 μs or more.

4. PWM Frequency

The motor speed can be controlled by inputting the PWM signal to the PWM pin.
(The PWM control is also accomplished by inputting the PWM signal through the IN1 and IN2 pins instead of the PWM pin.)
The motor that controlled by the PWM frequency runs alternately in Normal mode and Short brake mode.
The shoot-through current is generated otherwise on overlap of the ON states of the upper and lower power transistors of the output circuit. To prevent this shoot-through current, the TB6641FG/FTG internally generates the dead time when the upper and lower power transistors switch on and off.
Therefore, the PWM control with the synchronous rectification is available without inputting the off time externally.

The operational range of the PWM frequency is stated up to 100 kHz. However, in actual operations, the output voltage will be distorted with respect to the input current even in the operation range. It is shown in the switching characteristics below.
The TB6641FG/FTG can support the frequency of even over 100 kHz only as far as its output distortions with respect to the inputs and the duty gaps are taken into account when it is used.
Note that the values of the following switching characteristics are given as typical values. The TB6641FG/FTG should be used with a sufficient safety margin because they vary with power supply voltages, temperatures, and IC variation.

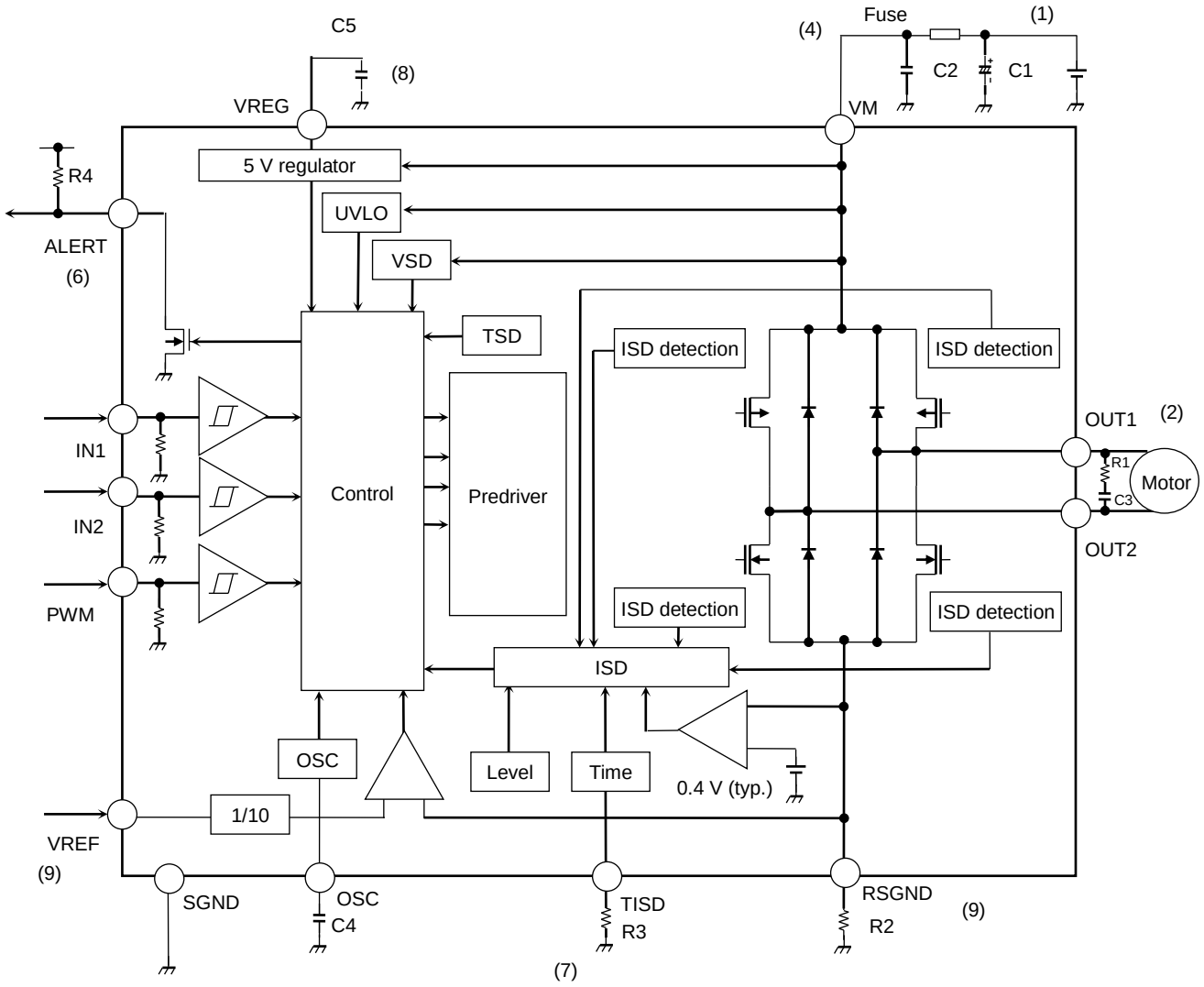
Switching Characteristics



VM = 24 V Ta = 25°C

Characteristics	Value	Unit
t_{pLH}	650 (typ.)	ns
t_{pHL}	450 (typ.)	
t_r	90 (typ.)	
t_f	130 (typ.)	

5. Application Circuit Example



(1) Capacitors Connected to the Power Supply Pin

Connect the capacitors between VM and GND as near the IC as possible.

Recommended Value

Characteristics	Symbol	Recommended Value	Remarks
VM – GND	C1	10 μF to 100 μF	Electrolytic capacitor
	C2	0.1 μF to 1 μF	Ceramic capacitor

(2) Capacitor and Resistor Between the Outputs

Connect the R1 resistor and the C3 capacitor only for removing the brush noise of the motor. In this case, limit the current by using R1 because the outputs momentarily move to the short circuit mode in conduction if C3 is not charged.

(3) Wiring of VM, OUT1, OUT2 and RSGND

The motor causes a large current flow through the TB6641FG/FTG. Therefore, sufficient space should be secured on designing the IC wiring pattern. Particularly for RSGND and SGND, a space large enough for their connections to GND should be secured so as not to be affected by wiring impedance.

(4) Fuse

For preventing a continuous flow of a large current due to overcurrent or IC damages, an appropriate fuse should be placed in the power supply of the TB6641FG/FTG.
The TB6641FG/FTG may be destroyed because of illegal use such as exceeding the absolute maximum ratings, incorrect wirings and abnormal pulse noise induced by wirings and loads. As a result, a large current continuously flows into the TB6641FG/FTG leads to smoking and ignition. To make these negative impacts as small as possible, appropriate control of the capacitance and weld time of the fuse as well as positioning of the fuse in the circuit is required.
The TB6641FG/FTG incorporates an overcurrent detection circuit (ISD). However, it does not necessarily protect the TB6641FG/FTG in any case. On activation of the ISD circuit, overcurrent conditions should be removed immediately. Depending on the usage and the use environment of the TB6641FG/FTG, like using it with the absolute maximum ratings being exceeded, the ISD circuit may not operate correctly; or the TB6641FG/FTG may be broken before the ISD circuit is activated. Even after the activation of the ISD circuit, the TB6641FG/FTG may be destroyed due to the IC heating if overcurrent continues flowing too long.
There is a concern that a secondary destruction of the IC due to continuous overcurrent may occur. Another concern is that the ISD circuit may not run due to its blank time, interacting with the output load conditions. Toshiba, therefore, describes in the specification that the ISD circuit does not necessarily run in any case as one of the usage considerations.
For instance, if a current that neither reaches the absolute maximum output current rating nor infringes the lower limit of the operating voltage of the ISD circuit continues flowing, the DMOS transistors in the output stage will be degraded. On the other hand, if once a current exceeding the absolute maximum output current rating flows into the DMOS transistors in the output stage, they are degraded as well. Therefore, even though the TB6641FG/FTG is not broken after a single overcurrent detection, it may be broken after two or three times of overcurrent detection because repeated detections will deepen the DMOS degradation.

Toshiba recommends the use of a fuse in the power supply to cope with such a secondary destruction.

(5) FIN

FIN has a role of heat radiation. Therefore, design the pattern in consideration of the heat design.
(FIN is electrically connected to the back side of the chip; thus should be insulated or shorted to GND.)

(6) ALERT Pin

The ALERT pin behaves as an open-drain output. It has a pull-up resistor in an external power source to output high level. When the low level is outputted to the ALERT pin, the TB6641FG/FTG operates normally. When the high level is outputted to the ALERT pin (High-impedance), the TB6641FG/FTG operates with some failures (UVLO, TSD, VSD and/or ISD is running).
It is recommended to use a pull-up resistor of 10 kΩ to 100 kΩ.

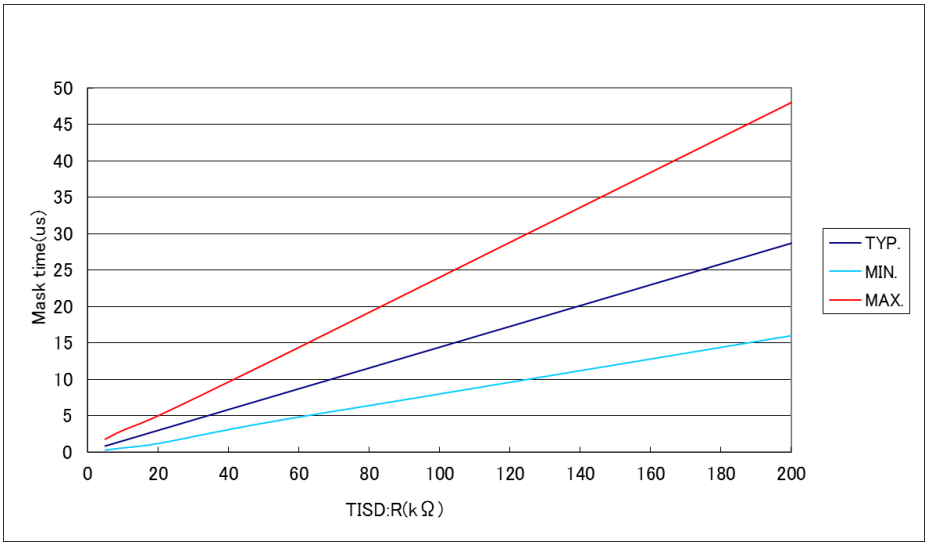
(7) Resistor set for TISD pin

One ISD detection feature is provided for each of the four output power transistors.
Detection current is programmed 7 A (typ.) (4.5 A to 10 A) internally. If any one of the four ISD detection runs over the ISD detection time (mask time), it turns off all the output power transistors (puts them in High-impedance state).
The external resistor of the TISD pin configures the ISD detection time (mask time).
The normal operation returns by setting both the IN1 and IN2 pins Low and releasing the ISD detection.

The change of the ISD mask time with respect to the external resistor values of the TISD pin is shown in the following figure.
The mask time through the TISD pin should be controlled as follows;
Longer than the time of preventing incorrect operations of the TB6641FG/FTG due to noises
Shorter than the time of preventing the IC destruction during overcurrent detection

The resistor provided for the TISD pin should be 5 kΩ or more. However, in disabling the overcurrent detection function, please connect the TISD pin to GND.

ISD behavior on load shorts
Irrespective of usage of the constant current PWM control (i.e. a detection resistor is connected between the RSGND and the SGND pins), pay attention that if wiring impedance exists between the RSGND and the SGND pins, the ISD function may not work even on a load short because the constant current PWM control operates before running of the ISD circuit.



Relation of external resistance of TISD pin and ISD mask time (for reference only)

Note: Please set the external resistor in the range of 5 kΩ to 200 kΩ.

Note: The complementary output circuit consists of N-channel and P-channel DMOS transistors, thus the ISD current thresholds show slight differences.

(8) Capacitor for VREG pin

Please connect the capacitors between VREG and GND as near the IC as possible.

Recommended Values

Characteristics	Symbol	Recommended Value	Remarks
VRE-GND	C5	100 pF to 0.01 μF	Ceramic capacitor

(9) Calculations for Constant Current PWM Control of the RSGND and VREF Pins

As for the configuration of the constant current PWM control, the peak current in the constant current operation is determined by inputting voltage to the VREF pin. The peak current value is calculated by the following equation:

I_O = VREF/R2 × 1/10 [A] For example, when R2 = 0.2 Ω, and VREF = 2 V, I_O = 1 A

The constant current PWM frequency is also configurable by controlling the capacitor of the OSC pin. The oscillation frequency is approximated by the following equation:

fosc [Hz] (typ.) = 0.42/ (Cosc [F] × 10^3) For example, when C4; Cosc = 1800 pF, then fosc = 233 kHz

The OSC frequency should be configured to 500 kHz or less. If it is configured to higher than 500 kHz, the switching loss of the output stages controlled by the PWM drive becomes larger. Note, however, that if the OSC frequency is too low, the PWM frequency may fall within the audible range.

Sufficient safety margin should be secured because the PWM frequency varies with the power supply voltage, temperature, and IC variation.

The RSGND pin turns off all the output transistors (puts them in high-impedance state) when the voltage exceeds 0.4 V (typ.) in order to prevent overvoltage which occurs in connecting to the detection resistor. It is the same control as that of the ISD circuit. At this time, also the ALERT pin is driven high. To return the operation of the TB6641FG/FTG to the normal mode, the overvoltage detection should be released by setting both the IN1 and IN2 pins low.

As for the RSGND pin, it is recommended to use an overvoltage detection resistor of 0.1 Ω or more.

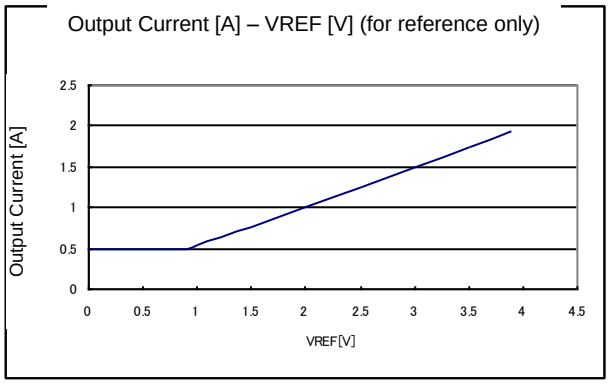
The voltage across the detection resistor will be compared to the reference voltage across the SGND pin. Therefore, the overvoltage detection resistor of the RSGND should be assigned near the RSGND pin and SGND pin but not to be affected by wiring impedance.

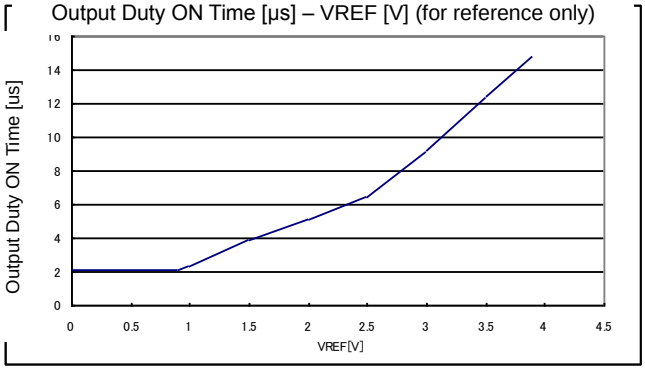
When the constant current PWM control is not used, the RSGND pin should be shorted to the SGND pin instead of connected to the R2 resistor.

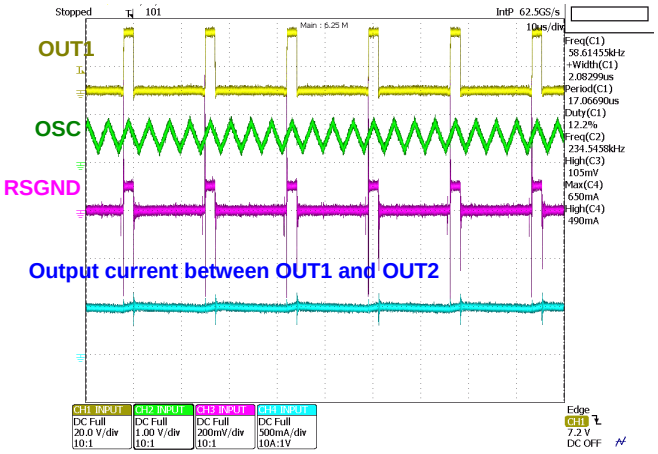
In this case, sufficient space should be secured between the RSGND pin and the SGND pin; otherwise wiring impedance generated between these pins will work like a detection resistor. As a result, the motor moves as if its speed is controlled by a constant current PWM frequency. Moreover, the OSC pin should be connected to the capacitor or short-circuited to GND.

The characteristics curves of the output current and the output duty ON time with respect to VREF respectively are shown below. And their active waveforms are also shown below.

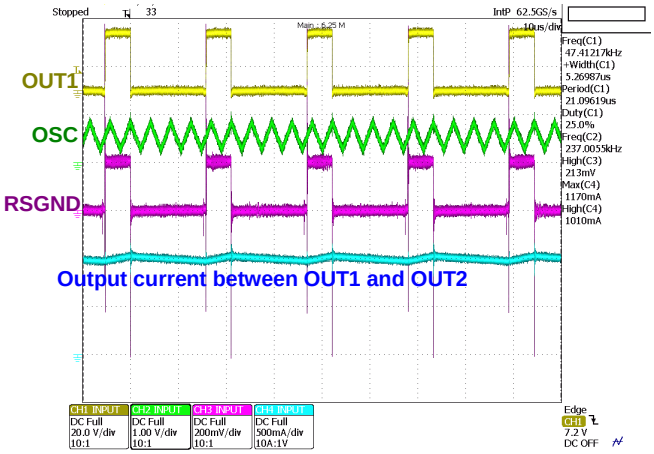
To prevent the malfunctions due to noise, the duty ON time of about 2 μs is provided by default. Note that the offset current is provided at the output. Amount of off sets of the output current vary with loads. As for the load conditions shown below (a resistor and a load of 5Ω + 2 mH), the nominal offset is 0.5 A or so.







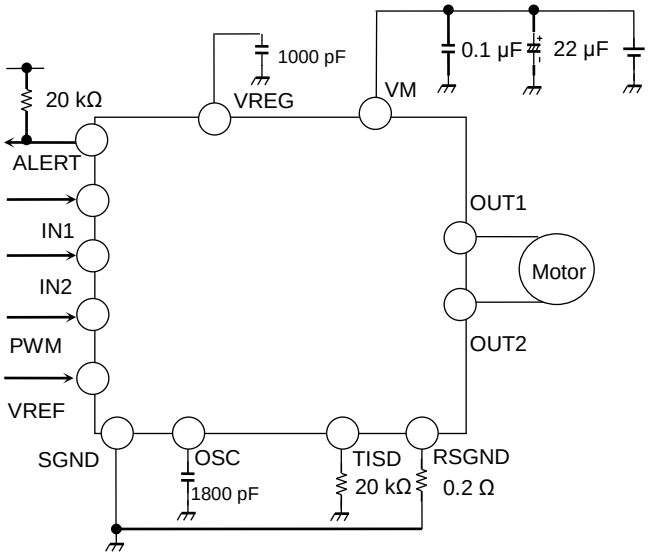
Reference waveforms when VREF = 0 V



Reference waveforms when VREF = 2.0 V

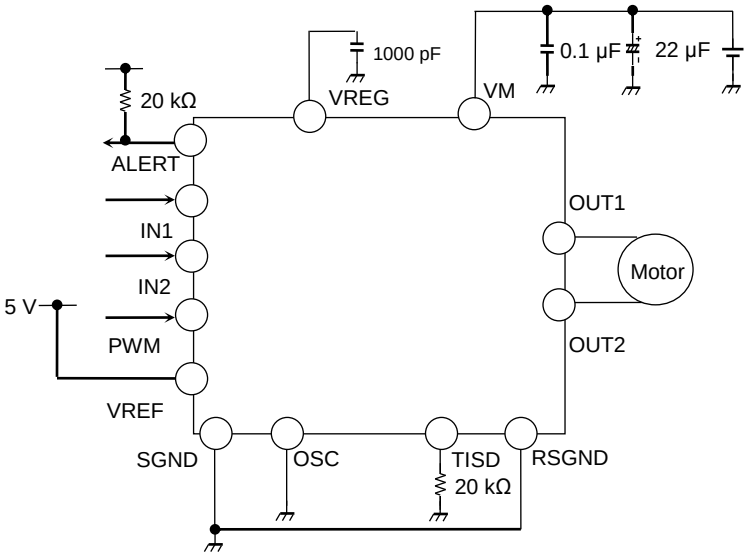
Conditions: VM = 24 V, OSC = 1800 pF, RSGND; 0.2 Ω, IN1 = H, IN2 = L, VREF = any value, Loads; 5 Ω + 2 mH

(a) Application Circuit Example in case of using Constant Current PWM Control



(b) Application Circuit Example in case of NOT using Constant Current PWM Control

The RSGND pin should be shorted to the SGND pin, and the VREF pin should be pulled high (5 V).



6. Power Dissipation

The power loss of the TB6641FG/FTG can be roughly estimated by the following equations:

(1) When PWM Duty = 100%

$P = VM \times I_{CC} + I_O^2 \times R_{ON} (U + L)$

For example, when VM = 24 V and the output current, I_O = 0.5 A (For I_{CC} and R_{ON} (U + L), refer to the electrical characteristics on the data sheet.)
P (typ.) = 24 V × 2.5 mA (typ.) + $(0.5\ A)^2$ × 0.55 Ω (typ.) = 0.1975 W
P (max) = 24 V × 8 mA (max) + $(0.5\ A)^2$ × 0.9 Ω (max) = 0.417 W

(2) When the PWM control is active

The power dissipation in case of using the PWM control can be roughly calculated as follows:
(Switching loss occurring actually is not considered.)
$P = \{VM \times I_{CC} + I_O^2 \times R_{ON} (U + L)\} \times$ PWM duty

7. Calculation of Heat Generation

Mutual relation of the ambient temperature, Ta, and the junction temperature, Tj, is roughly estimated by the following equation:

$T_j = P \times R_{th\ (j\text{-}a)} + Ta$

*: $R_{th\ (j\text{-}a)}$: Heat resistance between the junction and ambient temperatures

*: Ta: Ambient temperature (Stable ambient temperature avoiding the affect of any heat generation)

For example, when VM = 24 V, output current (I_O) = 0.5 A, Ta = 85 °C, and P (max) = 0.417 W,

(1) In mounted on the board of HSOP16-P-300-1.00 (please refer to the following graph)
When $R_{th\ (j\text{-}a)}$ = 89.3 °C/W (board size: 60 mm × 30 mm× 1.6 mm),
T_j = 0.417 W × 89.3 °C/W + 85 °C = 122.2 °C

The transient thermal resistance (Rth (j-a)) for 1 s is approximately 16 °C/W. When Ta = 85 °C and P = 0.417 W,

Tj = 0.417 W× 16 °C/W + 85 °C = 91.7 °C

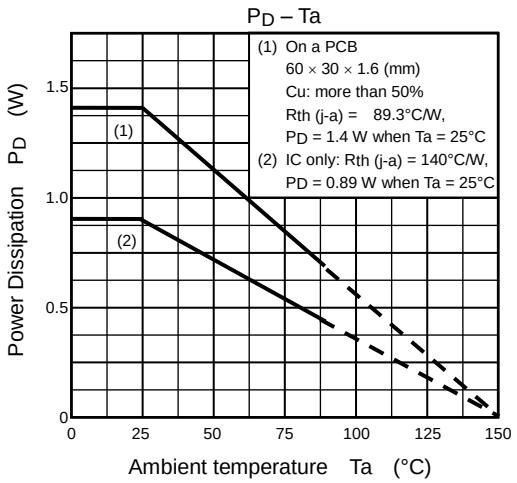
(2) In mounted on the board of P-VQFN32-0505-0.50-002 (please refer to the following graph)
When $R_{th\ (j\text{-}a)}$ = 35.2 °C/W (based on JEDEC standard, 4-layer board, sized 76.2 mm × 114.3 mm × 1.6 mm),
T_j = 0.417 W × 35.2 °C/W + 85 °C = 99.7 °C

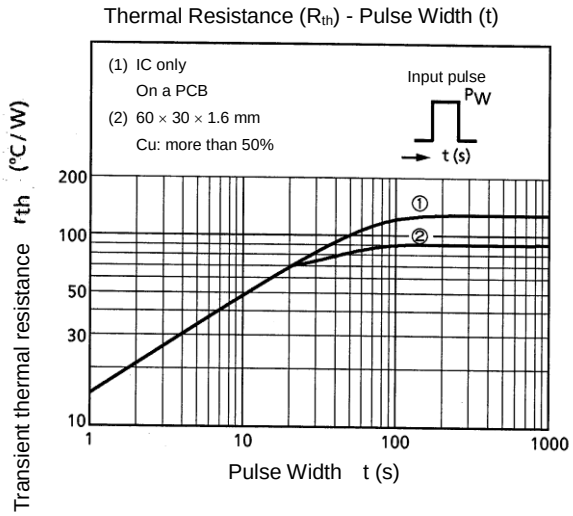
Moreover, the transient thermal resistance (Rth (j-a)) for 1 s is approximately 12 °C/W. When Ta = 85 °C and P = 0.417 W,

Tj = 0.417 W × 12 °C/W + 85 °C = 90 °C.

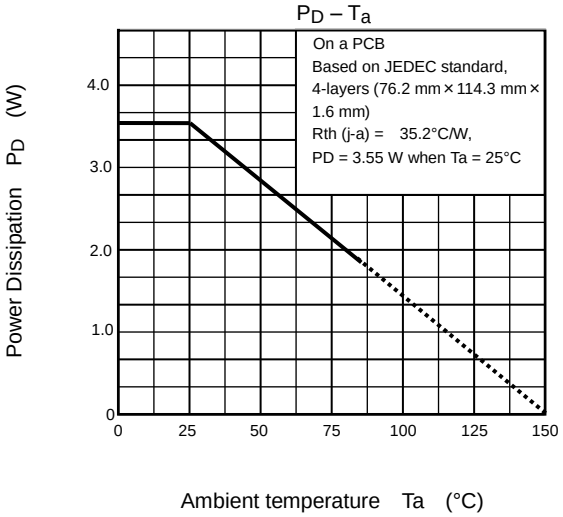
Care must be taken for Rth (j-a) which is dependent on use conditions such as a board mount method. Higher the ambient temperature is, smaller will be the power dissipation.
Note that the equations described here are only the ways to find out rough estimation. A sufficient evaluation of the TB6641FG/FTG with the junction temperature less than 150°C is required for using the TB6641FG/FTG with a full safety margin.

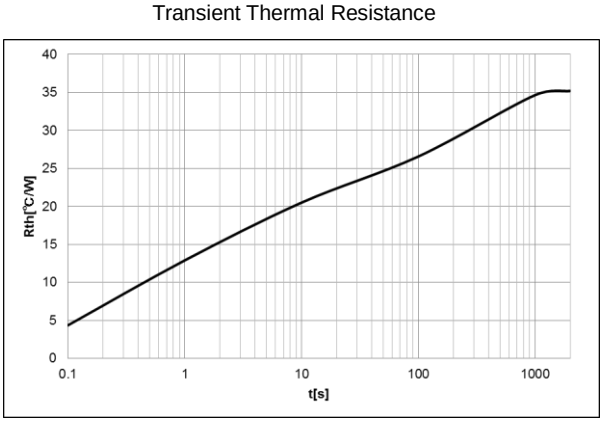
HSOP16-P-300-1.00





P-VQFN32-0505-0.50-002

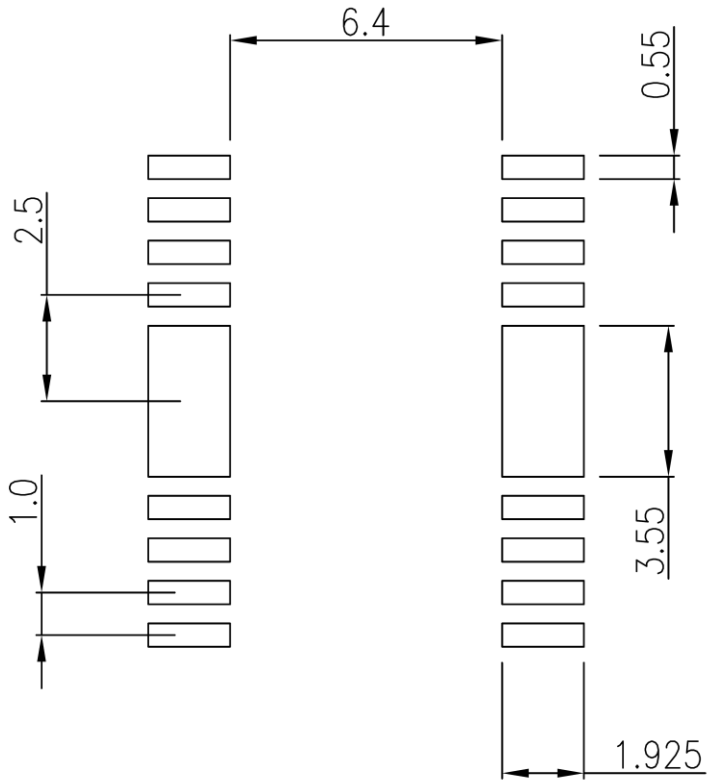




8. Land Pattern Example (for reference only)

HSOP16-P-300-1.00

Unit: mm



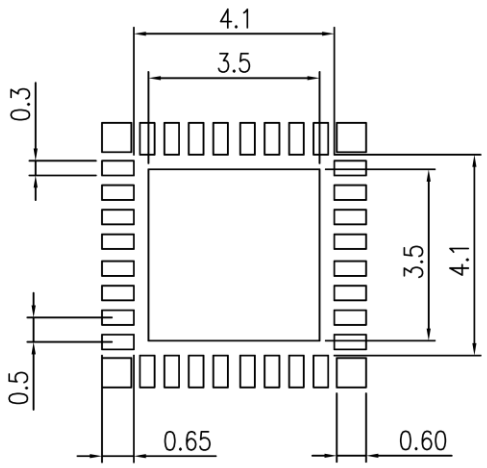
Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only.
  TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

Note: Design the pattern in consideration of the heat design because the fin has the role of heat radiation. (The back side should be insulated or connected to GND because it is connected to the back of the chip electrically.)

Land Pattern Example

P-VQFN32-0505-0.50-002 Unit: mm



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Note 1: Design the pattern in consideration of the heat design because the exposed metal portion of the back side has the role of heat radiation.
(The exposed metal portion of the back side should be insulated or connected to GND because it is connected to the back of the chip electrically.)

Note 2: Though each OUT1, RSGND, OUT2, VM, and SGND has two pins, short out these two pins in the external IC respectively.

Notes on Contents

(1) Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

(2) Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

(3) Timing Charts

Timing charts may be simplified for explanatory purposes.

(4) Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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(5) Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (TJ) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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