TB6631FNG
Usage considerations

Summary

TB6631FNG is a 3-phase full-wave sine-wave PWM brushless motor controller. Auto lead angle function that is controlled by feed backing of the rotation number is incorporated. It is for fan motors of home appliances.

This is a reference.
Please do not determine the final equipment design by this material.

Contents

Figure contents

Table contents

1. Power supply voltage

1.1. Absolute maximum ratings and usage range

Power supply voltage of VCC terminal has two standards; the absolute maximum ratings and the usage range. The absolute maximum ratings of the power supply voltage must not be exceeded even for a moment. Please use the IC within the usage range.

Table 1.1 Absolute maximum ratings of power supply voltage (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	18	V

Table 1.2 Power supply voltage usage range (Ta = 25°C)

Characteristic	Symbol	Voltage range	Unit
Power supply voltage	V_{CC}	7 to 16.5	V

1.2. Sequence of power supply

In applying Vcc or turning off the power, the IC operation may be unstable depending on the input conditions. To avoid malfunction of the motor, please obey the following sequence.

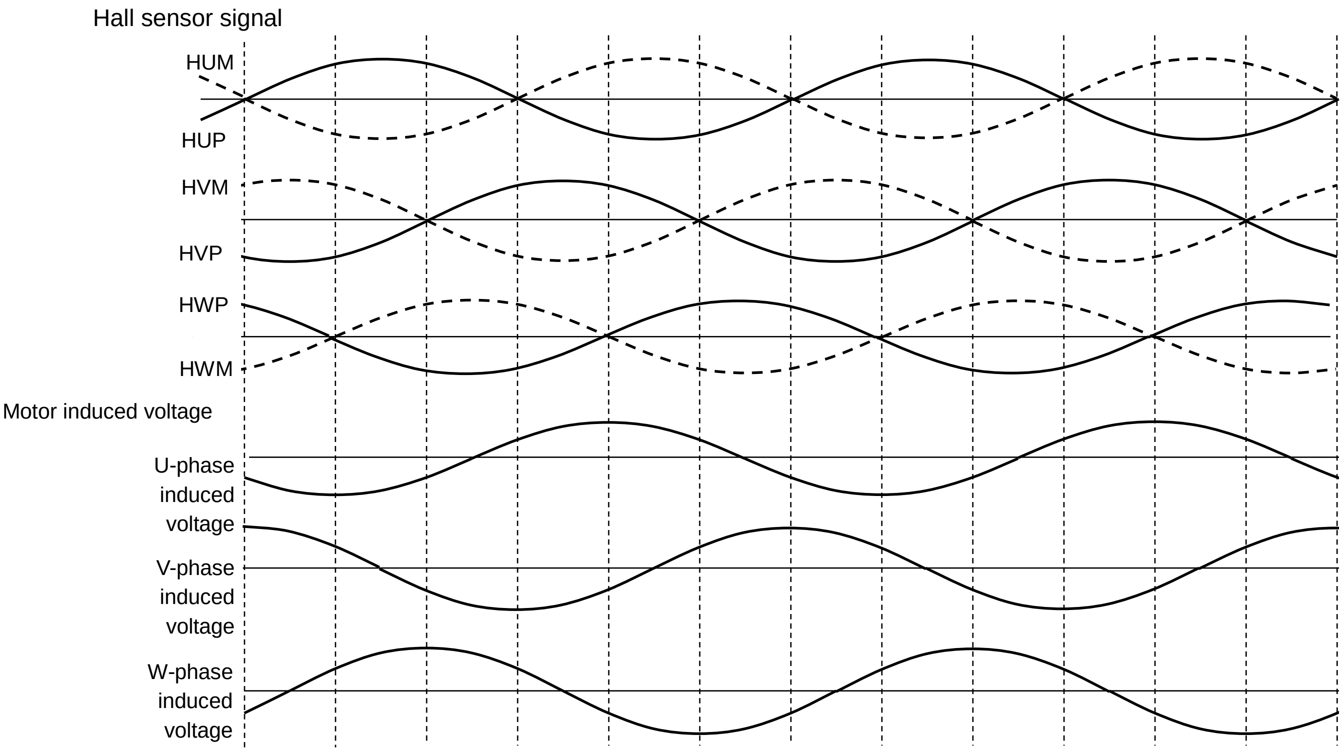
1. Sequence of applying Vcc
   In applying Vcc, connect Vsp to GND or set open. In case terminals of CW/CCW, RES, LA, UL, IDC, and TEST2 are controlled by signals of external IC, connect them to GND or set open. Then, after applying power supply of VCC, please set each terminal to change the input voltage if needed.

2. Sequence of power shut down (Vcc)
   Please turn off the power supply of Vcc after Vsp is configured 0 V. In case terminals of CW/CCW, RES, LA, UL, IDC, and TEST2 are controlled by signals of external IC, connect each terminal to GND or set open before Vcc is shutdown.

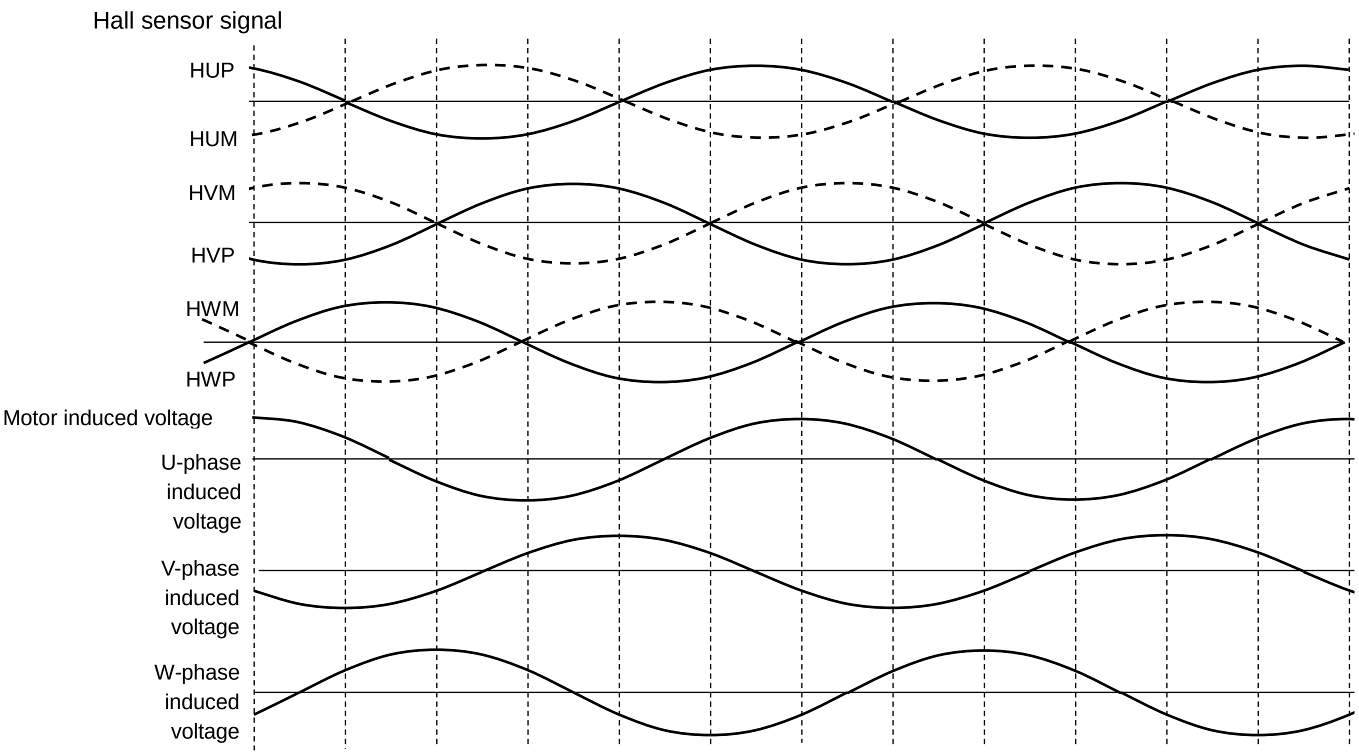
2. Notes in using the motor

Please use the motor whose phase relation between hall sensors and induced voltage corresponds to the following timing chart.

Forward rotation (CW/CCW = L)



Reverse rotation (CW/CCW = H)



3. Application circuit example

<In case of adopting a power device which incorporates a gate driver>

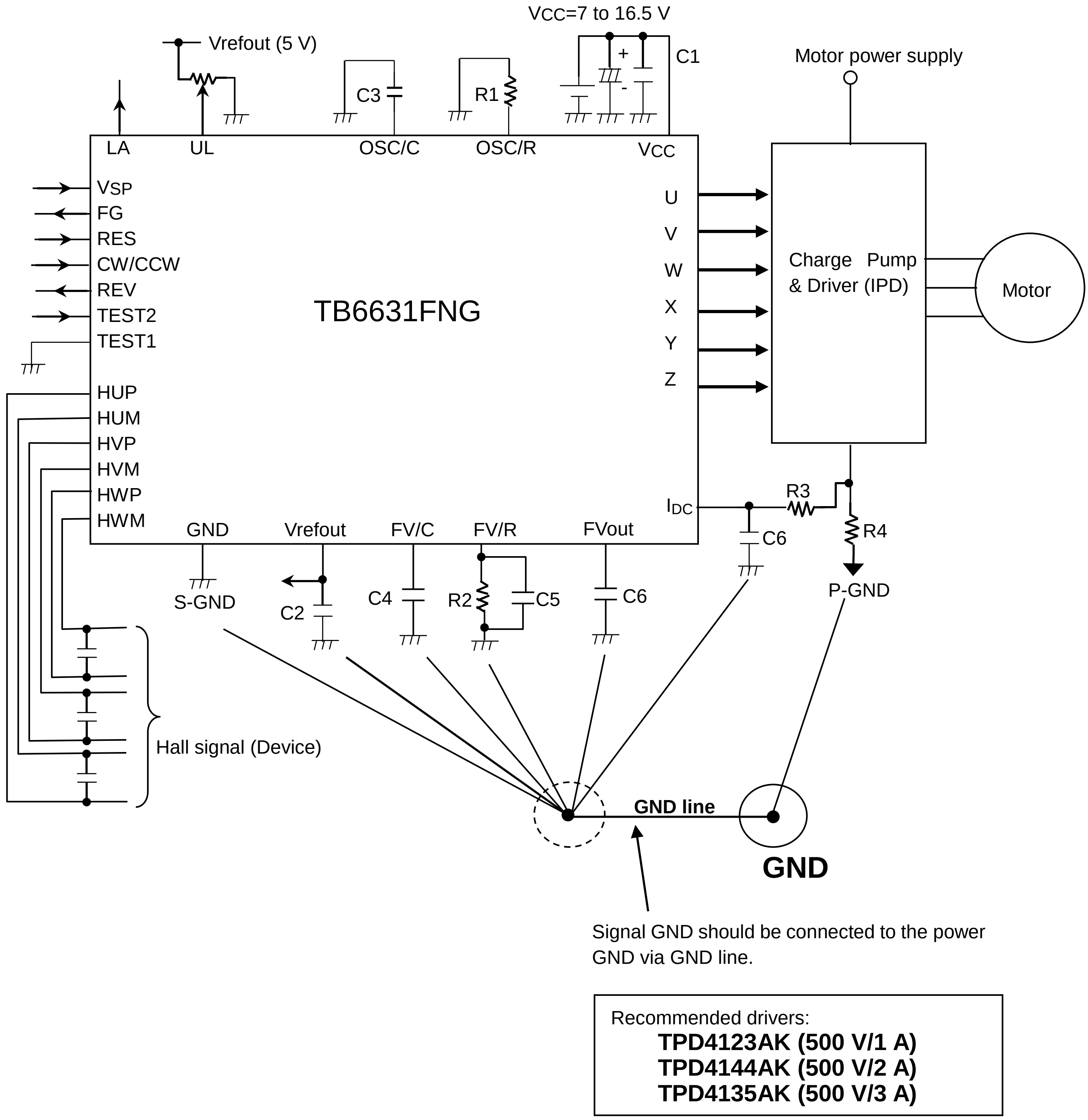


Figure 3.1 Application circuit example

<In case of adopting discrete devices>

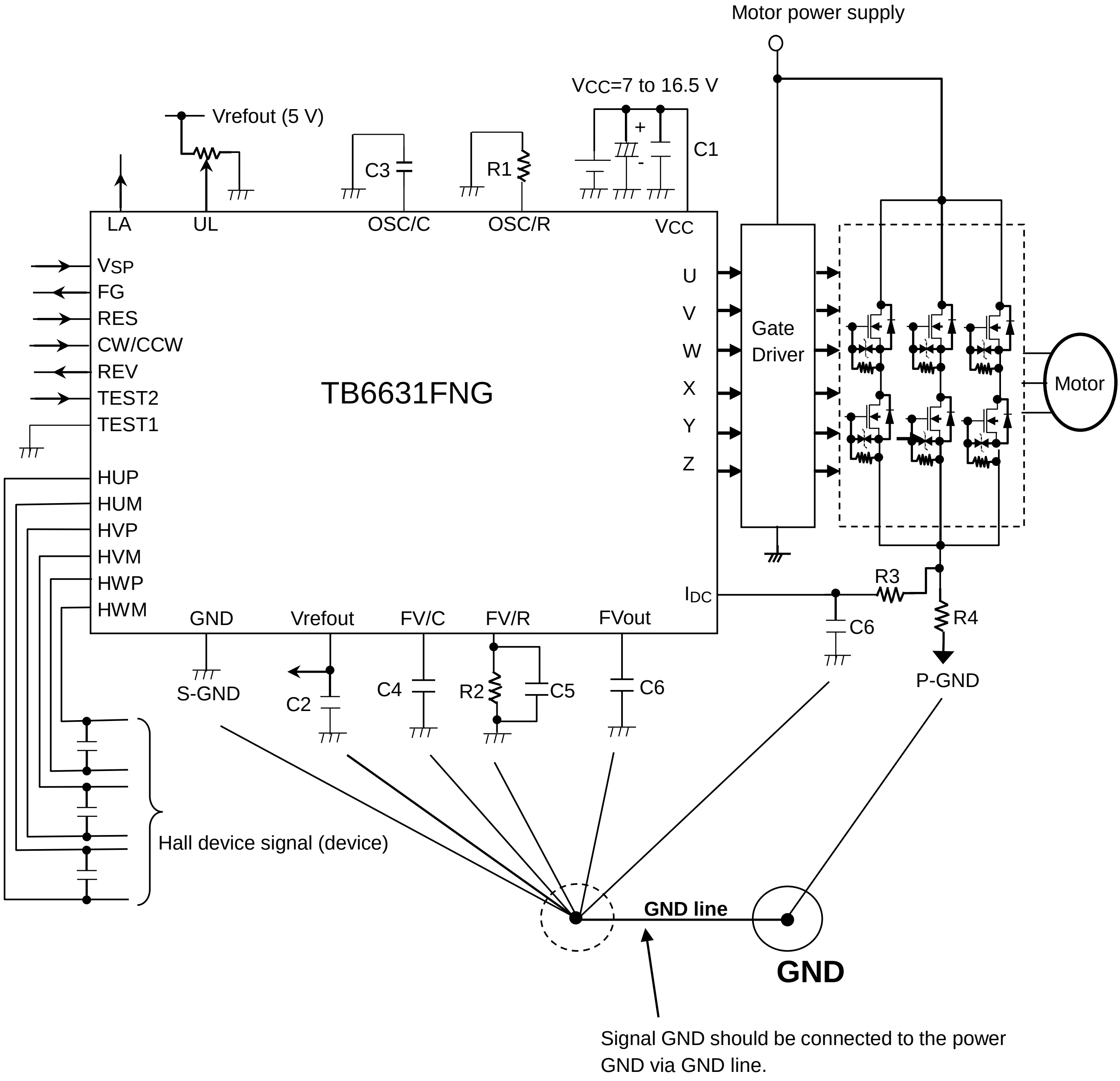


Figure 3.2 Application circuit example

(1) Capacitor for Vcc terminal

Connect the ceramic capacitor and the electrolytic capacitor between Vcc and GND as close to the IC as possible if needed in order to reduce the noise and the fluctuation of the voltage at Vcc terminal. In particular, the power supply fluctuations and the noise, which generate at high frequency, can be effectively reduced by connecting ceramic capacitors near the IC.

Table 3.1　Capacitor for Vcc terminal

Item	Component	Recommended value
Between Vcc and GND: C1	Electrolytic capacitor	10 μF to 33 μF
	Ceramic capacitor	0.1 μF to 0.22 μF

(2) Capacitor for Vrefout terminal

The Vrefout terminal supplies power to the hall elements and the hall IC, and configures terminals. In this case, the output current of Vrefout terminal should be 30 mA or less.
Please connect the capacitor between Vrefout and GND as close to the IC as possible in order to reduce the noise and the fluctuation of the voltage at the Vrefout terminal.

Table 3.2　Capacitor for Vrefout terminal

Item	Component	Recommended value
Between Vrefout and GND: C2	Ceramic capacitor	0.22 μF to 1 μF

(3) OSC/R and OSC/C terminals

OSC/R and OSC/C terminals set reference oscillating frequency.
Connect the resistor (R1) between OSC/R terminal and GND and connect the capacitor (C3) between OSC/C terminal and GND not to be influenced by noise and wiring impedance. They should be connected as close to the IC as possible. The typical value of the oscillation frequency (fosc) can be gained from below approximate equation. Components of R1 and C3 are recommended to be applied under the conditions of the following table3-3.

fosc = 15.11 / CR

C3 = External capacitor (330 pF)

R1 = External resistor (9.1 kΩ or 10 kΩ)

Table 3.3　Carrier frequency

Item	Conditions	Operation range
Carrier frequency	C3 = 330 pF, R1 = 9.1 kΩ	18 kHz to 22 kHz
	C3 = 330 pF, R1 = 10 kΩ	16.2 kHz to 19.8 kHz

Moreover, the carrier frequency (FC) and the off time of upper and lower output (TOFF) are calculated from below formulas.

FC = fosc / 252

T_{OFF} = 9 / fosc

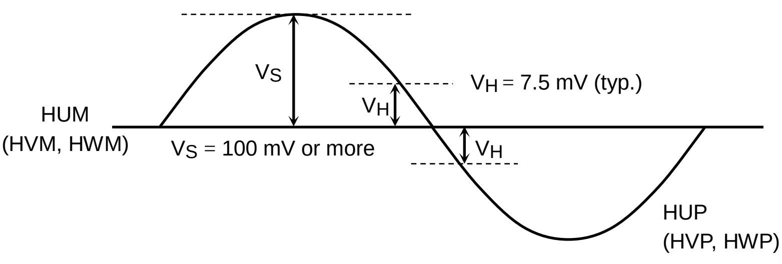
In sine-wave drive, the operation is controlled by synchronous rectifier. The off time (TOFF) of upper phase (U, V, and W) and lower phase (X, Y, and Z) is about 2 μs (when TOFF = 9 / fosc and fosc = 4.5 MHz). Therefore, pay attention to the off time of the used power IC, the switching speed of the gate driver, and that of the discrete device. When the response time delays, the penetrating current may be generated and the IC might be destroyed because upper and lower phases of the output step turn on at the same time.

(4) HUP, HUM, HVP, HVM, HWP, HWM terminals

Input hall signals to HUP, HUM, HVP, HVM, HWP, and HWM terminals. Select hall elements or hall ICs to provide hall signals. Connect output terminals of U, V, and W, and the hall signal terminals of HUP, HUM, HVP, HVM, HWP, and HWM, to the motor to have the relation shown in the timing chart of “2. Notes in using the motor”.

<Notes in using the hall elements>

- If 5 V is supplied from the Vrefout power supply to the hall elements, add the limiting resistor to the power supply terminal of the hall element in order not to exceed the maximum input current of the hall element.
- To recognize switching of the hall signal correctly, the amplitude of the hall elements should be 100 mV or more and the input voltage range should be 1.5 V to 3.5 V.
- Hall amplifier has a hysteresis. When the amplitude of the hall amplifier is small, the phase gap of the switching timing becomes large. So, please set the amplitude of the amplifier as large as possible.
- When the capacitor for reducing the noise of the hall signal is attached, please arrange it close to HUP and HUM terminals, HVP and HVM terminals, and HWP and HWM terminals for each. The recommended capacitor is 0.001 μF to 0.1 μF.

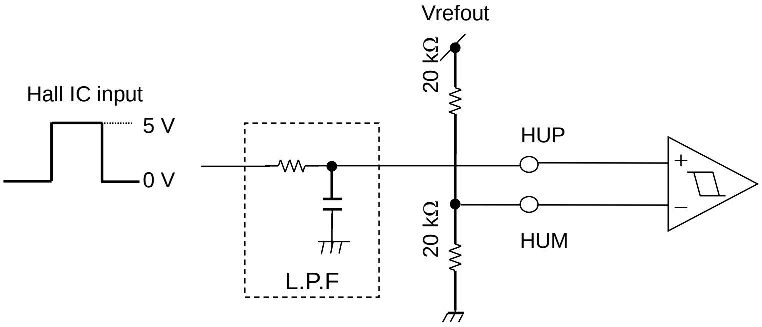


< Notes in using the hall IC>

Please configure HUP, HVP, HWP, HUM, HVM, and HWM as follows. It is recommended to adopt low-pass filter between the input terminal and GND to reduce the noise. However, in this case, delay time of the input signal should be considered.

(1) HUP, HVP, and HWP: Input voltage: H level = Vrefout, L level = GND
HUM, HVM, and HWM: Input voltage: Vrefout/2 * Configure it with resistive dividing voltage between Vrefout terminal and GND.

(2) HUP, HVP, and HWP: Input voltage: Vrefout/2 * Configure it with resistive dividing voltage between Vrefout terminal and GND.
HUM, HVM, and HWM: Input voltage: H level = Vrefout, L level = GND



*) In case of V phase and W phase are also the same.

(5) I_{DC} terminal

I_{DC} terminal provides the current limit function. This function is available when the output current is detected by the current detection resistor (R4).
The conduction signal outputs low when the voltage of the I_{DC} terminal is 0.5 V (typ.) or more.
The current limit protection is released at every carrier frequency.

Current limit threshold = 0.5 V / R4

Example: When R4 = 0.5 Ω, current limit threshold = 0.5 V / 0.5 Ω = 1.0 A

Internal IC of Idc terminal incorporates the digital filter of 1 μs (typ.) and the analog filter of 1 μs (typ.). It is influenced by the noise generated in the power system when the current detection resistor is connected. When malfunction, which turns off the driving output, occurs because of the noise, please connect the low-pass filter (CR) externally. Select the appropriate constant number of the CR filter to gain the relation that the cut off frequency (fcut) is 10 times or more of the carrier frequency (Fc). The capacitor for the filter should be connected as close to the IC as possible. In this time, please connect the GND-line of the capacitor to the S-GND.

Cut off frequency (fcut) = 1/ (2πCR) [Hz]

When Carrier frequency (Fc) = 20 kHz and fcut > 10 × Fc, CR < 7.96×10^{-7}

For example, configure R = 5.1 kΩ and C = 100 pF, and confirm the operation.

(6) CW/CCW terminal

In using this terminal by fixing the voltage of the terminal, connect the CW/CCW terminal to Vrefout or GND. In connecting to Vrefout, it becomes high level. In connecting to S-GND, it becomes low level.
To switch the logic of the CW/CCW terminal by inputting the external control signal, configure the Vsp terminal 0.7 V or less. Then, change the input signal level after the output of the conduction signal is turned off. Please start the motor operation by setting Vsp after switching the input signal. When the logic of the CW/CCW is switched under the condition that the conduction signal is outputting, off time of upper and lower output is reduced. Therefore, the penetrating current may be generated and the IC may be destroyed because upper and lower phases of the output step are turned on at the same time. So, please pay attention to deal with this terminal.

(7) Vsp terminal

Motor operation including rotating speed can be controlled by inputting command signal of the output ON duty to Vsp terminal. Please input analog voltage as a command signal. Moreover, when rotation speed needs to be controlled, please connect Vsp and FG terminals to the device such as MCU and feedback the speed.
When the motor operation changes from the normal mode to the stop or the low-rotation mode, the motor back-EMF may occur and the current might be regenerated to the motor power supply. Therefore, there is a possibility to boost the power supply voltage. So, pay attention in changing the motor speed from high to low or turning off the operation. To avoid destroying the power device by boosting voltage, please slow down the speed carefully by confirming the operation state through the experiment.

(8) FG terminal

Push-pull circuit of 5 V output is constructed. When rotation speed needs to be controlled, input FG signal to MCU to use this signal as the information of the motor rotating number.

(9) TEST1 terminal

It is a terminal for shipping test of the IC. Be sure to set it to a low level. It is recommended to connect TEST1 terminal to GND. It incorporates the pull-down resistor. However, in setting it open, it is concerned that the terminal voltage rises rapidly influenced by board wirings. In setting it open unavoidably, please confirm that IC terminal voltage is 0.8 V or less.

(10) TEST2 terminal

The timings of the modulated-wave generation and the reset are determined by the TEST2 terminal. In case of fixing the voltage of this terminal, please connect it to Vrefout or S-GND. (Connecting to Vrefout:" H", Connecting to GND: "L")

(11) RES terminal

When the input signal is configured high level, the conduction signal outputs low. And when the RES terminal is configured low level or open, the motor operates again. When the abnormality is detected externally, the motor operation is stopped or controlled slowdown by inputting the signal to the RES terminal. Moreover, when the RES terminal is set high level, charging of the boost strap capacitor is stopped. Thus, it is not charged in recovering the operation.

Table 3.4 Operation of RES terminal

RES	Conduction signal output (U, V, W, X, Y, and Z)
High	Low
Low or Open	Motor operation is available

(12) REV terminal

Push-pull circuit of 5 V output is constructed. It detects the direction of the motor rotation. When the configuration of the CW/CCW terminal and the actual rotation direction of the motor are not corresponded, the REV terminal outputs high level. When the operation is 180° commutation mode (hall input = 1 Hz or more), it outputs low level. The abnormality of the rotation direction can be detected by connecting it to the device such as MCU.

Table 3.5 Operation of REV terminal

CW/CCW	Actual motor rotation direction	REV
Low (CW)	CW (forward rotation)	Low
	CCW (reverse rotation)	High
High (CCW)	CW (forward rotation)	High
	CCW (reverse rotation)	Low

(13) U, V, W, X, Y, and Z terminals

Push-pull circuit of 5 V output is constructed to output conduction signals. Please connect them to the inputs of the power system such as the power IC and the gate driver IC.

(14) UL terminal

The UL terminal can configure the upper threshold of the lead angle. It can limit the lead angle, which is set by the LA terminal, in the range of 0 to 5 V.

(14) GND

Connect the GND terminal to the signal-GND line (S-GND). Design the GND pattern to avoid the influence of the power-GND of the motor. As for the connection example, please refer to the application circuit example in the figure 3.1 and figure 3.2.

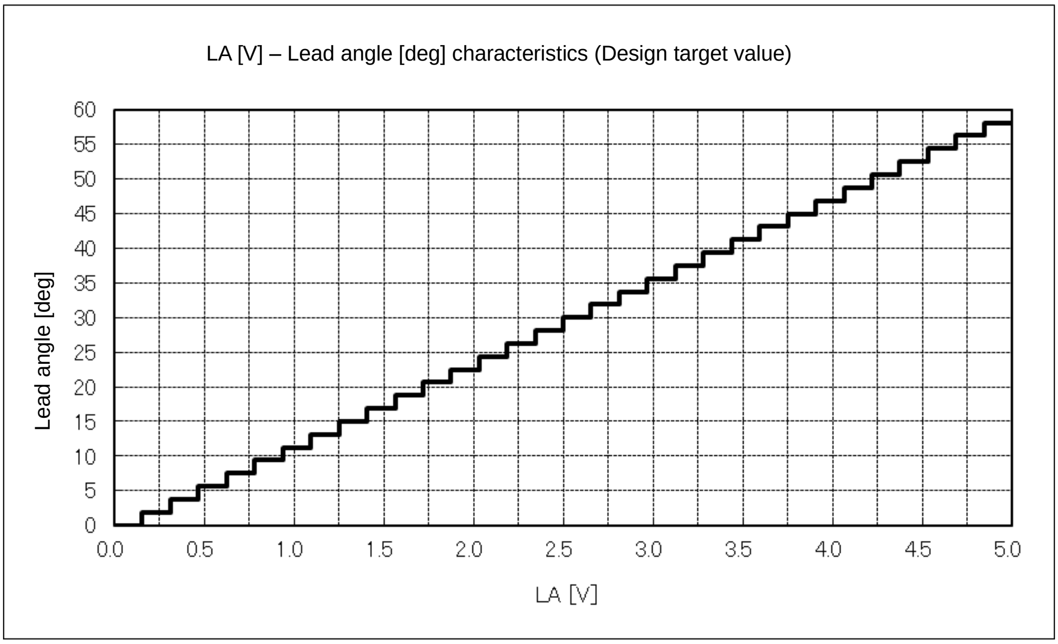
4. Lead angle control

The lead angle of the conduction signal according to the induced voltage can be adjusted by the input voltage of LA terminal. The range of the lead angle is 0 to 58 °. Lead angle control has two modes; the auto lead angle control mode and the external input lead angle control mode. As for the auto lead angle control, the lead angle is determined by changing the LA voltage automatically according to the FG frequency. As for the external lead angle control, the lead angle is determined according to the input voltage of the LA terminal.
The efficiency of the motor operation can be improved by adjusting the lead angle. The most appropriate lead angle depends on the applied motor. So, please determine the lead angle by evaluating with the actual motor. In adjusting the motor characteristics with the lead angle, change the lead angle by LA terminal and compare the motor current or efficiency. Please adjust the voltage of LA terminal by comparing the motor current or the efficiency. When the motor current or the efficiency has the smallest value in the same rotation speed before or after lead angle change, the LA voltage is the most appropriate value.

Table 4.1 Relation of LA voltage and lead angle

(Value is design target)

Step	LA [V]	Lead angle [deg]	Step	LA [V]	Lead angle [deg]	Step	LA [V]	Lead angle [deg]
0	0.000	0.000	11	1.719	20.625	22	3.438	41.250
1	0.156	1.875	12	1.875	22.500	23	3.594	43.125
2	0.313	3.750	13	2.031	24.375	24	3.750	45.000
3	0.469	5.625	14	2.188	26.250	25	3.906	46.875
4	0.625	7.500	15	2.344	28.125	26	4.063	48.750
5	0.781	9.375	16	2.500	30.000	27	4.219	50.625
6	0.938	11.250	17	2.656	31.875	28	4.375	52.500
7	1.094	13.125	18	2.813	33.750	29	4.531	54.375
8	1.250	15.000	19	2.969	35.625	30	4.688	56.250
9	1.406	16.875	20	3.125	37.500	31	4.844	58.125
10	1.563	18.750	21	3.281	39.375	32	5.000	58.125



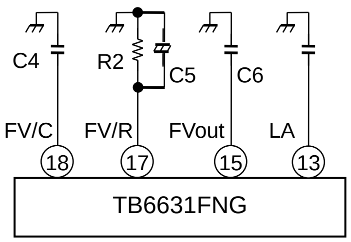
4.1. Terminal treatment in using auto lead angle function

In using auto lead angle function, set the external components as below. In this time, the LA terminal outputs voltage with the internal auto control by the frequency of the FG signal. Please configure the upper limit of the lead angle by the UL terminal.

Table 4.2 Terminal treatment in using auto lead angle function example

Pin number	Symbol	External component	Recommended value	Remarks
13	LA	C (LA)	Open	Capacitor for stabilization
15	FVout	C6	0.1 μF to 10 μF	Capacitor for stabilization
17	FV/R	R2	50 kΩ to 330 kΩ	Resistor for coefficient set of square curve
		C5	0.22 μF	Capacitor for stabilization
18	FV/C	C4	820 pF	Capacitor for coefficient set of square curve

<Application circuit example>



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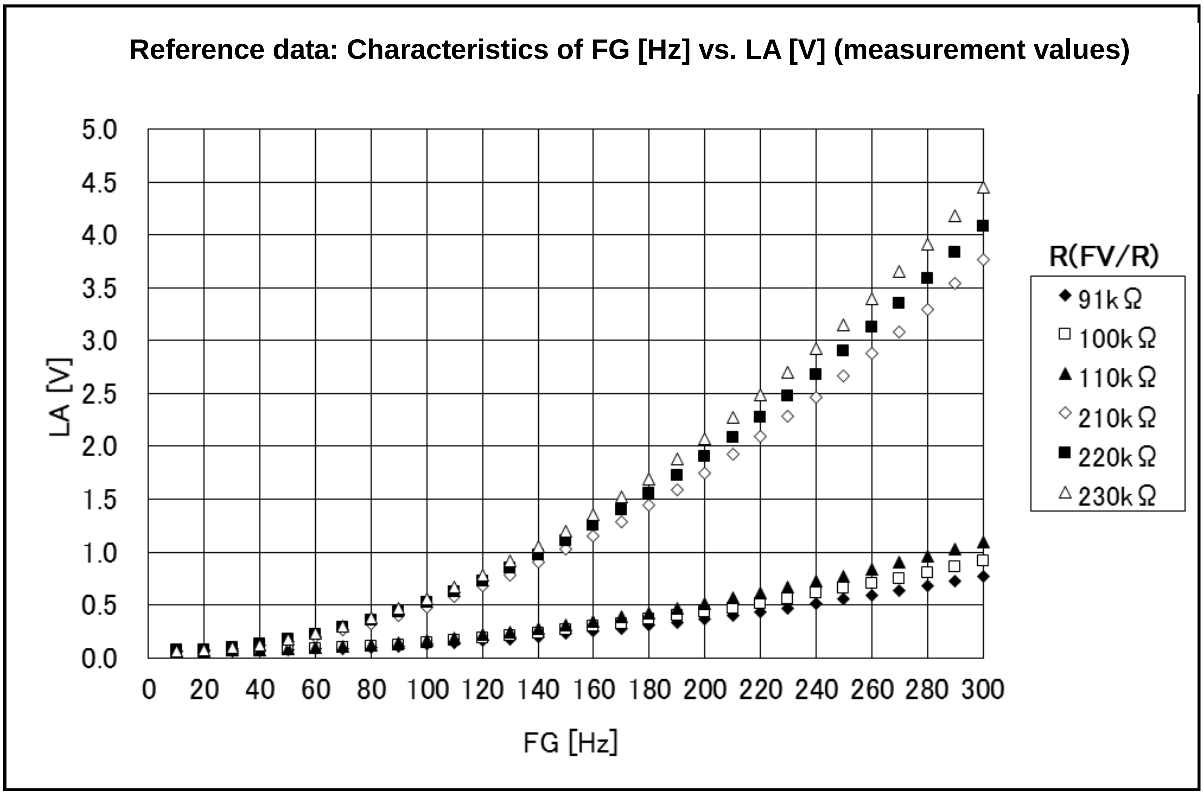


Reference data (measurement value)

R(FV/R)	91 kΩ	100 kΩ	110 kΩ	210 kΩ	220 kΩ	230 kΩ
C(FV/C)	820 pF	820 pF	820 pF	820 pF	820 pF	820 pF
FG [Hz]	LA [V]					
10	0.06	0.06	0.06	0.07	0.07	0.07
20	0.07	0.07	0.07	0.08	0.08	0.08
30	0.07	0.07	0.07	0.09	0.10	0.10
40	0.07	0.07	0.07	0.12	0.13	0.12
50	0.08	0.07	0.08	0.16	0.17	0.17
60	0.08	0.08	0.09	0.20	0.22	0.23
70	0.09	0.09	0.10	0.26	0.28	0.30
80	0.10	0.11	0.12	0.32	0.35	0.37
90	0.11	0.12	0.14	0.40	0.43	0.46
100	0.13	0.14	0.16	0.48	0.52	0.56
110	0.14	0.16	0.19	0.58	0.62	0.67
120	0.16	0.18	0.22	0.68	0.73	0.79
130	0.18	0.21	0.24	0.78	0.85	0.92
140	0.20	0.24	0.28	0.90	0.98	1.05
150	0.23	0.26	0.31	1.02	1.11	1.20

Reference data (measurement value)

R(FV/R)	91 kΩ	100 kΩ	110 kΩ	210 kΩ	220 kΩ	230 kΩ
C(FV/C)	820 pF	820 pF	820 pF	820 pF	820 pF	820 pF
FG [Hz]	LA [V]					
160	0.25	0.29	0.35	1.15	1.25	1.35
170	0.28	0.33	0.38	1.29	1.40	1.52
180	0.31	0.36	0.43	1.44	1.56	1.70
190	0.34	0.40	0.47	1.59	1.73	1.88
200	0.37	0.43	0.51	1.75	1.90	2.07
210	0.40	0.47	0.56	1.92	2.08	2.27
220	0.44	0.51	0.61	2.10	2.28	2.48
230	0.47	0.56	0.66	2.28	2.47	2.70
240	0.51	0.61	0.72	2.47	2.68	2.92
250	0.55	0.65	0.78	2.67	2.90	3.15
260	0.59	0.70	0.83	2.88	3.12	3.40
270	0.63	0.75	0.90	3.09	3.36	3.65
280	0.68	0.80	0.96	3.30	3.59	3.91
290	0.72	0.86	1.03	3.54	3.83	4.18
300	0.77	0.92	1.10	3.77	4.08	4.45

4.2. Setup auto lead angle

The lead angle changes depending on the applied motor. Therefore, to configure the most appropriate lead angle, please determine each constant number of the component by the actual equipment. The setup process is as follows;

Step 1) Drive the motor with necessary rotation number. Apply the voltage of 0 to 5 V to the LA terminal externally. Confirm the current or the efficiency to find the most appropriate LA voltage. When the motor current or the efficiency has the smallest value in the same rotation speed before or after lead angle change, the LA voltage is the most appropriate value.
When the lead angle is limited by the UL terminal, please connect the UL terminal to Vrefout as needed and release the limitation of the lead angle.

Step 2) Please change the constant number of the external component of R2 to set the LA voltage, which corresponds to the voltage shown in 'Step 1'. The relation of the external R2, C4, and FG frequency, and LA voltage is shown in the below formula.
LA voltage = 1393 × (C4 × R2 × FG frequency) ^ 2 [V]
Conditions:
FG frequency = 150 Hz
FV/C terminal: 820 pF (C4)
FV/R terminal: 220 kΩ (R2), 0.22 µF
FVout terminal: 0.1 µF

Step 3) Drive the motor and confirm that LA voltage equals to the voltage determined in "Step 1".

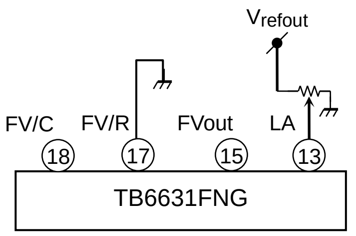
4.3. Terminal treatment in using external input lead angle function

In case of controlling the lead angle by inputting the external voltage to the LA terminal, please configure the external components as follows. Please connect the UL terminal to Vrefout.

Table 4.3 Terminal treatment in using external input lead angle function example

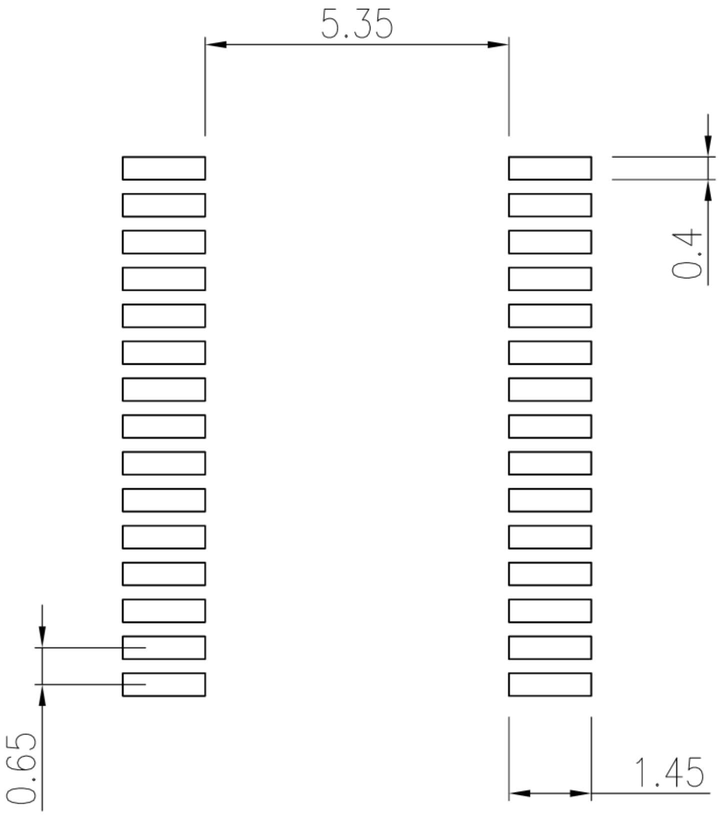
Pin No.	Pin name	External component	Remarks
13	LA	—	LA terminal: External input
15	FVout	None or C (FVout)	—
17	FV/R	Connect to GND	—
18	FV/C	None	—

<Application circuit example>



5. Land pattern dimensions (for reference only)

SSOP30-P-300-0.65 Unit: mm



Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

Figure 5.1 Land pattern dimensions (for reference only): SSOP30-P-300-0.65

Notes on Contents

1. Block Diagrams
   Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
   The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
   Timing charts may be simplified for explanatory purposes.

4. Absolute Maximum Ratings
   The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these absolute maximum ratings.
   Exceeding the absolute maximum rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
   Please use the IC within the specified operating ranges.

5. Application Circuits
   The application circuits shown in this document are provided for reference purposes only.
   Thorough evaluation is required, especially at the mass production design stage.
   Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

6. Test Circuits
   Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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