TB67Z800FTG
Usage considerations

Summary

The TB67Z800FTG incorporates 3-channel half bridge driver. It can control all channels independently.

Contents

Figure contents

1. Power supply

Operating range of the power supply voltage is 4 V to 22 V. The absolute maximum rating of the power supply voltage is 25 V that must not be exceeded, even for a moment. Do not exceed any of these ratings. Please use the IC within the range of the power dissipation.
Please pay attention in using the IC when the voltage of VM is 5.5 V or less because the characteristics of the output on resistance and the output voltage of VREG change in this condition.

2. Output current

The absolute maximum rating is 3 A. The absolute maximum rating is a set of a rating that must not be exceeded, even for a moment. Do not exceed any of these absolute maximum ratings for the rush current in motor startup and the current in the lock mode.
The average output current shall be increased or decreased depending on usage conditions such as ambient temperature and IC mounting method.
Take enough margins in designing so that the junction temperature of 150°C (Tj) is not exceeded.

3. Application circuit example

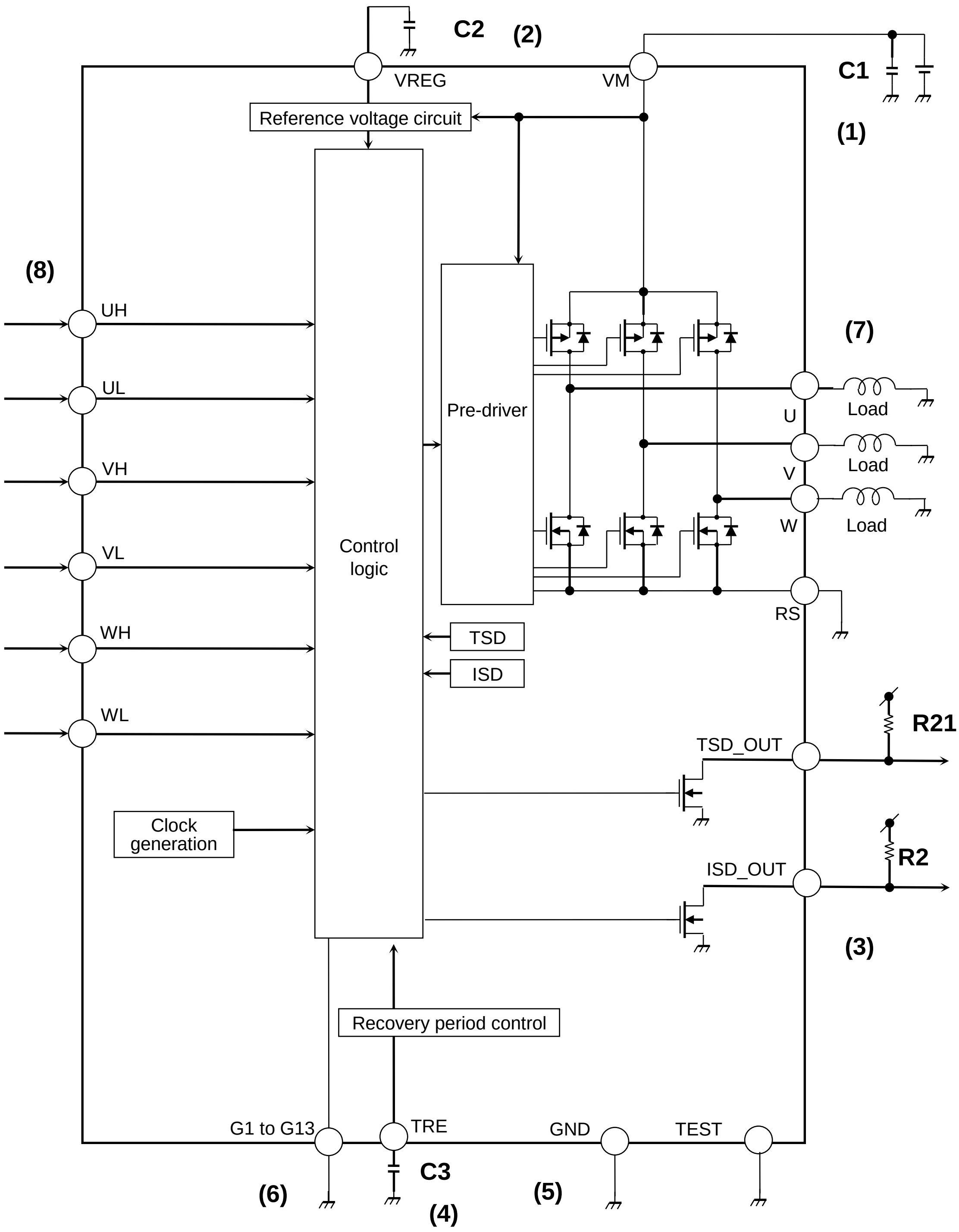


Figure 3.1 Application circuit example

(1) Capacitor for VM terminal

Take the GND pattern of the print board widely because large current flows from the power supply to the motor through VM terminal.
Connect the capacitor between VM and GND as close to the IC as possible in order to reduce the noise and vibration of VM terminal.

1 μF to 47 μF: Electrolytic capacitor
0.001 μF to 10 μF: Ceramic capacitor

When the power of the motor is small, applying the ceramic capacitor is enough.
However, the vibration of the power supply can be reduced more efficiently by connecting the large capacity of the electrolytic capacitor for reduction of low-frequency noise and the ceramic capacitor for reduction of high-frequency noise in parallel.

(2) Capacitor for VREG terminal

Connect the capacitor of 0.1 μF between VREG and GND as close to the IC as possible to reduce the noise and the vibration of VREG terminal.

(3) Setting TSD_OUT and ISD_OUT terminals

It is an open-drain output. So, the voltage should be pull-up by the resistance to output high level.
It is recommended to connect the resistance of 10 kΩ to 100 kΩ.

It incorporates the thermal shutdown circuit (TSD). When the junction temperature (Tj) exceeds 165 °C (typ.), all outputs are turned off (High-impedance: Hi-Z). Then, TSD_OUT terminal outputs low.
Moreover, it has the hysteresis of 15 °C (typ.). When the junction temperature (Tj) decreases, this function is released and the state of the TSD_OUT terminal is high level (Hi-Z).

Over–current detection (ISD) is incorporated in each of six output power transistors.
The range of the detection current is 3 A to 6 A. If any of them exceeds the threshold value, all outputs are turned off (High-impedance: Hi-Z).
This function is released after the capacitor restarting term of the TRE terminal is completed.

(4) Setting TRE terminal

Over–current detection (ISD) is incorporated in each of six output power transistors.
The range of the detection current is 3 A to 6 A. If any of them exceeds the threshold value, all outputs are turned off (High-impedance: Hi-Z).
Restart term can be set by the capacitor of TRE terminal.

Restart term: T = 0.313×31.5 times×C×10 ˆ 6
When C = 1 μF, T = 9.86 s

(5) Setting GND terminal

Please take the GND wiring pattern widely with solid wiring as possible.

(6) Setting TEST terminal / Setting G1 to G13 terminals

Please connect to GND.

(7) Setting U, V, W, and RS terminals

Please take the wiring pattern widely because large current flows in the motor.

(8) Setting UH, UL, VH, VL, WH, and WL terminals

Inputting and outputting are according to the below table.

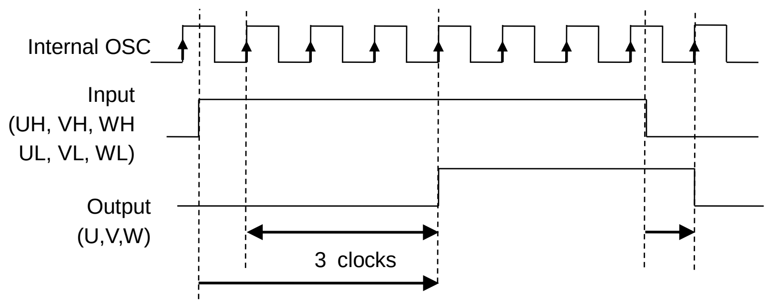
1. Function table

Mode	UH	UL	U
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

Mode	VH	VL	V
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

Mode	WH	WL	W
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

Logical output changes in synchronization with OCS clocks. To avoid generation of penetrating current, when logical input changes from low to high, the outputting level changes after the delay of 3 OCS clocks is inserted. Frequency of OSC is 9 MHz ±30 %.



4. Power consumption

The power consumption is calculated from below formulas.

Power consumption P [W] = VM × IM + I (RMS)^2 × Ron
Example: When VM = 12 V and IOUT (peak) = 1.1 A,
(As for circuit current (IM) and output ON resistance (RON), please refer to 'Electrical characteristics' in the technical data sheet.)

$$P(IC)\ Typ = 12\ V \times 6\ mA + (0.707 \times 1.1\ A)^2 \times 0.6\Omega = 0.432\ W$$
$$P(IC)\ Max = 12\ V \times 8.5\ mA + (0.707 \times 1.1\ A)^2 \times 1.2\ \Omega = 0.827\ W$$

Junction temperature (Tj) of the IC is calculated from the ambient temperature (Ta) and the power consumption shown below.

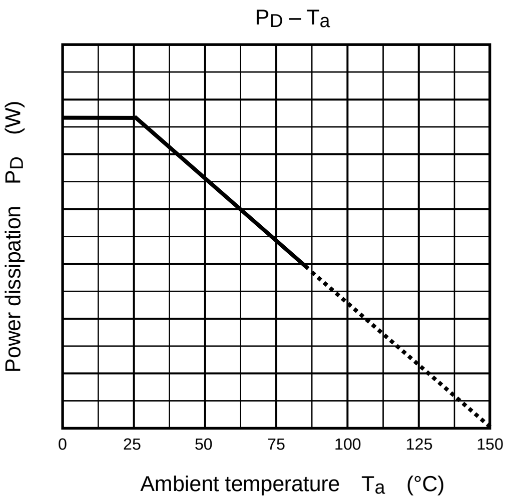
$$Tj = P \times \theta ja + Ta$$

θ ja: Heat resistance between junction temperature and ambient temperature
Ta: Ambient temperature (Surrounding constant temperature which avoids influence of heat)

Example: When mounted to the package, θja is calculated 44.64°C/W from the power dissipation provided in below figure.
When Ta = 85°C, Power consumption (P MAX) = 0.827 W,

$$Tj = 0.827\ W \times 44.64°\ C/W + 85°\ C = 122°\ C$$

Pay attention that θja depends on the usage conditions such as mounting method.
When ambient temperature is high, the power dissipation decreases.
Please use the IC with enough margin after evaluating the board by setting the junction temperature 150°C or less because above formulas are rough calculations.



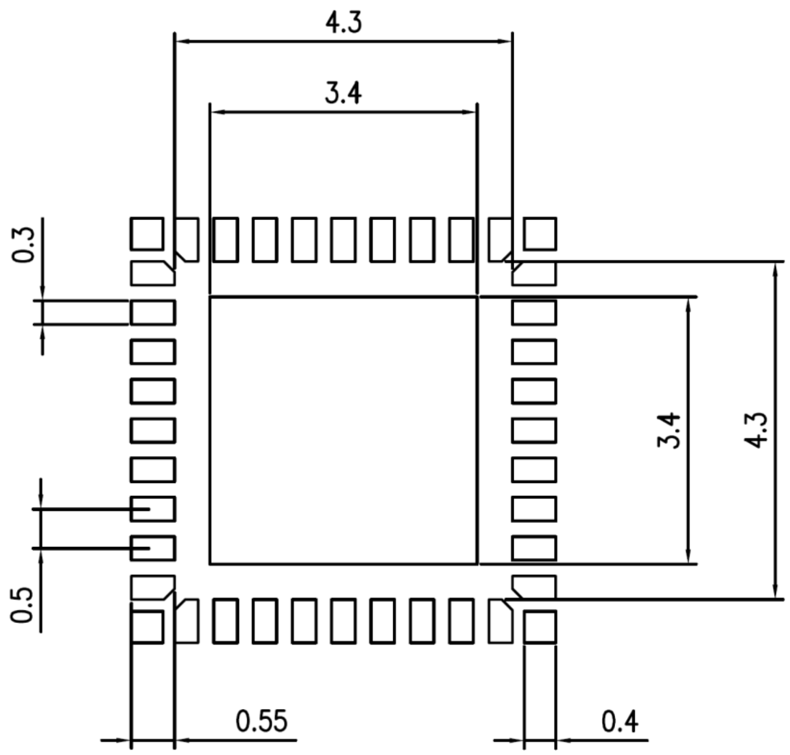
When mounted to the board
(4-layer FR4 board:76.2 mm × 114.3 mm × 1.6 mm)

Figure 4.1 Power dissipation

5. Land pattern dimensions (for reference only)

(1) P-VQFN36-0505-0.50-001

Unit: mm



Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

Figure 5.1 Land pattern dimensions (for reference only) (P-VQFN36-0505-0.50-001**)**

Note 1: Design the pattern in consideration of the heat design because the back side (E-PAD (3.4 mm×3.4 mm)) and the four corners of the PAD have the role of heat radiation. (The back side (E-PAD) and the four corners of the PAD should be connected to GND because they are connected to the back of the chip electrically.)

Note 2: Because each U, V, W, RS, and VM has two pins, short out these two pins at the external pattern respectively.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

RESTRICTIONS ON PRODUCT USE