APPLICATION NOTE (Summary)

TC90205FG

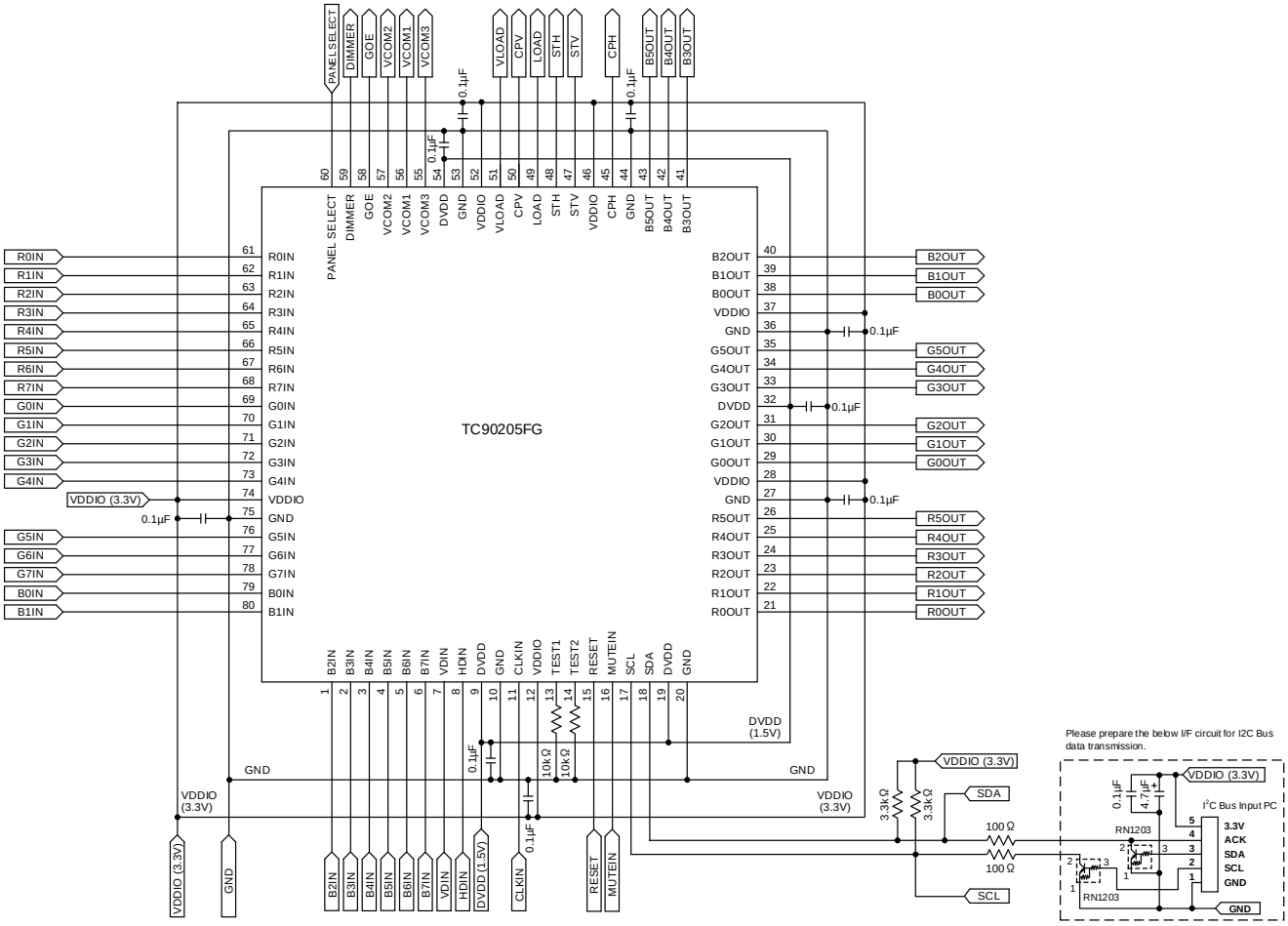
1. Overview

TC90205FG has picture quality improver (Horizontal lower bit expander, Edge Enhancement, Color adjustment, contrast adjustment, etc.) for input digital RGB video signal (6bit/8bit), and it outputs digital RGB video signal (6bit/8bit).
Timing control signals for panel operating are outputted with RGB video signal.

2. Feature

- Input and output video signal format are digital RGB (WVGA) or ITU-R BT.601 (720x480(480p)).
- It has picture quality improver.
- It has timing control pulse output for LCD panel.
- It needs to transmit data of I²C Bus.
- Power supply : 3.3V , 1.5V
- Package : LQFP80pin 12 x 12 mm (LQFP80-P-1212-0.50F)

3. An example of Application Circuit



4. Pin Description

Pin No.	Pin name	Block	IO	Function
1	B2IN	Digital IN	Input	Digital RGB input (B2)
2	B3IN	Digital IN	Input	Digital RGB input (B3)
3	B4IN	Digital IN	Input	Digital RGB input (B4)
4	B5IN	Digital IN	Input	Digital RGB input (B5)
5	B6IN	Digital IN	Input	Digital RGB input (B6)
6	B7IN	Digital IN	Input	Digital RGB input (B7)
7	VDIN	Digital IN	Input	Digital RGB input (Vertical sync signal)
8	HDIN	Digital IN	Input	Digital RGB input (Horizontal sync signal)
9	DVDD	Power	-	1.5V power supply for logic block
10	GND	Power	-	GND
11	CLKIN	Digital IN	Input	Digital RGB input (Clock signal)
12	VDDIO	Power	-	3.3V power supply for I/O block
13	TEST1	TEST	Input	For TEST
14	TEST2	TEST	Input	For TEST
15	RESET	RESET	Input	Reset control
16	MUTEIN	MUTE	Input	Mute control
17	SCL	I^2C	Input	I^2C -BUS control (SCL)
18	SDA	I^2C	I/O	I^2C -BUS control (SDA)
19	DVDD	Power	-	1.5V power supply for logic block
20	GND	Power	-	GND
21	R0OUT	Digital OUT	Output	Digital RGB output (R0)
22	R1OUT	Digital OUT	Output	Digital RGB output (R1)
23	R2OUT	Digital OUT	Output	Digital RGB output (R2)
24	R3OUT	Digital OUT	Output	Digital RGB output (R3)
25	R4OUT	Digital OUT	Output	Digital RGB output (R4)
26	R5OUT	Digital OUT	Output	Digital RGB output (R5)
27	GND	Power	-	GND
28	VDDIO	Power	-	3.3V power supply for I/O block
29	G0OUT	Digital OUT	Output	Digital RGB output (G0)
30	G1OUT	Digital OUT	Output	Digital RGB output (G1)
31	G2OUT	Digital OUT	Output	Digital RGB output (G2)
32	DVDD	Power	-	1.5V power supply for logic block
33	G3OUT	Digital OUT	Output	Digital RGB output (G3)
34	G4OUT	Digital OUT	Output	Digital RGB output (G4)
35	G5OUT	Digital OUT	Output	Digital RGB output (G5)
36	GND	Power	-	GND
37	VDDIO	Power	-	3.3V power supply for I/O block
38	B0OUT	Digital OUT	Output	Digital RGB output (B0)
39	B1OUT	Digital OUT	Output	Digital RGB output (B1)
40	B2OUT	Digital OUT	Output	Digital RGB output (B2)

Pin No.	Pin name	Block	IO	Function
41	B3OUT	Digital OUT	Output	Digital RGB output (B3)
42	B4OUT	Digital OUT	Output	Digital RGB output (B4)
43	B5OUT	Digital OUT	Output	Digital RGB output (B5)
44	GND	Power	-	GND
45	CPH	LCD control	Output	Control signal for LCD panel (Horizontal clock signal)
46	VDDIO	Power	-	3.3V power supply for I/O block
47	STV	LCD control	Output	Control signal for LCD panel (Vertical start pulse for writing)
48	STH	LCD control	Output	Control signal for LCD panel (Horizontal start pulse for writing)
49	LOAD	LCD control	Output	Control signal for LCD panel (Horizontal enable pulse for writing)
50	CPV	LCD control	Output	Control signal for LCD panel (Vertical clock signal)
51	VLOAD	LCD control	Output	Control signal for LCD panel (Vertical enable pulse for writing)
52	VDDIO	Power	-	3.3V power supply for I/O block
53	GND	Power	-	GND
54	DVDD	Power	-	1.5V power supply for logic block
55	VCOM3	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 3)
56	VCOM1	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 1)
57	VCOM2	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 2)
58	GOE	LCD control	Output	Control signal for LCD panel (Panel reset signal)
59	DIMMER	PWM	Output	PWM signal output
60	PANELSELECT	LCD control	Input	Control signal for LCD panel (Polarity select for GOE signal)
61	R0IN	Digital IN	Input	Digital RGB input (R0)
62	R1IN	Digital IN	Input	Digital RGB input (R1)
63	R2IN	Digital IN	Input	Digital RGB input (R2)
64	R3IN	Digital IN	Input	Digital RGB input (R3)
65	R4IN	Digital IN	Input	Digital RGB input (R4)
66	R5IN	Digital IN	Input	Digital RGB input (R5)
67	R6IN	Digital IN	Input	Digital RGB input (R6)
68	R7IN	Digital IN	Input	Digital RGB input (R7)
69	G0IN	Digital IN	Input	Digital RGB input (G0)
70	G1IN	Digital IN	Input	Digital RGB input (G1)
71	G2IN	Digital IN	Input	Digital RGB input (G2)
72	G3IN	Digital IN	Input	Digital RGB input (G3)
73	G4IN	Digital IN	Input	Digital RGB input (G4)
74	VDDIO	Power	-	3.3V power supply for I/O block
75	GND	Power	-	GND
76	G5IN	Digital IN	Input	Digital RGB input (G5)
77	G6IN	Digital IN	Input	Digital RGB input (G6)
78	G7IN	Digital IN	Input	Digital RGB input (G7)
79	B0IN	Digital IN	Input	Digital RGB input (B0)
80	B1IN	Digital IN	Input	Digital RGB input (B1)

5. I²C Bus Control

5.1 Slave address

It has 2 slave address (0xBC or 0xBE).
It is setup by the terminal “PANELSELECT”.
(The polarity of GOE signal is inverted by PANELSELECT terminal status.)
The mode (Write mode and Read mode) is determined by LSB of slave address.

PANELSELECT pin	Slave address	
	Write mode	Read mode
L	0xBC	0xBD
H	0xBE	0xBF

5.2 Segment address

TC90205FG has Segment Address, and applies to Sub Address below Segment Address.

Segment address	Contents
0x00	Input signal setting Output signal setting for panel control (T-con) Test pattern output Horizontal lower bit expander Picture quality improver (HVD enhancer)
0x01	Picture quality improver (Horizontal enhancer, Color management, Dynamic Y-gamma correction, etc…) PWM signal setting, Masking process
0x02	RGB gamma correction, Dither, FRC

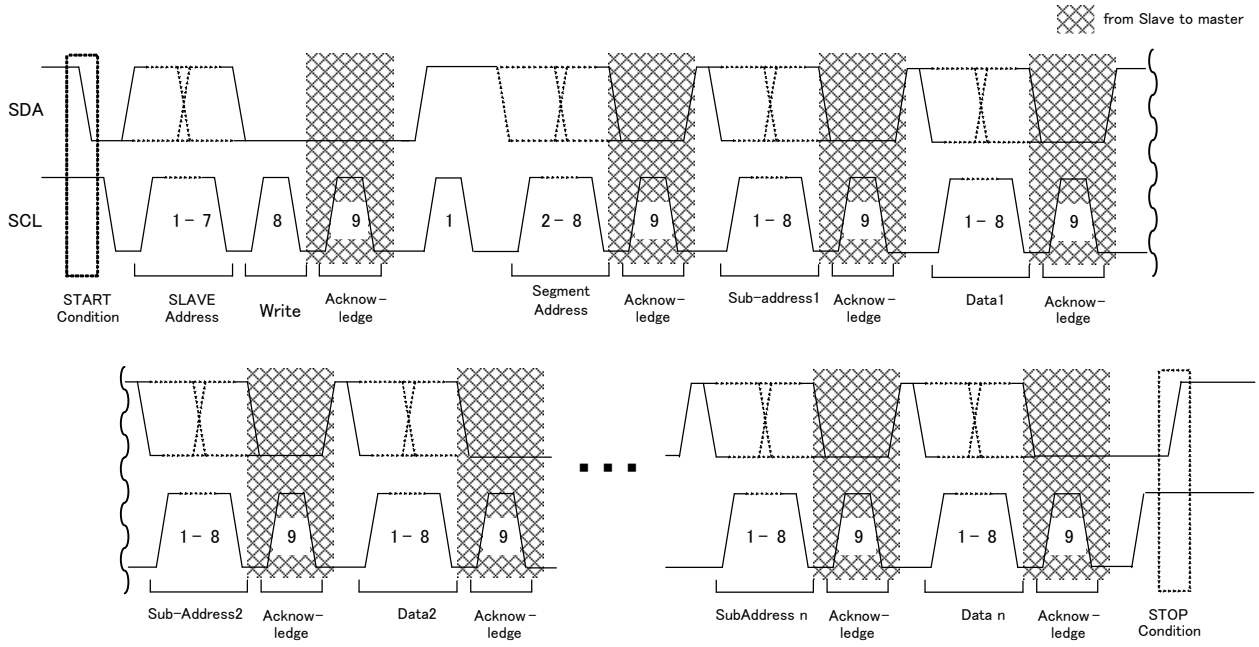
5.3 Data transmission format

5.3.1 Write mode format

When the LSB of the SLAVE Address is set to 0, it means the write mode.
The write mode format for one Sub-Address data has the following sequence:
START Condition/ SLAVE Address (write mode)/ Segment Address/ Sub-Address/ Data / STOP Condition.

5.3.2 Multi sub address write mode format

When the MSB of the Segment Address is set to 1, it means the multi Sub-Address write mode format as shown in following image.
This mode can translate two or more Sub-Address data, and it has the following sequence:
START Condition/ SLAVE Address (write mode)/ Segment Address (MSB=1)/ Sub-Address1/ Data1 / Sub-Address2/ Data2 /.../ Sub-Address n/ Data n / STOP Condition.

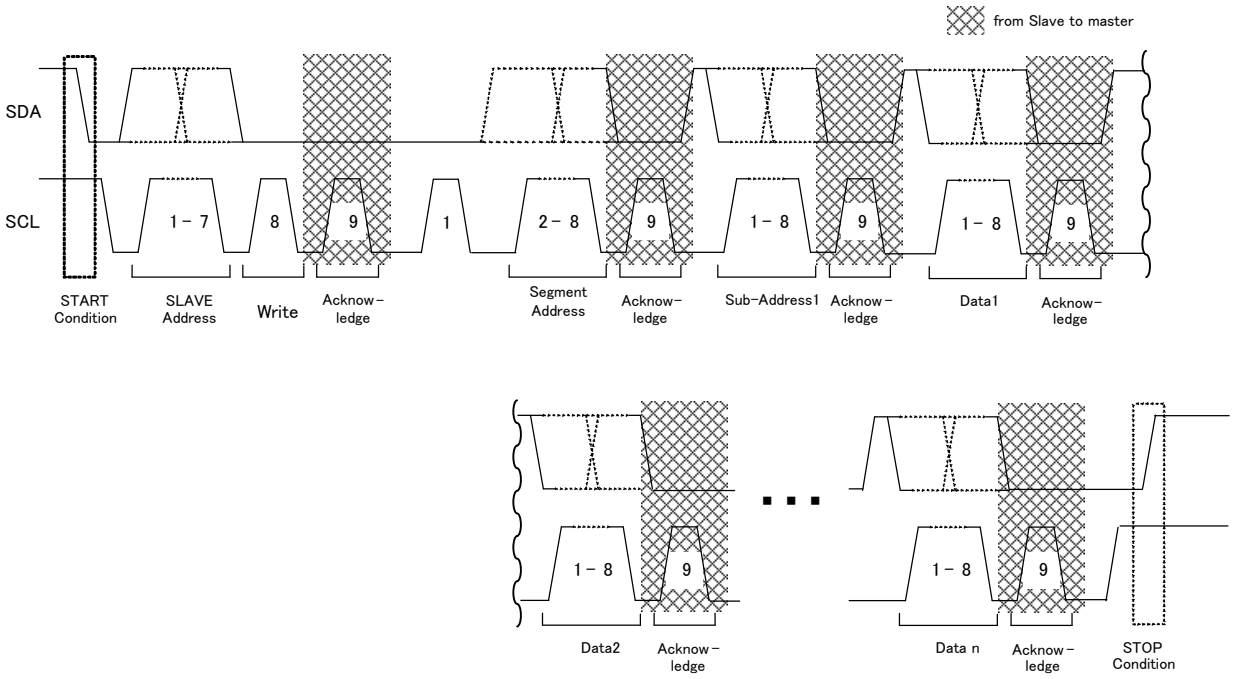


5.3.3 Continuous write mode format (Auto increment mode)

When the MSB of the Segment Address byte is set to 0, it means the continuous write mode format as shown in following image.

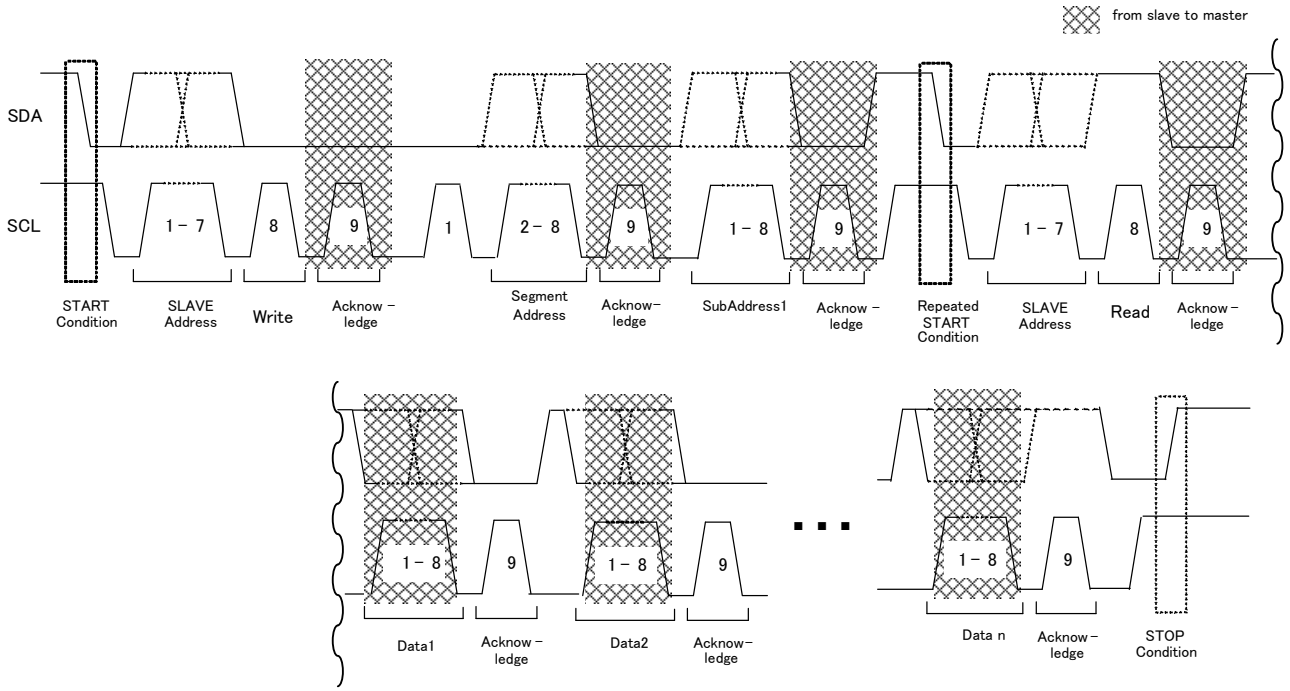
This mode can translate two or more data which have continuous Sub-Address, and it has the following sequence:

START Condition/ SLAVE Address (write mode)/ Segment Address (MSB=0)/ Sub-Address1/ Data1 / Data2 /.../ Data n (=Sub-Address n+1) / STOP Condition.



5.3.4 Read mode

When the LSB of the SLAVE Address is set to 1, it means the read mode as shown in following image.
The read mode has continuous mode only. (auto increment of Sub-Address).
The sequence of this mode is as follows:
START Condition/ SLAVE Address (write)/ Segment Address/ Sub-Address/ Repeated START Condition/ SLAVE Address (read)/ Data1(read) / Data2(read) /.../ Data n (read) / STOP Condition.
At the first, this mode needs to set Segment Address and Sub-Address with write mode, and then Repeated START Condition is also needed to start to read sequence.
And more, the master should output negative ACK(High) at the last read data before the STOP Condition.
If the STOP Condition is send without this negative ACK, this LSI does not recognize the end of read sequence and does not release SDA line to open condition until next START Condition or negative ACK.
And more, if there is no negative ACK(High) then this LSI keeps outputting until the Sub-Address reaches 0xFF, and repeats the output of the data of the Sub-Address 0xFF afterwards. So please notice about this negative ACK output to avoid data translation error.



6. Register

● **Please not change the data value of the registers** which are colored to gray in this document, because these registers are defined as "Reserved".
If “Reserved” register bit exists on sub address to change data, **please write initial data value to the bit on the “Reserved” register and don’t change the value**.

● not VLT：Not concerned with vertical sync signal timing, it changes to new data.
● INIT: **：Default setting.
● Underline portion are default setting.
● In this document, data value is described as follows.
Ex. 0x3F(hexadecimal) = 0011_1111 (binary) = 63 (decimal)

6.1 Segment Address 0x00

6.1.1 Sub Address 0x00 (Input / output terminal control)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x00	**IPIN_SEL[3:0]**				**OUTBIT**	Reserved	**OPIN_SEL[1:0]**	
not VLT	DRGB-in bit selection		Input bit reverse	Input R/B reverse	RGB output bit number		Output bit reverse	Output R/B reverse
INIT: 0x00	00:8bit 01:6bit 1*:6bit (lower bit interpolation)		0:Normal 1:MSB/LSB reverse	0:Normal 1:R-B (Y-C) interchange	0: 6bit 1: 8bit	Fix to 0	0:Normal 1:MSB/LSB reverse	0:Normal 1:RB(YC) interchange

IPIN_SEL[3:2]: Bit selection for digital RGB input
00: 8bit input
01: 6bit input
1*: 6bit input (lower bit interpolation)

IPIN_SEL[1]: MSB/LSB reverse for digital RGB input
0: Normal
1: MSB/LSB reverse
Ex) R signal
R7IN pin to R0 input, R6IN pin to R1 input, …, R0IN pin to R7 input

The case of 6bit input mode at IPIN_SEL[3:2], for R7IN to R2IN signal are processed.
(An example of R signal input.)
Therefore the processing is R7IN pin = R2 input, R6IN pin = R3 input, …, R2IN pin = R7 input

IPIN_SEL[0]: R-B signal interchange for digital RGB input
0: Normal
1: R-B interchange
It can interchange R input signal and B input signal.
R7IN pin = B7 input, R6IN = B6 input, …, R0IN pin = B0 input
B7IN pin = R7 input, B6IN = R6 input, …, B0IN pin = R0 input

OUTBIT: Bit number of digital RGB output signal
0: 6bit
1: 8bit
When 8bit-RGB signal output, the lower 2bit is outputted from the timing signal output pin. When 8bit-RGB signal output, the register “OPIN_SEL[1]” cannot use.

OPIN_SEL[1]: MSB/LSB reverse for digital RGB output

0: Normal
1: MSB/LSB reverse
Ex) R signal
R5OUT pin = R0 output, R4OUT pin = R1 output, …, R0OUT pin = R5 output

OPIN_SEL[0]: R-B interchange for digital RGB output
0: Normal
1: R-B interchange
It can interchange R output signal and B output signal.
R5OUT pin to B5 output, R4OUT to B4 output, …, R0OUT pin to B0 output
B5OUT pin to R5 output, B4OUT to R4 output, …, B0OUT pin to R0 output

6.1.2 Sub Address 0x01 to 0x11 (Timing controller (T-con) pulse output)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x01	**LCD_Out**	**LCD_Out _Mode**	**P_CPV**	**P_LOAD**	**P_STH**	**P_VLOAD**	**P_STV**	**P_CPH**
not VLT	T-con pulse output 0:OFF (ALL Low) 1:ON	T-con Output mode 0:Other 1:Standard (HD,VD,DE)	CPV pulse polarity 0:Negative 1:Positive	LOAD pulse polarity 0:Negative 1:Positive	STH pulse polarity 0:Negative 1:Positive	VLOAD pulse polarity 0:Negative 1:Positive	STV pulse polarity 0:Negative 1:Positive	CPH pulse polarity 0:Negative 1:Positive
INIT: 0x7F								
0x02	**P_VCOM2**	**P_DE**	**EN_SEL**	**VCOM_2V**	**GOE_HOLD[2:0]**			**GOE_HP**
not VLT	VCOM2 polarity 0:Reverce polarity for VCOM1 1:Same polarity for VCOM1	Enable pulse polarity 0:Negative 1:Positive	VLOAD pin select 0:VLOAD 1:ENABLE	VCOM 2V mode 0:OFF 1:ON	GOE reset period 000:1V to 010:3V to 111:8V			GOE pulse output 0:OFF 1:ON
INIT: 0x64								
0x03	**STH_START[7:0]**							
not VLT	Start phase of STH pulse (Moving before leading edge of DE)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x04	**STH_WIDTH[7:0]**							
not VLT	Width of STH pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x05	Reserved	Reserved	**STV_VSTART[5:0]**					
not VLT	Width of STV pulse (Reference of DE timing)							
INIT: 0x02	Fix to 0	Fix to 0	00_0000:-1Line to 00_0010:+1Line to 11_1111:+62Line					
0x06	Reserved	Reserved	Reserved	**STV_VWIDTH[4:0]**				
not VLT	Width of STV pulse							
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	0_0000:1Line to 1_1111:32Line				
0x07	**STV_HSTART[7:0]**							
not VLT	Start phase of STV pulse (Moving before leading edge of DE)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x08	**LOAD_START[7:0]**							
not VLT	Start pulse of LOAD pulse (Moving before leading edge of DE)							
INIT: 0x08	00000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x09	**LOAD_WIDTH[7:0]**							
not VLT	Width of LOAD pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x0A	**CPV_START[7:0]**							
not VLT	Start phase of CPV pulse (Moving before leading edge of DE)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x0B	**CPV_WIDTH[7:0]**							
not VLT	Width of CPV pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x0C	**VLOAD_START[7:0]**							
not VLT	Start phase of VLOAD pulse (Moving before leading edge of DE)							
INIT: 0x08	00_0000_0000:-7clk to 00_0000_1000:+1clk to 11_1111_1111:+1016clk							
0x0D	**VLOAD_WIDTH[7:0]**							
not VLT	Width of VLOAD pulse							
INIT: 0x00	0000_0000:1clk to 1111_1111:256clk							
0x0E	**VLOAD_START [9:8]**		**VCOM_VSTART[5:0]**					
not VLT			VCOM start line (Reference of DE timing)					
INIT: 0x02			00_0000:-1Line to 00_0010:+1Line to 11_1111:+62Line					
0x0F	**VCOM_HSTART[7:0]**							
not VLT	VCOM start position (Moving before leading edge of DE)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							
0x10	**VCOM3_POL**	Reserved	**VCOM3_VSTART[5:0]**					
not VLT	VCOM3 polarity	Fix to 0	VCOM3 start line (Reference of DE timing)					
INIT: 0x02	0:Reverce polarity for VCOM1 1:Same polarity for VCOM1		00_0000:-1Line to 00_0010:+1Line to 11_1111:+62Line					
0x11	**VCOM3_HSTART[7:0]**							
not VLT	VCOM3 Horizontal start position (Moving before leading edge of DE)							
INIT: 0x08	0000_0000:-7clk to 0000_1000:+1clk to 1111_1111:+248clk							

6.1.3 Sub Address 0x13 to 0x15 (Input signal setting)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x13	**CLOCKIN**	**SYNCIN**	Reserved	**DE_END**	Reserved	Reserved	Reserved	**DMODE**
not VLT	Input Clock polarity	Input Sync polarity		Internal Synchronous reference				Input signal mode
INIT: 0x06	0:Normal 1: Reverse	0:Negative 1:Positive	Fix to 0	0:HD/VD 1:Enable	Fix to 0	Fix to 1	Fix to 1	0: WVGA 1 :480p
0x14	**H_STA[7:0]**							
not VLT	Horizontal start position adjustment of digital input 0000_0001:1clk to 1001_0111:151clk to 1111_1111:255clk Notes: 0000_0000: forbid							
INIT: 0x97								
0x15	**V_STA[7:0]**							
not VLT	Vertical start position adjustment of digital input 0000_0010:2Line to 0010_0110:38Line to 1111_1111:255Line Notes: 0000_0000, 0000_0001: forbid							
INIT: 0x26								

6.1.4 Sub Address 0x20 to 0x2E (Test pattern output)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x20	**SIGPAT**	Reserved	**UD**	**LR**	**PATTERN[3]**	**PATTERN[2:0]**		
not VLT	Test pattern		Horizon/ Vertical switch	Left/Right invert	YCbCr mode	Pattern select		
INIT: 0x00	0:OFF 1:ON	Fix to 0	0:Normal 1:H/V switch	0:Normal 1:Left/Right reverse	0:RGB 1:YCbCr	000:Raster (Black) 001:Color bar	010:Ramp 011:Raster 100:1dot-check/ Stripe	101:RGB gamma 110:Raster (black) 111:Input signal
0x21	**COLOR_TYPE**	**WINDOW_TYPE[2:0]**			Reserved	**FLM_TYPE[2:0]**		
not VLT	Color bar type	Window display				Diagonal line	Cross line	Frame line
INIT: 0x01	0:Normal 1:Vertical Y step added	0:OFF 1:ON	0:400x240 1:280x280	0:Inside 1:Outsidel	Fix to 0	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON
0x22	**FLM_LEVEL[7:0]**							
not VLT	Frame color							
INIT: 0xFF	0000_0000:0LSB(Black) to 1111_1111:255LSB(White)							
0x23	**WINDOW_LEVEL[7:0]**							
not VLT	Window color							
INIT: 0x00	0000_0000:0LSB(Black) to 1111_1111:255LSB(White)							
0x24	**POINT_TYPE[3:0]**				Reserved	**POINT_X[10:8]**		
not VLT	Cursor			Cross line mode				
	Line width		Size					
INIT: 0x00	00:OFF 01:1dot	10:3dot 11:5dot	0:19dot 1:39dot	0:OFF 1:ON	Fix to 0			
0x25	**POINT_X[7:0]**							
not VLT	Horizontal center position of Cursor **[10:0]**							
INIT: 0x00	000_0000_0000:1st dot to 011_0001_1111:800th dot							
0x26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**POINT_Y[9:8]**	
not VLT								
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0		
0x27	**POINT_Y[7:0]**							
not VLT	Vertical center position of Cursor **[9:0]**							
INIT: 0x00	00_0000_0000:1st line to 01_1101_1111:480th line							

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x28 **not VLT** INIT: 0x00	**RAMP_TYPE[3:0]**				RASTER_TYPE[3:0]			
	Ramp setting				Raster color	Fixed color for Raster		
	0000:Ramp	0001 to 0011 :Ramp	1000 to 1111 :Step	0100 to 0111 Unused	0:Fixed color 1:Register setting	000:White 001:Yellow 010:Cyan	011:Green 100:Magenta	101:Red 110:Blue 111:Black
0x29 **not VLT** INIT: 0x00	**RASTER_G[7:0]**							
	Green level of register setting for Raster							
	0000_0000:0LSB to 1111_1111:255LSB							
0x2A **not VLT** INIT: 0x00	**RASTER_B[7:0]**							
	Blue level of register setting for Raster							
	0000_0000:0LSB to 1111_1111:255LSB							
0x2B **not VLT** INIT: 0x00	**RASTER_R[7:0]**							
	Red level of register setting for Raster							
	0000_0000:0LSB to 1111_1111:255LSB							
0x2C **not VLT** INIT: 0x00	Reserved	Reserved	Reserved	Reserved	**RAMP_COLOR[1:0]**		**DOT_TYPE[1:0]**	
	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Ramp color		1dot-check/Stripe pattern	
					00:RGB Ramp 01:G Ramp	10:B Ramp 11:R Ramp	00:1dot-check 01:H Stripe	10:V Stripe 11:1dot-check (G)
0x2D **not VLT** INIT: 0x00	**BLACK_LEVEL[7:0]**							
	Black level for 1dot-check/Stripe							
	0000_0000:0LSB(Black) to 1111_1111:255LSB(White)							
0x2E **not VLT** INIT: 0xFF	**WHITE_LEVEL[7:0]**							
	White level for 1dot-check/Stripe							
	0000_0000:0LSB(Black) to 1111_1111:255LSB(White)							

Test pattern

1) Pattern : select **PATTERN[2:0]**
2) Window
3) Frame : Diagonal line, Cross line, External frame line
4) Cursor

SIGPAT: Test pattern function ON/OFF

0:OFF
1:ON

UD: Horizon-Vertical interchange of pattern

0: Normal
1: H/V switch
Available only selecting Color bar or Ramp

LR: Left-Right reverse of Pattern

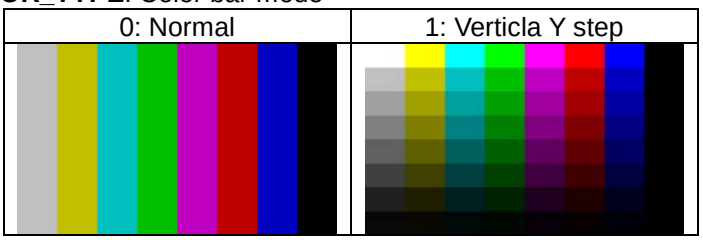
0: Normal
1: Left-Right reverse
Available only selecting Color bar or Ramp, 1dot check, Stripe.

PATTERN[3]: YCbCr mode

0: OFF
1: ON
Cb/Cr value is fixed 0 (Center) for window, cursor, frame. .
Only Y value is available for test pattern.

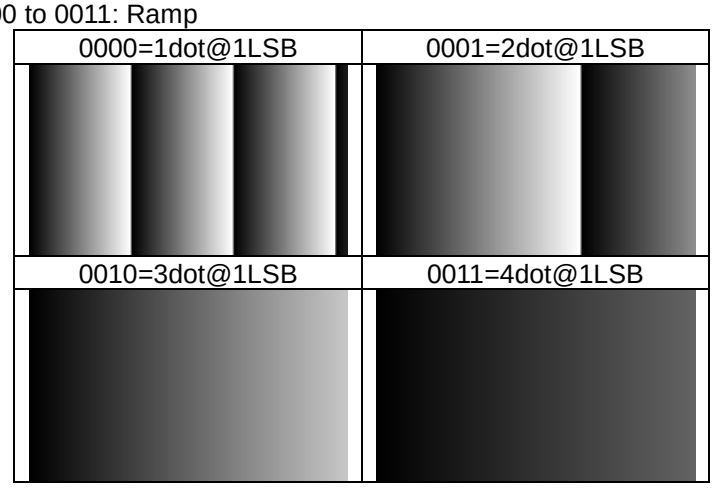
PATTERN[2:0]: Pattern select
- 000: Raster (Black)
- 001: Color bar
  - Mode select; **COLOR_TYPE**
- 010: Ramp
  - Mode select; **RAMP_TYPE[3:0]**
  - Color setting; **RAMP_COLOR[1:0]**
- 011: Raster
  - Raster color setting; **RASTER_TYPE[3:0], RASTER_G[7:0], RASTER_B[7:0], RASTER_R[7:0]**
- 100: 1dot-check / Stripe
  - Mode select; **DOT_TYPE[1:0]**
  - Color setting; **BLACK_LEVEL[7:0], WHITE_LEVEL[7:0]**
- 101: RGB gamma pattern
- 110: Raster (Black)
- 111: Input picture (no-pattern)

COLOR_TYPE: Color bar mode



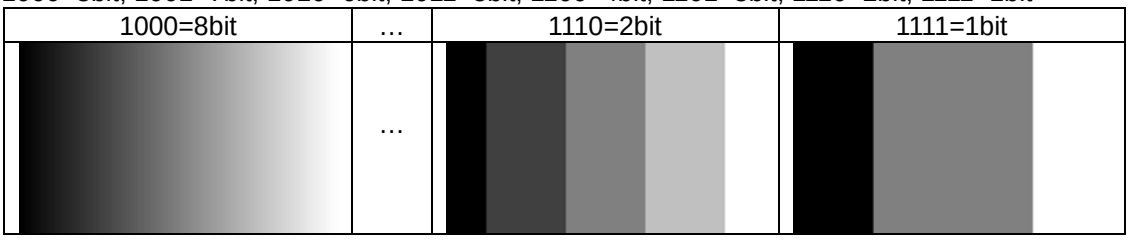
RAMP_TYPE[3:0]: Ramp mode

0000 to 0011: Ramp



1000 to 1111: Step

1000=8bit, 1001=7bit, 1010=6bit, 1011=5bit, 1100=4bit, 1101=3bit, 1110=2bit, 1111=1bit



RASTER_TYPE[3]: Color select for Raster
0: Fixed color
Color is selected by **RASTER_TYPE[2:0]**.
1: Register setting color
Color is setting by **RASTER_G[7:0]**, **RASTER_B[7:0]** and **RASTER_R[7:0]**.
RASTER_TYPE[2:0]: Select fixed color for Raster
000: White
001: Yellow
010: Cyan
011: Green
100: Magenta
101: Red
110: Blue
111: Black
RASTER_G[7:0]: Green level of register setting color for Raster
RASTER_B[7:0]: Blue level of register setting color for Raster
RASTER_R[7:0]: Red level of register setting color for Raster
0000_0000: 0LSB to 1111_1111: 255LSB

DOT_TYPE[1:0]: 1dot-check / Stripe mode
00: 1dot check (Black/White)
01: Horizontal Stripe (Black/White)
10: Vertical Stripe (Black/White)
11: 1dot check (Green)
BLACK_LEVEL[7:0]: Black level for 1dot-check / Stripe
0000_0000: 0LSB to 1111_1111: 255LSB
WHITE_LEVEL[7:0]: White level for 1dot-check / Stripe
0000_0000: 0LSB to 1111_1111: 255LSB

WINDOW_TYPE[2]: ON/OFF for Window
0: OFF
1: ON
WINDOW_TYPE[1]: Size setting for Window
0: 480x240
1: 280x280
WINDOW_TYPE[0]: Mode setting for Window
0: Internal
1: External
RGB value at selecting position is changed to the value of **WINDOW_LEVEL[7:0]**.
WINDOW_LEVEL[7:0]: RGB level for Window
0000_0000: 0LSB (Black) to 1111_1111: 255LSB (White)

FLM_TYPE[2]: ON/OFF for Diagonal line
0: OFF
1: ON
FLM_TYPE[1]: ON/OFF for Cross line
0: OFF
1: ON
FLM_TYPE[0]: ON/OFF for External flame line
0: OFF
1: ON

POINT_TYPE[3:2]: Line width for Cursor
00: OFF
01: 1dot
10: 3dot
11: 5dot
POINT_TYPE[1]: Size for Cursor
0: 19dot
1: 39dot
POINT_TYPE[0]: Cross line mode for Cursor
0: OFF
1: ON
POINT_X[10:0]: Horizontal position for Cursor
000_0000_0000: 1st dot to 011_0001_1111: 800th dot
POINT_Y[10:0]: Vertical position for Cursor
000_0000_0000: 1st line to 011_0001_1111: 480th line

6.1.5 Sub Address 0x30 to 0x36 (Horizontal lower bit interpolator)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x30	**SGRAD_ON**	**BIT6**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Horizontal lower bit interpolator	Forced 6bit Output						
INIT: 0x00	0:OFF 1:ON	0:Normal 1:6bit	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x31	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**565MODE**	**555MODE**
							5:6:5 mode	5:5:5 mode
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	0:OFF 1:ON	0:OFF 1:ON
0x32	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x33	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x34	**LENOFF**	**LEN[6:0]**						
	Restraining Horizontal line 1	Horizontal line restraining 1 (By width of neighbor step)						
INIT: 0x00	0:OFF 1:ON	000_0000:0dot to 111_1111:127dot						
0x35	Reserved	**LEN_C[6:0]**						
		Horizontal line restraining 2 (By width of self-step)						
INIT: 0x00	Fix to 0	000_0000:0dot to 111_1111:127dot						
0x36	Reserved	Reserved	Reserved	Reserved	**LENG[1:0]**		**LENG_C[1:0]**	
					Change step for Horizontal line restraining 1		Change step for Horizontal line restraining 2	
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	00:1dot 01:2dot	10:3dot 11:4dot	00:1dot 01:2dot	10:3dot 11:4dot

SGRAD_ON: ON/OFF for Horizontal lower bit interpolator
0: OFF
1: ON

BIT6: Forced 6bit Output
0: Normal (OFF)
1: 6bit out (ON)

565MODE: 5:6:5 mode
0: OFF
1: ON
In this mode, 5:6:5-input is outputted to 7:8:7 by interpolation.
555MODE has priority over **565MODE**.

555MODE: 5:5:5 mode
0: OFF
1: ON
In this mode, 5:5:5-input is outputted to 7:7:7 by interpolation.
555MODE has priority over **565MODE**.

LENOFF: Horizontal line restraining 1
0: OFF
1: ON
LEN[6:0]: Start width for Horizontal line restraining 1 (By width of neighbor step)
000_0000: 0dot to 111_1111: 127dot
When start width setting is made big, correction strength becomes weak.
LEN_C[6:0]: Threshold width for Horizontal line restraining 2 (By width of self-step)
000_0000: 0dot to 111_1111: 127dot
When start width setting is made big, correction strength becomes weak.

LENG[1:0]: Change step for Horizontal line restraining 1
00: 1dot to 11: 4dot
LENG_C[1:0]: Change step for Horizontal line restraining 2
00: 1dot to 11: 4dot

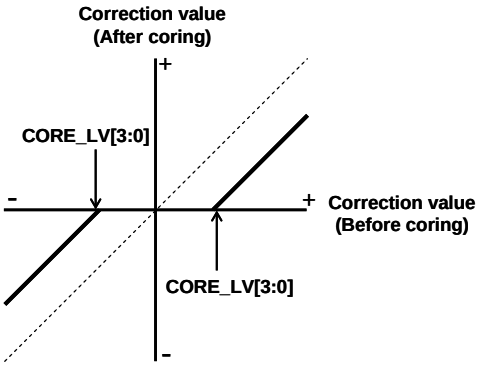
6.1.6 Sub Address 0x40 to 0x47,0x4E (HVD Enhancer, Noise canceller)

Segment 0x00

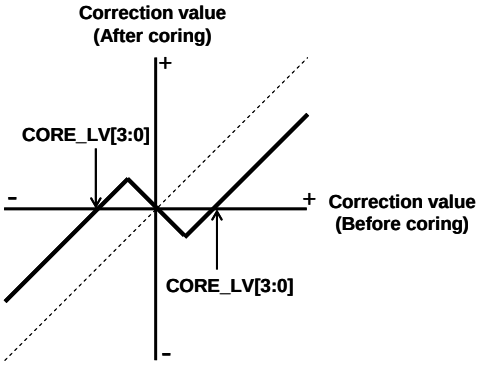
Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x40	**ENHON**	**CORE_MET**	Reserved	Reserved	Reserved	**HALFSEL**	Reserved	Reserved
	Enhancer	Noise canceller				Filter process		
INIT: 0x00	0:OFF 1:ON	0:OFF (Coring) 1:ON (N.C. process)	Fix to 0	Fix to 0	Fix to 0	0:OFF 1:ON	Fix to 0	Fix to 0
0x41	**V_35**	**V_OFF**	**H_SEL**	**H_35**	**H_OFF**	**D_SEL**	**D_35**	**D_OFF**
	Vertical tap		Horizontal tap			Diagonal tap		
INIT: 0x00	0:3tap 1:5tap	0:ON 1:OFF	0:Narrow 1:Wide	0:3tap 1:5tap	0:ON 1:OFF	0:Narrow 1:Wide	0:3tap 1:5tap	0:ON 1:OFF
0x42	**ENHLV[3:0]**				**ENHLV_CORE[3:0]**			
	Enhancer gain				Noise canceller gain			
INIT: 0x00	0000:min to 1111:max				0000:min to 1111:max			
0x43	**CORE_LV[7:0]**							
	Coring level							
INIT: 0x00	0000_0000:Coring OFF 0000_0001:min to 1111_1111:max							
0x44	Reserved	Reserved	Reserved	Reserved	Reserved	**LIM_ GAIN_SEL**	Reserved	Reserved
						LIM/GAIN sequence		
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	0:LIM->GAIN 1:GAIN->LIM	Fix to 0	Fix to 0
0x45	**YCO1_ON**	**YCO1_COLV**	Reserved	Reserved	**YCO1_YLV[3:0]**			
	Coring variable for Y 1	Coring variable for Y 1 Gain			Coring variable for Y 1 Start Y level			
INIT: 0x00	0:OFF 1:ON	0:Y/16 1:Y/8	Fix to 0	Fix to 0	0000: 0LSB to 1111: 480LSB (10bit, 32LSB step)			
0x46	**YCO2_ON**	**YCO2_COLV**	Reserved	Reserved	**YCO2_YLV[3:0]**			
	Coring variable for Y 2	Coring variable for Y 2 Gain			Coring variable for Y 2 Start Y level			
INIT: 0x00	0:OFF 1:ON	0:Y/16 1:Y/8	Fix to 0	Fix to 0	0000: 0LSB to 1111: 480LSB (10bit, 32LSB step)			
0x47	**LIMIT_ON**	**LIMIT_MET**	**LIMIT_LV[5:0]**					
	Enhancer Limit	Limit processing	Limit level					
INIT: 0x00	0:OFF 1:ON	0:Keep level 1:Paring	00_0000:0(OFF) 00_0001:min to 11_1111:max					
0x4E	Reserved	Reserved	Reserved	**CNRON**	**CNR_GAIN**			
				Chroma NR	Chroma NR			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	0:OFF 1:ON	Gain 0000:min to 1111:max			

ENHON: HVD Enhancer function
0: OFF
1: ON

CORE_MET: Select the coring processing for HVD enhancer
0: Coring mode (non-correction for coring area)
1: Noise canceller mode (minus gain for coring area)



<When **CORE_MET** = 0>



<When **CORE_MET** = 1>

6.1.7 Sub Address 0x50 to 0x5F (Dynamic Y-gamma correction by histogram detection)

Segment 0x00

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x50	**HDR_ON**	**HDR_C_OFF**	**HDR_HIST_ON**	Reserved	Reserved	Reserved	Reserved	Reserved
	ON/OFF	Color linkage	Histogram detection					
INIT: 0x20	0:OFF 1:ON	0:ON 1:OFF	0:OFF 1:ON	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x51 INIT: 0x03	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 1
0x52 INIT: 0x80	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x53 INIT: 0x03	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 1
0x54 INIT: 0x80	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x55 INIT: 0x00	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x56	**HDR_HISTGAIN[7:0]**							
INIT: 0xF0	Histogram Gain setting 0000 0000: Linear (Gain 0) to 1111 0000 to 1111 1111: Gain max							
0x57	**HDR_HISTBLEND[7:0]**							
INIT: 0xF0	Histogram Blending rate 0000 0000: Original to 1111 0000 to 1111 1111: Rate max							
0x58	Reserved	**HDR_HISTLIM_H[2:0]**			Reserved	**HDR_HISTLIM_L[2:0]**		
INIT: 0x22	Fix to 0	Limiter for upper limit gain 0:ON 1:OFF	Limit level width for upper limit gain 00:min to 10:typ. to 11: max		Fix to 0	Limiter for lower limit gain 0:ON 1:OFF	Limit level width for lower limit gain 00:min to 10:typ. to 11: max	
0x59 INIT: 0x20	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x5A INIT: 0x80	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x5B INIT: 0x70	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 1	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x5C INIT: 0x10	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x5D INIT: 0x03	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 1	Reserved Fix to 1
0x5E INIT: 0x00	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0	Reserved Fix to 0
0x5F	Reserved	Reserved	**IIR_ON[1:0]**		Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Histogram time constant 00: OFF, 01:Small 10: middle 11: Large		Fix to 0	Fix to 0	Fix to 0	Fix to 0

The registers (at Segment Add.0x00 Sub Add. 0x50 to 0x 5F) control the Dynamic YC gamma correction by histogram detection.

This function adjusts dynamically the Y gamma curve and C level by the histogram of input video signal. This function is processed before the Dynamic Y gamma (at Segment Add. 0x01).

The Dynamic Y gamma (at Segment Add. 0x01) is corrected sequentially, but this function is corrected with respect to each V. The detection area for this function is same as making area for picture quality improver.

6.2 Segment Address 0x01

6.2.1 Sub Address 0x00 to 0x02 (Forced-off of picture quality improver, Mute)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	**ENHOFF**	**CTIOFF**	**CNTBRTPS**	**CLVLPS**	**ROUNDDN**	**YMUTE**	**CMUTE**
		Y Enhancer	CTI	Contrast Brightness	Color level adjustment	Cut off lower bit for 6bit output	Y Mute	C Mute
INIT: 0x00	Fix to 0	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Normal 1:Cut off	0:Normal 1:YMUTE	0:Normal 1:CMUTE
0x01	**STGAN PASS**	**YGANPASS**	**COMPPASS**	Reserved	Reserved	**MTXOUTSW**	**BBACK**	**RGB MUTE**
	Static Y-gamma	Dynamic Y-gamma	C gain linked Y gamma			6bit accuracy ensuring	Blue Back	RGB Mute
INIT: 0x03	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	0:Noraml 1:Forced OFF	Fix to 0	Fix to 0	0:OFF 1:ON	0:Normal 1:Blue back	0:Normal 1:MUTE
0x02	**RGB_ CNTBRTPS**	Reserved	**CMPS**	Reserved	Reserved	Reserved	Reserved	**MUTE_AUTO**
	RGB adjustment of picture		Color Management					Mute by pin control
INIT: 0x00	0:Noraml 1:Forced OFF	Fix to 0	0:Noraml 1:Forced OFF	Fix to 0	Fix to 0	Fix to 0	Fix to 0	0:OFF 1:ON

Available register of “forced-off” are as follows.

Register	Switchable function
ENHOFF	Sharpness, LTI, YNC
CTIOFF	CTI, CNC
CNTBRTPS	Contrast, Brightness
CLVLPS	C gain, Cb/Cr offset
STGANPASS	Static Y-gamma correction
YGANPASS	Dynamic Y-gamma correction
COMPPASS	C gain linked Y gamma
RGB_CNTBRTPS	Picture RGB contrast Picture RGB brightness
CMPS	Color management Skin color correction, Tint

6.2.2 Sub Address 0x03 to 0x06 (Sharpness, LTI, YNC)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x03	Reserved	**ENHLIM[2:0]**			**ENHGA[2:0]**			**FENH**
	Fix to 0	Sharpness1 Coring level			Sharpness1 Gain			Sharpness1 f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001:*0.125% to 111:*0.875%			0:CLK/4 1:CLk/2
0x04	Reserved	**ENHLIM2[2:0]**			**ENHGA2[2:0]**			**FENH2**
	Fix to 0	Sharpness2 Coring level			Sharpness2 gain			Sharpness2 f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001:*0.125% to 111:*0.875%			0:CLK/8 1:CLK/6
0x05	Reserved	**LTILIM[2:0]**			**LTIGA[2:0]**			**FLTI**
	Fix to 0	LTI Coring			LTI Gain			LTI f0
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001:*0.125% to 111:*0.875%			0:CLK/6 1:CLK/4
0x06	Reserved	**NCLIM[2:0]**			**NCGA[1:0]**		**FNC[1:0]**	
	Fix to 0	YNC Coring			YNC gain		YNC f0	
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			00:OFF 01:*0.125% to 11:*0.5%		00:CLK/8 01:CLK/6	10:CLK/4 11:CLK/2

6.2.3 Sub Address 0x07 to 0x08 (Brightness, Contrast)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x07	Reserved	**ADJCONT[6:0]**						
	Fix to 0	Contrast						
INIT: 0x40		000_0000:*0 to 100_0000:*1 to 111_1111:*1.98						
0x08	Reserved	**ADJBRIT[6:0]**						
	Fix to 0	Brightness						
INIT: 0x00		100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (8bit,)						

6.2.4 Sub Address 0x09 to 0x0A (CTI, CNC)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x09	**FCTI[1]**	**CTILIM[2:0]**			**CTIGA[2:0]**			**FCTI[0]**
	CTI f0	CTI Coring			CTI Gain			CTI f0
INIT: 0x00	10:CLK/8 11:CLK/6	000:0LSB to 111:7LSB (1LSB step @8bit)			000:OFF 001:*0.250% to 111:*1.750%			00:CLK/16 01:CLK/12
0x0A	Reserved	**CNCLIM**			**CNCGA**		**FCNC**	
	Fix to 0	CNC Coring			CNC Gain		CNC f0	
INIT: 0x00		000:0LSB to 111:7LSB (1LSB step @8bit)			00:OFF 01:*0.125% to 11:*0.5%		00:CLK/8 01:CLK/6	10:CLK/4 11:CLK/2

6.2.5 Sub Address 0x0B to 0x0F (Cb/Cr gain, Cb/Cr offset, Tint)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x0B	**CBGAIN[7:0]**							
	Cb gain							
INIT: 0x40	0000_0000:*0 to 0100_0000:*1 to 1111_1111:*3.98							
0x0C	**CRGAIN[7:0]**							
	Cr gain							
INIT: 0x40	0000_0000:*0 to 0100_0000:*1 to 1111_1111:*3.98							
0x0D	Reserved	**CBOFS[6:0]**						
	Fix to 0	Cb offset						
INIT: 0x00		100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (8bit, 1LSB)						
0x0E	Reserved	**CROFS[6:0]**						
	Fix to 0	Cr offset						
INIT: 0x00		100_0000:-64LSB to 000_0000:0LSB to 011_1111:+63LSB (8bit, 1LSB)						
0x0F	**TINT[7:0]**							
	TINT adjustment							
INIT: 0x00	1111_1111: -44.8° to 1000_0000: -0.35° to 0000_0000: ±0° to 0111_1111: +44.45° 0.35° step							

6.2.6 Sub Address 0x10 to 0x14 (PWM output to DIMMER terminal)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x10	**PWM_MUTE**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	PWM linked to MUTE							
INIT: 0x00	0:OFF 1:ON	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x11	**PWM_SW**	Reserved	Reserved	Reserved	Reserved	Reserved	**PWM_NP**	**PWM_VLAT**
	PWM ON/OFF						Output Polarity	V latch control
INIT: 0x00	0:OFF 1:ON	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	0: Normal 1: Invert	0: OFF 1: ON
0x12	Reserved	Reserved	Reserved	Reserved	**PWM DUTY[11:8]**			
					DUTY setting [11:8]			
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0				
0x13	**PWM DUTY[7:0]**							
	DUTY setting [7:0]							
INIT: 0x00	0000_0000_0000:0.024% to 0111_1111_1111:50% to 1111_1111_1111:100.00%							
0x14	**PWM_SW[1:0]**		**PWM_DIV[5:0]**					
	PWM frequency		PWM frequency setting					
INIT: 0x00	00:1/2048 01:1/4096	10:1/8192 11:1/16384	00_0000:*1 to 11_1111:*64					

PWM pulse output function setting of DIMMER terminal is available in sub address 0x10 to 0x14.

Frequency of PWM output pulse

PWM output frequency is defined by panel clock frequency and register setting of **PWM_DIV[5:0]** and **PWM_SW[1:0]**.

The panel clock is presented as (A)[Hz] and the output PWM pulse frequency presented as (B)[Hz] in following formula.

(B) = (A) ÷ **PWM_SW** ÷ **PWM_DIV**

ex) In the case of panel clock: 33.3MHz, the maximum and minimum frequency are calculated as follows.

Max : 33.3[MHz] ÷ 2048 ÷ 1 = 16.26[kHz] (11bit resolution)
Min : 33.3[MHz] ÷ 16384 ÷ 64 = 31.76[Hz] (14bit resolution)

Notification of PWM output function

DIMMER terminal is Low statement at the reset condition. And this DIMMER terminal is not a open-drain type buffer, so do not make pull up with high voltage.

The duty is set by **PWM_DUTY[11:0]**, but there is not 0% setting. Please use **PWM_SET[7]** OFF setting for 0

6.2.7 Sub Address 0x15 to 0x1D (Color management, Skin color correction)

Segment 0x01

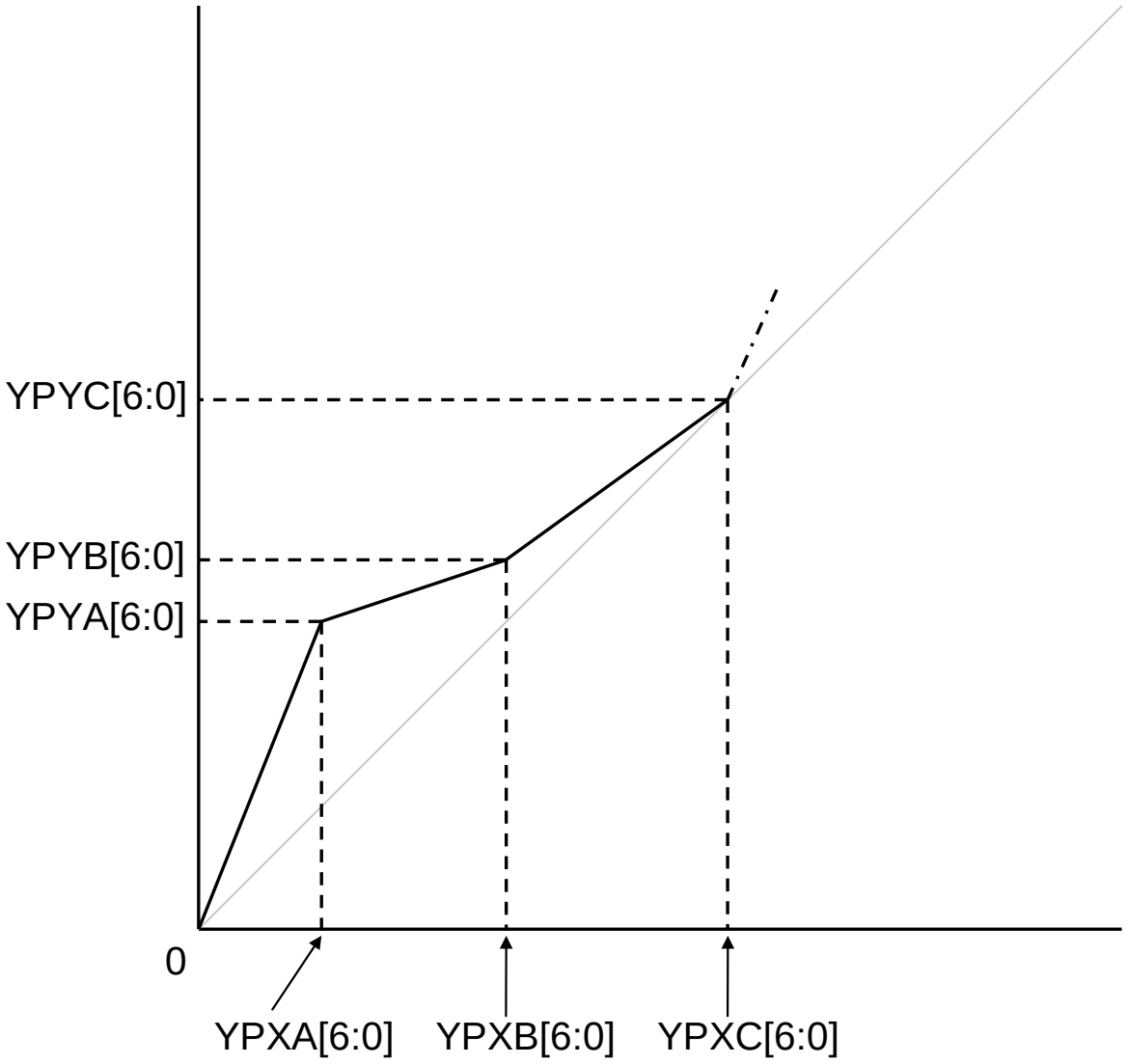
Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x15	**GAIN1[7:0]**							
	Color management (1st axis) gain setting							
INIT: 0x00	1000_0000: Color attenuation max to 0000_0000: OFF to 0111_1111: Color extension max							
0x16	**GAIN2[7:0]**							
	Color management (2nd axis) gain setting							
INIT: 0x00	1000_0000: Color attenuation max to 0000_0000: OFF to 0111_1111: Color extension max							
0x17	**GAIN3[7:0]**							
	Color management (3rd axis) gain setting							
INIT: 0x00	1000_0000: Color attenuation max to 0000_0000: OFF to 0111_1111: Color extension max							
0x18	**PH1[7:0]**							
	Color management (1st axis) center phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x19	**PH2[7:0]**							
	Color management (2nd axis) center phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x1A	**PH3[7:0]**							
	Color management (3rd axis) center phase setting							
INIT: 0x00	0x00: Cb(+) axis to 0x40: Cr(+) axis to 0x80: Cb(-) axis to 0xC0: Cr(-) axis to 0x00: Cb(+) axis							
0x1B	**CMON**	Reserved	**WIN3[1:0]**		**WIN2[1:0]**		**WIN1[1:0]**	
	Color management		3rd axis Correction width		2nd axis Correction width		1st axis Correction width	
INIT: 0x00	0:OFF 1:ON	Fix to 0	00:±22.5° 01:±45° 1*:±90°		00:±22.5° 01:±45° 1*:±90°		00:±22.5° 01:±45° 1*:±90°	
0x1C	**FRON**	**RNFROFF**	**LIM_FR[2:0]**			**GAIN_FR[2:0]**		
	Skin color correction	Skin color correction range C mute	Skin color correction Correction range of chroma level			Skin color correction Gain setting		
INIT: 0x00	0:OFF 1:ON	0:OFF 1:ON	000:OFF 001: min range to 111: max range			000:OFF 01: min to 111: max		
0x1D	**COLOFF**	**RN1OFF**	**RN2OFF**	**RN3OFF**	**WIN_FR**	**PH_FR[2:0]**		
	C Mute	1st axis C mute	2nd axis C Mute	3rd axis C Mute	Skin color correction Color Phase width	Skin color Center phase adjustment		
INIT: 0x00	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON	0:45° 1:90°	100:for red to 000:Center to 011:for green (2.8°step)		

6.2.8 Sub Address 0x20 to 0x2F (Static Y-gamma correction)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x20	Reserved	**YPXA[6:0]**						
		Static Y-gamma correction A X axis						
INIT: 0x0F	Fix to 0	000_0000: 1LSB to 000_1111: 31LSB to 111_1111: 255LSB (2LSB step)						
0x21	Reserved	**YPYA[6:0]**						
		Static Y-gamma correction A Y axis						
INIT: 0x0F	Fix to 0	000_0000: 1LSB to 000_1111: 31LSB to 111_1111: 255LSB (2LSB step)						
0x22	Reserved	**YPXB[6:0]**						
		Static Y gamma correction B X axis						
INIT: 0x1F	Fix to 0	000_0000: 1LSB to 001_1111: 63LSB to 111_1111: 255LSB (2LSB step)						
0x23	Reserved	**YPYB[6:0]**						
		Static Y-gamma correction B Y axis						
INIT: 0x1F	Fix to 0	000_0000: 1LSB to 001_1111: 63LSB to 111_1111: 255LSB (2LSB step)						
0x24	Reserved	**YPXC[6:0]**						
		Static Y-gamma correction C X axis						
INIT: 0x2F	Fix to 0	000_0000: 1LSB to 010_1111: 95LSB to 111_1111: 255LSB (2LSB step)						
0x25	Reserved	**YPYC[6:0]**						
		Static Y-gamma correction C Y axis						
INIT: 0x2F	Fix to 0	000_0000: 1LSB to 010_1111: 95LSB to 111_1111: 255LSB (2LSB step)						
0x26	Reserved	**YPXD[6:0]**						
		Static Y-gamma correction D X axis						
INIT: 0x3F	Fix to 0	000_0000: 1LSB to 011_1111: 127LSB to 111_1111: 255LSB (2LSB step)						
0x27	Reserved	**YPYD[6:0]**						
		Static Y-gamma correction D Y axis						
INIT: 0x3F	Fix to 0	000_0000: 1LSB to 011_1111: 127LSB to 111_1111: 255LSB (2LSB step)						
0x28	Reserved	**YPXE[6:0]**						
		Static Y-gamma correction E X axis						
INIT: 0x4F	Fix to 0	000_000: 1LSB to 100_1111: 159LSB to 111_1111: 255LSB (2LSB step)						
0x29	Reserved	**YPYE[6:0]**						
		Static Y-gamma correction E Y axis						
INIT: 0x4F	Fix to 0	000_0000: 1LSB to 100_1111: 159LSB to 111_1111: 255LSB (2LSB step)						
0x2A	Reserved	**YPXF[6:0]**						
		Static Y –gamma correction F X axis						
INIT: 0x5F	Fix to 0	000_0000: 1LSB to 101_1111: 191LSB to 111_1111: 255LSB (2LSB step)						
0x2B	Reserved	**YPYF[6:0]**						
		Static Y-gamma correction F Y axis						
INIT: 0x5F	Fix to 0	000_0000: 1LSB to 101_1111: 191LSB to 111_1111: 255LSB (2LSB step)						
0x2C	Reserved	**YPXG[6:0]**						
		Static Y-gamma correction G X axis						
INIT: 0x6F	Fix to 0	000_0000: 1LSB to 110_1111: 223LSB to 111_1111: 255LSB (2LSB step)						
0x2D	Reserved	**YPYG[6:0]**						
		Static Y-gamma correction G Y axis						
INIT: 0x6F	Fix to 0	000_0000: 1LSB to 110_1111: 223LSB to 111_1111: 255LSB (2LSB step)						
0x2E	Reserved	**YPXH[6:0]**						
		Static Y-gamma correction H X axis						
INIT: 0x7F	Fix to 0	000_0000: 1LSB to 111_1111: 255LSB (2LSB step)						
0x2F	Reserved	**YPYH[6:0]**						
		Static Y-gamma correction H Y axis						
INIT: 0x7F	Fix to 0	000_0000: 1LSB to 111_1111: 255LSB (2LSB step)						

<Y static gamma correction>
It correct Y static gamma.
It is available for eight point setting and starting point is 0LSB of input and 0LSB of output.
Setting: 2LSB step



6.2.9 Sub Address 0x30 to 0x37, 0x42 to 0x4E (Dynamic Y gamma correction)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x30	Reserved	Reserved	Reserved	**DYGANMA1[4:0]**				
				Dynamic Y gamma (Dark portion) gain				
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	1_0000:*0 to 0_0000:*1 to 0_1111:*1.94 (*1/16 step)				
0x31	Reserved	Reserved	Reserved	**DYGANMA2[4:0]**				
				Dynamic Y gamma (Light portion) gain				
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	1_0000:*0 to 0_0000:*1 to 0_1111:*1.94 (*1/16 step)				
0x32	Reserved	Reserved	Reserved	Reserved	**DYGANSW[3:0]**			
					Light portion control		Dark portion control	
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	00 or 01 : Normal 10: Only gain up 11: Only gain down		00 or 01 : Normal 10: Only gain down 11: Only gain up	
0x33	**DYGA1HYST[7:0]**							
	Dead zone setting for Dynamic Y gamma (Dark portion)							
	Dark side				Light side			
INIT: 0x00	0: OFF 1: ON	000:2LSB to 111:16LSB (2LSB Step)			0: OFF 1: ON	000:2LSB to 111:16LSB (2LSB Step)		
0x34	**DYGA2HYST[7:0]**							
	Dead zone setting for Dynamic Y gamma (Light portion)							
	Dark side				Light side			
INIT: 0x00	0: OFF 1: ON	000:2LSB to 111:16LSB (2LSB Step)			0: OFF 1: ON	000:2LSB to 111:16LSB (2LSB Step)		
0x35	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x36	**CMPDLYSEL**	**COMPSW[1:0]**		Reserved	Reserved	Reserved	Reserved	Reserved
	YCCOMP select	Minus gain control						
INIT: 0x00	0: Before static gamma 1: After static gamma	00: 1/8 01: 1/4	10: 1/2 11: 1/1	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x37	Reserved	**COMPGA[6:0]**						
		YCCOMP gain						
INIT: 0x00	Fix to 0	000_0000:*0 to 111_1111:*7.9375						

DYGANMA1[4:0]: Gain control of dark portion dynamic gamma, 0x16 is recommended value.
DYGANMA2[4:0]: Gain control of light portion dynamic gamma, 0x16 is recommended value.
DYGANSW[1:0]: Direction setting for dark portion Y dynamic gamma control, 00 is recommended setting.
00 or 01: Normal operation, both Y level up and down direction.
10: Y level down direction control only
11: Y level up direction control only
DYGANSW[3:2]: Direction setting for light portion Y dynamic gamma control, 00 is recommended setting.
00 or 01: Normal operation, both Y level up and down direction.
10: Y level up direction control only
11: Y level down direction control only
DYGA1HYST[7:0]: Dead zone setting for Dark portion
DYGA2HYST[7:0]: Dead zone setting for Light portion
COMPGA[6:0]: Gain of YCCOMP
000_0000: gain less 000_0001: small gain to 111_1111: big gain
COMPSW[1:0]: Minus direction gain.
00: x1/8 01: x1/4 10: x1/2 11: x1

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x42	Reserved	Reserved	Reserved	**DYGAINTG**	Reserved	Reserved	Reserved	Reserved
				Integration of detection value				
INIT: 0x00	Fix to 0	Fix to 0	Fix to 0	0: OFF 1: ON	Fix to 0	Fix to 0	Fix to 0	Fix to 0
0x43	**DYG1DEG[2:0]**			**DYG1IRE[2:0]**			Reserved	**DYG1SW[0]**
	Dark portion detection range			Dark portion detection threshold				Dark portion D-gamma
INIT: 0x00	000: 3.63IRE to 111: 58.2IRE			000: 0 IRE to 111: 25 IRE 3.57 IRE step			Fix to 0	0: OFF 1: ON
0x44	**DYG1GAN[2:0]**			**DYG1SFT[2:0]**			Reserved	Reserved
	Dark portion gain range			Dark portion level range				
INIT: 0x00	000: 3.125% to 111: 50%			000: 0% to 111: 21.88%			Fix to 0	Fix to 0
0x45	**DYG1SPU[7:0]**							
	Rising control for Dark portion time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							
0x46	**DYG1SPD[7:0]**							
	Falling control for Dark portion time constant							
INIT: 0x00	0000_0000: Slow to 1111_1111: Fast							
0x47	**DYG2DEG[2:0]**			**DYG2IRE[2:0]**			Reserved	**DYG2SW[0]**
	Light portion detection range			Light portion detection threshold				Light portion D-gamma
INIT: 0x00	000: -3.63IRE to 111: -58.2IRE			000: 100IRE to 111: 75 IRE -3.57IRE step			Fix to 0	0: OFF 1: ON
0x48	**DYG2GAN[2:0]**			**DYG2SFT[2:0]**			Reserved	Reserved
	Light portion gain range			Light portion level range				
INIT: 0x00	000: 3.125% to 111: 50%			000: 0% to 111: 21.88%			Fix to 0	Fix to 0
0x49	**DYG2SPU[7:0]**							
	Rising control for Light portion time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							
0x4A	**DYG2SPD[7:0]**							
	Falling control for Light portion time constant							
INIT: 0x00	0000_0000:Slow to 1111_1111: Fast							
0x4B	**DYGA_DISP[0]**	**DYGA_VST[6:0]**						
	Detection area limit	Vertical start position of detection area for dynamic Y-gamma						
INIT: 0x00	0: OFF 1: ON	000_0000: 1st line to 111_1111: 509th line 4line step						
0x4C	**DYGA_DISP[1]**	**DYGA_VWD[6:0]**						
	Display the detect area (dark portion)	Vertical width of detection area for dynamic Y-gamma						
INIT: 0x00	0: OFF 1: ON	000_0000: 0Line to 111_1111: 508Lines 4line step						
0x4D	**DYGA_DISP[2]**	**DYGA_HST[6:0]**						
	Display the detect area (light portion)	Horizontal start position of detection area for dynamic Y-gamma						
INIT: 0x00	0: OFF 1: ON	000_0000: 1st clk to 111_1111: 1017th clk 8clk step						
0x4E	Reserved	**DYGA_HWD[6:0]**						
		Horizontal width of detection area for dynamic Y-gamma						
INIT: 0x00	Fix to 0	000_0000: 0clk to 111_1111: 1016clks 8clk step						

6.2.10 A setting of dynamic Y gamma

Segment 0x01

Sub Addr.	Recommended data value	functions	Remarks
0x42	0x10	Detection mode setting	DYGAINTG: 1 is recommended
0x43	0xE1	Dark portion dynamic gamma setting 1	If dark portion function tern to OFF, then the data change to 0xE0
0x44	0xE0	Dark portion dynamic gamma setting 2	-
0x45	0x90	Dark portion control rising time constant	Please set the same value in 0x45 and 0x46.
0x46	0x90	Dark portion control falling time constant	
0x47	0xF1	Light portion dynamic gamma setting 1	If light portion function tern to OFF, then the data change to 0xF0
0x48	0xFC	Light portion dynamic gamma setting 2	-
0x49	0x88	Light portion control rising time constant	Please set the same value in 0x49 and 0x4A.
0x4A	0x88	Light portion control falling time constant	

6.2.11 Detection area for dynamic Y-gamma correction

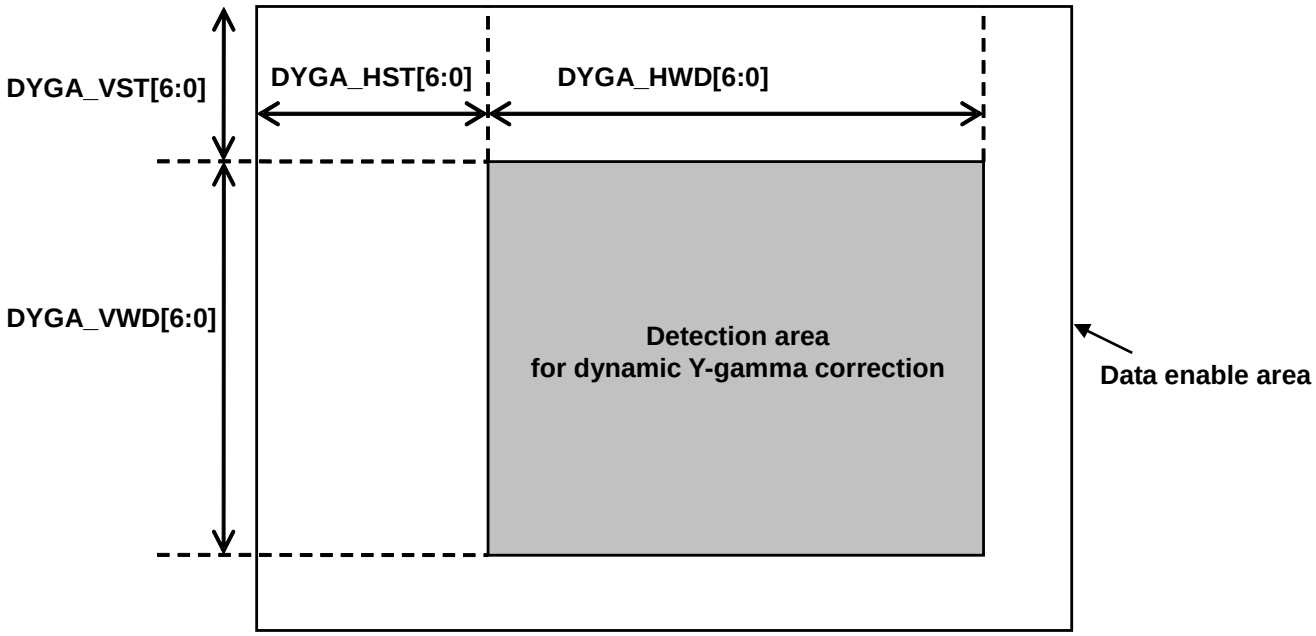
The setting for detection area of dynamic Y-gamma correction at Segment 0x01 0x4B to 0x4E.

DYGA_DISP[0]: Detection area limit of dynamic Y-gamma correction function ON/OFF
0: OFF 1: ON

DYGA_DISP[1]: Display detection area of dark portion
0: OFF 1: ON
If setting is ON, setting area of DYGA_VST[6:0], DYGA_VWD[6:0], DYGA_HST[6:0], DYGA_HWD[6:0] becomes to darkness.

DYGA_DISP[2]: Display detection area of light portion
0: OFF 1: ON
If setting is ON, setting area of DYGA_VST[6:0], DYGA_VWD[6:0], DYGA_HST[6:0], DYGA_HWD[6:0] becomes to lightness.

DYGA_VST[6:0], DYGA_VWD[6:0], DYGA_HST[6:0], DYGA_HWD[6:0]
The detection area setting for dynamic Y-gamma control.
Please refer to the following figure about each setting



6.2.12 Sub Address 0x38 to 0x39 (Mute level setting)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x38	**MUTE_Y(G)**							
	Mute level setting(G or Y)							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB (8bit, 1LSB step)							
0x39	**MUTE_CR(R)**				**MUTE_CB (B)**			
	Mute level setting(R or Cr)				Mute level setting (B or Cb)			
INIT: 0x00	<R> 0000:0LSB to 1111:255LSB <Cr> 1000:-128LSB to 0000:0LSB to 0111:127LSB (8bit, 1LSB step)				<B> 0000:0LSB to 1111:255LSB <Cb> 1000:-128LSB to 0000:0LSB to 0111:127LSB (8bit, 1LSB step)			

6.2.13 Sub Address 0x6B to 0x7E (Masking for Picture quality improver)

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x6B	**MASK0_ON**	**MASK0_XOR**	**MASK0_HST[9:8]**		**MASK0_HWD[9:8]**		**MASK0_ VST[8]**	**MASK0_ VWD[8]**
	MASK0 ON	MASK0 Mask polarity	MASK0 Horizontal start position		MASK0 Horizontal width		MASK0 Vertical start position	MASK0 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x6C	**MASK0_HST[7:0]**							
	MASK0 Horizontal start position							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023 ck)							
0x6D	**MASK0_HWD[7:0]**							
	MASK0 Horizontal width							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023ck)							
0x6E	**MASK0_VST[7:0]**							
	MASK0 Vertical start position							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512 line)							
0x6F	**MASK0_VWD[7:0]**							
	MASK0 Vertical width							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512Line)							

Segment 0x01

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x70	**MASK1_ON**	**MASK1_XOR**	**MASK1_HST[9:8]**		**MASK1_HWD[9:8]**		**MASK1_ VST[8]**	**MASK1_ VWD[8]**
	MASK1 ON	MASK1 Mask polarity	MASK1 Horizontal start position		MASK1 Horizontal width		MASK1 Vertical start position	MASK1 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x71	**MASK1_HST[7:0]**							
	MASK1 Horizontal start position							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023 ck)							
0x72	**MASK1_HWD[7:0]**							
	MASK1 Horizontal width							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023ck)							
0x73	**MASK1_VST[7:0]**							
	MASK1 Vertical start position							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512 line)							
0x74	**MASK1_VWD[7:0]**							
	MASK1 Vertical width							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512Line)							
0x75	**MASK2_ON**	**MASK2_XOR**	**MASK2_HST[9:8]**		**MASK2_HWD[9:8]**		**MASK2 _VST[8]**	**MASK2 _VWD[8]**
	MASK2 ON	MASK2 Mask polarity	MASK2 Horizontal start position		MASK2 Horizontal width		MASK2 Vertical start position	MASK2 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x76	**MASK2_HST[7:0]**							
	MASK2 Horizontal start position							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023 ck)							
0x77	**MASK2_HWD[7:0]**							
	MASK2 Horizontal width							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023ck)							
0x78	**MASK2_VST[7:0]**							
	MASK2 Vertical start position							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512 line)							
0x79	**MASK2_VWD[7:0]**							
	MASK2 Vertical width							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512Line)							
0x7A	**MASK3_ON**	**MASK3_XOR**	**MASK3_HST[9:8]**		**MASK3_HWD[9:8]**		**MASK3 _VST[8]**	**MASK3 _VWD[8]**
	MASK3 ON	MASK3 Mask polarity	MASK3 Horizontal start position		MASK3 Horizontal width		MASK3 Vertical start position	MASK3 Vertical width
INIT: 0x00	0: OFF 1: ON	0: Normal 1: Reverse	Setting of MSB		Setting of MSB		Setting of MSB	Setting of MSB
0x7B	**MASK3_HST[7:0]**							
	MASK3 Horizontal start position							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023 ck)							
0x7C	**MASK3_HWD[7:0]**							
	MASK3 Horizontal width							
INIT: 0x00	00_0000_0000: (0 ck) to 11_1111_1111: (1023ck)							
0x7D	**MASK3_VST[7:0]**							
	MASK3 Vertical start position							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512 line)							
0x7E	**MASK3_VWD[7:0]**							
	MASK3 Vertical width							
INIT: 0x00	0_0000_0000: (1 line) to 1_1111_1111: (512Line)							

6.2.14 Sub Address 0x3C to 0x41 (APL detection)

Segment 0x01

Sub Add	D7	D6	D5	D4	D3	D2	D1	D0
0x3C	**APL_DISP[0]**	**APLVST[6:0]**						
VLT	Detection area setting	APL detection area Vertical start line						
INIT: 0x00	0: OFF 1: ON	000_0000: 1st line to 111_1111: 509th line (4Line step)						
0x3D	**APL_DISP[1]**	**APLVWD[6:0]**						
VLT	Detection area display	APL detection area Vertical width						
INIT: 0x00	0: OFF 1: ON	000_0000: 0Line to 111_1111: 508Lines (4Lines step)						
0x3E	Reserved	**APLHST[6:0]**						
VLT	Fix to 0	APL detection area Horizontal start position 000_0000: 1st ck to 111_1111: 1017th ck (8clk step)						
INIT: 0x00								
0x3F	Reserved	**APLHWD[6:0]**						
VLT	Fix to 0	APL detection area Horizontal width 000_0000: 0clk to 111_1111: 1016clks (8clks step)						
INIT: 0x00								
0x40	Reserved	Reserved	Reserved	Reserved	**APL_SW[1:0]**		Reserved	Reserved
VLT	Fix to 0	Fix to 0	Fix to 0	Fix to 0	Y input select 0*:Before Edge Enhancer 10: After Y-gamma 11: After Contrast / Brightness		Fix to 0	Fix to 0
INIT: 0x00								
0x41	**APLGAIN[7:0]**							
VLT	APL Time constant							
INIT: 0x00	0000_0000 : Slow to 1111_1111 : Fast							

6.2.15 APL detection function setting (Sub Address 0x3C to 0x41)

APL_SW[1:0]: Y signal position for APL detection
0*: Before Y edge enhancer
10: After Dynamic Y gamma
11: After Contrast/ Brightness processing

APLGAIN[7:0]: APL detection time constant setting
0000_0000: slow
1111_1111: fast

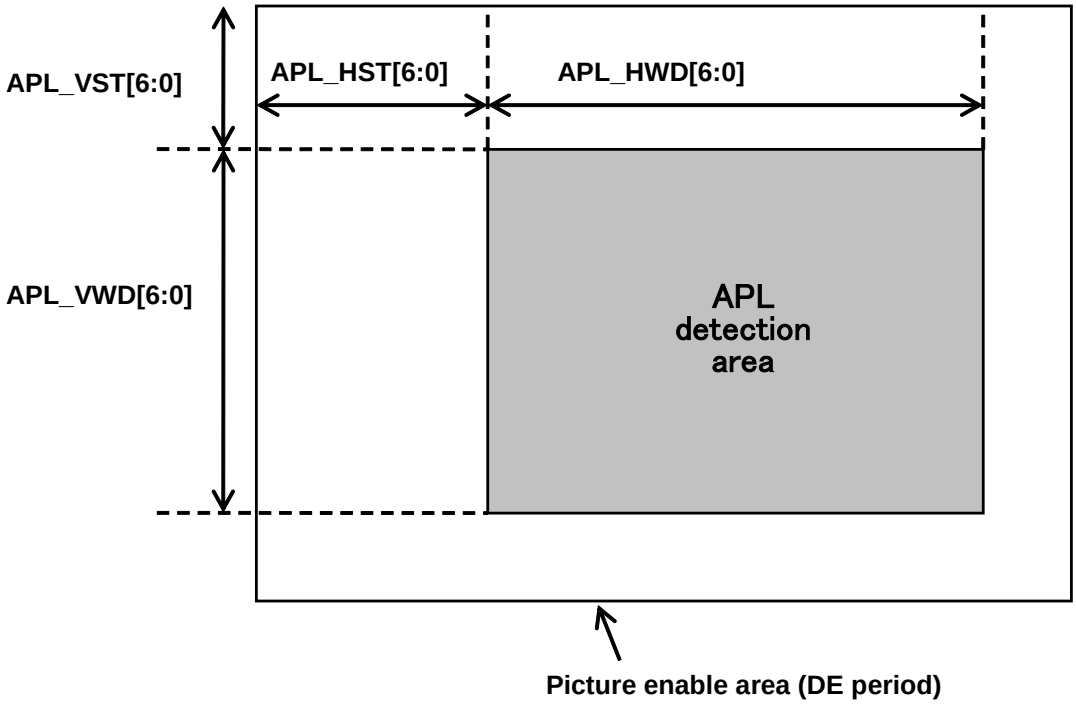
6.2.16 APL detection area limit setting (Sub Address 0x3C to 0x3F)

APL_DISP[0]: APL detection area limit setting function ON/OFF
0: OFF
1: ON

APL_DISP[1]: Display function of detection area to visible
0: OFF 1: ON

APL_VST[6:0], **DYGA_VWD[6:0]**, **DYGA_HST[6:0]**, **DYGA_HWD[6:0]**

Please refer to the following figure.



6.2.17 Sub Address 0x60 to 0x61 (APL Detection : Read data only)

Segment 0x01

Sub Add	D7	D6	D5	D4	D3	D2	D1	D0
0x60 Read Only	**RD_APLDET[11:4]**							
	APL detection value (read only)							
	0000_0000_0000:Dark to 1111_1111_1111: Light							
0x61 Read Only	**RD_APLDET[3:0]**				Reserved	Reserved	Reserved	Reserved
	0000_0000_0000:Dark to 1111_1111_1111: Light				Fix to 0	Fix to 0	Fix to 0	Fix to 0

6.3 Segment Address 0x02

6.3.1 Sub Address 0x00 (RGB-gamma correction ON/OFF, FRC/Dither)

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x00	**RGB_ GANMAON**	**GANMA_ RGBSAME**	**FRCON**	**HALF_FRC**	**FRC_PCON[1:0]**		**DITHERON**	**N_HALF**
	RGB-gamma correction		FRC	Frame process	Line process for FRC		Dither process	
	0: OFF 1: ON	0: Normal 1: RGB same setting	0: OFF 1: ON	0: 4 Frame 1: 2 Frame	00:Line process ON 01:Line process OFF 10:Line process (1/2 rate) 11:Line process (1/4 rate)		0: OFF 1: ON	0: 3bit 1: 2bit
INIT: 0x00								

6.3.2 Sub Address 0x01 to 0x06 (Adjustment in RGB signal)

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x01	**PICT_RCONT[7:0]**							
	Picture contrast (Red)							
INIT: 0x80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x02	**PICT_GCONT[7:0]**							
	Picture contrast (Green)							
INIT: 0x80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x03	**PICT_BCONT[7:0]**							
	Picture contrast (Blue)							
INIT: 0x80	0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x04	**PICT_ CNTON**	**PICT_ CONT_SAME**	**PICT_RBRT[5:0]**					
	Picture RGB contrast		Picture brightness (Red)					
	0:OFF 1:ON	0:Each signal 1:RGB same setting	10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB (8bit)					
INIT: 0x00								
0x05	**PICT_ BRTON**	**PICT_BRT_ RGBSAME**	**PICT_GBRT[5:0]**					
	Picture RGB brightness		Picture brightness (Green)					
	0:OFF 1:ON	0:Each signal 1:RGB same setting	10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB (8bit)					
INIT: 0x00								
0x06	Reserved	Reserved	**PICT_BBRT[5:0]**					
			Picture brightness (Blue)					
	Fix to 0	Fix to 0	10_0000:-32LSB to 00_0000:±0LSB to 01_1111:+31LSB (8bit)					
INIT: 0x00								

6.3.3 Sub Address 0x07 to 0x0F (Adjustment in RGB contrast and brightness)

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x07	**RCONT[7:0]**							
INIT: 0x80	RGB contrast (Red) before RGB gamma correction 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x08	**GCONT[7:0]**							
INIT: 0x80	RGB contrast (Green) before RGB gamma correction 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x09	**BCONT[7:0]**							
INIT: 0x80	RGB contrast (Blue) before RGB gamma correction 0000_0000 : x0 to 1000_0000 : x1 to 1111_1111 : x1.992							
0x0A	**CONTON**	**CONT_SAME**	**RBRT[5:0]**					
	RGB contrast before RGB gamma		RGB brightness (Red) before RGB gamma correction					
INIT: 0x00	0: OFF 1: ON	0: Each signal 1: Same	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					
0x0B	**BRTON**	**BRT_ RGBSAME**	**GBRT[5:0]**					
	RGB brightness before RGB gamma		RGB brightness (Green) before RGB gamma correction					
INIT: 0x00	0: OFF 1: ON	0: Each signal 1: Same	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					
0x0C	Reserved	Reserved	**BBRT[5:0]**					
			RGB brightness (Blue) before RGB gamma correction					
INIT: 0x00	Fix to 0	Fix to 0	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					
0x0D	**OFSTON**	**OFST _RGBSAME**	**ROFST[5:0]**					
	RGB brightness after RGB gamma		RGB brightness (Red) after RGB gamma correction					
INIT: 0x00	0: OFF 1: ON	0: Each signal 1: Same	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					
0x0E	Reserved	Reserved	**GOFST[5:0]**					
			RGB brightness (Green) after RGB gamma correction					
INIT: 0x00	Fix to 0	Fix to 0	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					
0x0F	Reserved	Reserved	**BOFST[5:0]**					
			RGB brightness (Blue) after RGB gamma correction					
INIT: 0x00	Fix to 0	Fix to 0	10_0000: -32LSB to 00_0000: ±0LSB to 01_1111: +31LSB (8bit)					

6.3.4 Sub Address 0x10 to 0x6F (RGB gamma correction)

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x10	**RPXA[7:0]**							
not VLT	R gamma A:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x11	**RPYA[7:0]**							
not VLT	R gamma A:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x12	**RPXB[7:0]**							
not VLT	R gamma B:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x13	**RPYB[7:0]**							
not VLT	R gamma B:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x14	**RPXC[7:0]**							
not VLT	R gamma C:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x15	**RPYC[7:0]**							
not VLT	R gamma C:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x16	**RPXD[7:0]**							
not VLT	R gamma D:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x17	**RPYD[7:0]**							
not VLT	R gamma D:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x18	**RPXE[7:0]**							
not VLT	R gamma E:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x19	**RPYE[7:0]**							
not VLT	R gamma E:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1A	**RPXF[7:0]**							
not VLT	R gamma F:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1B	**RPYF[7:0]**							
not VLT	R gamma F:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1C	**RPXG[7:0]**							
not VLT	R gamma G:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1D	**RPYG[7:0]**							
not VLT	R gamma G:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1E	**RPXH[7:0]**							
not VLT	R gamma H:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x1F	**RPYH[7:0]**							
not VLT	R gamma H:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x20	**RPXI[7:0]**							
not VLT	R gamma I:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x21	**RPYI[7:0]**							
not VLT	R gamma I:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x22	**RPXJ[7:0]**							
not VLT	R gamma J:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x23	**RPYJ[7:0]**							
not VLT	R gamma J:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x24	**RPXK[7:0]**							
not VLT	R gamma K:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x25	**RPYK[7:0]**							
not VLT	R gamma K:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x26	**RPXL[7:0]**							
not VLT	R gamma L:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x27	**RPYL[7:0]**							
not VLT	R gamma L:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x28	**RPXM[7:0]**							
not VLT	R gamma M:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x29	**RPYM[7:0]**							
not VLT	R gamma M:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2A	**RPXN[7:0]**							
not VLT	R gamma N:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2B	**RPYN[7:0]**							
not VLT	R gamma N:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2C	**RPXO[7:0]**							
not VLT	R gamma O:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2D	**RPYO[7:0]**							
not VLT	R gamma O:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2E	**RPXP[7:0]**							
not VLT	R gamma P:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x2F	**RPYP[7:0]**							
not VLT	R gamma P:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x30	**GPXA[7:0]**							
not VLT	G gamma A:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x31	**GPYA[7:0]**							
not VLT	G gamma A:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x32	**GPXB[7:0]**							
not VLT	G gamma B:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x33	**GPYB[7:0]**							
not VLT	G gamma B:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x34	**GPXC[7:0]**							
not VLT	G gamma C:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x35	**GPYC[7:0]**							
not VLT	G gamma C:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x36	**GPXD[7:0]**							
not VLT	G gamma D:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x37	**GPYD[7:0]**							
not VLT	G gamma D:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x38	**GPXE[7:0]**							
not VLT	G gamma E:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x39	**GPYE[7:0]**							
not VLT	G gamma E:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3A	**GPXF[7:0]**							
not VLT	G gamma F:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3B	**GPYF[7:0]**							
not VLT	G gamma F:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3C	**GPXG[7:0]**							
not VLT	G gamma G:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3D	**GPYG[7:0]**							
not VLT	G gamma G:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3E	**GPXH[7:0]**							
not VLT	G gamma H:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x3F	**GPYH[7:0]**							
not VLT	G gamma H:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x40	**GPXI[7:0]**							
not VLT	G gamma I:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x41	**GPYI[7:0]**							
not VLT	G gamma I:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x42	**GPXJ[7:0]**							
not VLT	G gamma J:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x43	**GPYJ[7:0]**							
not VLT	G gamma J:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x44	**GPXK[7:0]**							
not VLT	G gamma K:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x45	**GPYK[7:0]**							
not VLT	G gamma K:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x46	**GPXL[7:0]**							
not VLT	G gamma L:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x47	**GPYL[7:0]**							
not VLT	G gamma L:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x48	**GPXM[7:0]**							
not VLT	G gamma M:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x49	**GPYM[7:0]**							
not VLT	G gamma M:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4A	**GPXN[7:0]**							
not VLT	G gamma N:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4B	**GPYN[7:0]**							
not VLT	G gamma N:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4C	**GPXO[7:0]**							
not VLT	G gamma O:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4D	**GPYO[7:0]**							
not VLT	G gamma O:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4E	**GPXP[7:0]**							
not VLT	G gamma P:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x4F	**GPYP[7:0]**							
not VLT	G gamma P:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x50	**BPXA[7:0]**							
not VLT	B gamma A:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x51	**BPYA[7:0]**							
not VLT	B gamma A:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x52	**BPXB[7:0]**							
not VLT	B gamma B:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x53	**BPYB[7:0]**							
not VLT	B gamma B:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x54	**BPXC[7:0]**							
not VLT	B gamma C:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x55	**BPYC[7:0]**							
not VLT	B gamma C:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x56	**BPXD[7:0]**							
not VLT	B gamma D:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x57	**BPYD[7:0]**							
not VLT	B gamma D:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x58	**BPXE[7:0]**							
not VLT	B gamma E:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x59	**BPYE[7:0]**							
not VLT	B gamma E:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5A	**BPXF[7:0]**							
not VLT	B gamma F:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5B	**BPYF[7:0]**							
not VLT	B gamma F:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5C	**BPXG[7:0]**							
not VLT	B gamma G:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5D	**BPYG[7:0]**							
not VLT	B gamma G:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5E	**BPXH[7:0]**							
not VLT	B gamma H:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x5F	**BPYH[7:0]**							
not VLT	B gamma H:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x60	**BPXI[7:0]**							
not VLT	B gamma I:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x61	**BPYI[7:0]**							
not VLT	B gamma I:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x62	**BPXJ[7:0]**							
not VLT	B gamma J:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x63	**BPYJ[7:0]**							
not VLT	B gamma J:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x64	**BPXK[7:0]**							
not VLT	B gamma K:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x65	**BPYK[7:0]**							
not VLT	B gamma K:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x66	**BPXL[7:0]**							
not VLT	B gamma L:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x67	**BPYL[7:0]**							
not VLT	B gamma L:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x68	**BPXM[7:0]**							
not VLT	B gamma M:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x69	**BPYM[7:0]**							
not VLT	B gamma M:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6A	**BPXN[7:0]**							
not VLT	B gamma N:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6B	**BPYN[7:0]**							
not VLT	B gamma N:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6C	**BPXO[7:0]**							
not VLT	B gamma O:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6D	**BPYO[7:0]**							
not VLT	B gamma O:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6E	**BPXP[7:0]**							
not VLT	B gamma P:X axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x6F	**BPYP[7:0]**							
not VLT	B gamma P:Y axis							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							

<RGB gamma correction>
This function is RGB gamma correction for each R,G and B.
Setting: 1LSB step, 16 points

Notes: The registers of RGB gamma correction don't have V latch process. Thus, when the registers of this function is changed, the mute process is needed.

6.3.5 Sub Address 0x70 (Fade-in, Fade-out)

Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x70	**FDOUTON**	**FDOTIME[2:0]**			**FDINON**	**FDITIME[2:0]**		
	Fade Out				Fade IN			
INIT: 0x00	0:OFF 1:ON	000:8V to 111:128V			0:OFF 1:ON	000:8V to 11:128V		

6.3.6 Sub Address 0x74 to 0x76 (Blue back level)

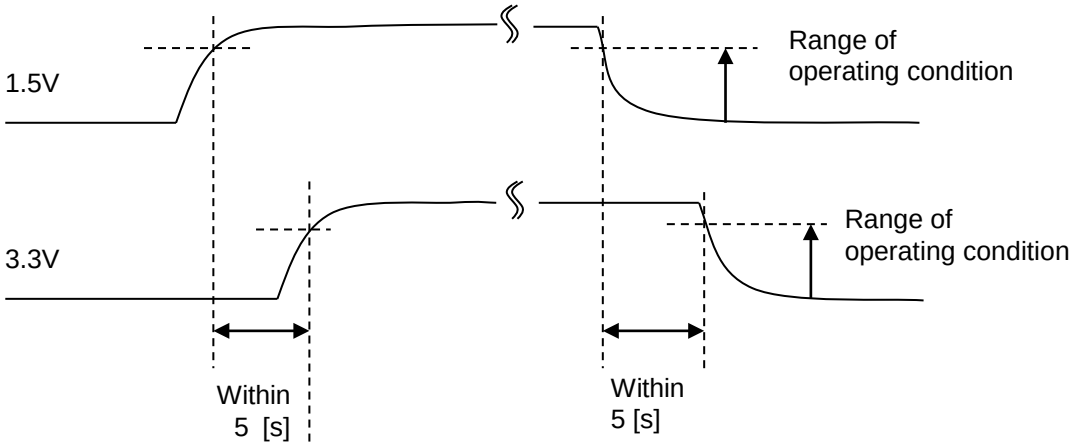
Segment 0x02

Sub	D7	D6	D5	D4	D3	D2	D1	D0
0x74	**BBACK_R(CR)[7:0]**							
	Red level for Blue back							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x75	**BBACK_G(Y)[7:0]**							
	Green level for Blue back							
INIT: 0x00	0000_0000:0LSB to 1111_1111:255LSB							
0x76	**BBACK_B(CB)[7:0]**							
	Blue level for Blue back							
INIT: 0xC0	0000_0000:0LSB to 1100_0000:192LSB to 1111_1111:255LSB							

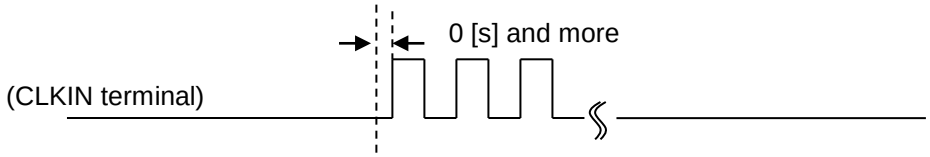
7. Control condition for Power ON and OFF

This section is critical to the reliability assurance of the IC.
Read it carefully before setting power-on/off control, reset control and I²C Bus control timing settings.

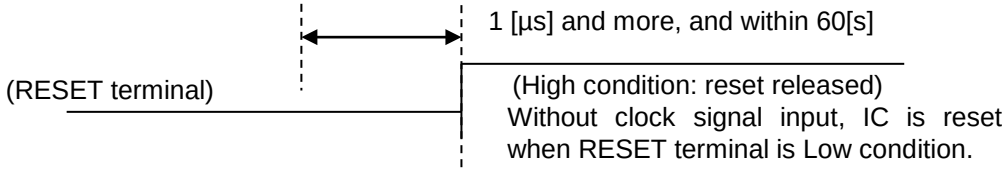
(1) Power ON/OFF
Supply voltage are 1.5V and 3.3V.
The order of power-on and power-off of 2-system VDD is good with random order.
However, please complete power-on and power-off of 2-system VDD within 5 [s].



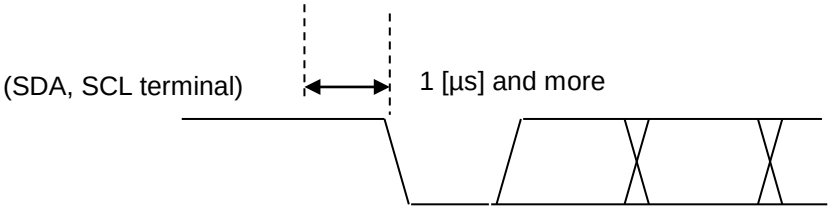
(2) Clock input
Clock signal is inputted
after operating condition for 3.3V
supply voltage.



(3) Reset
Keep the RESET state for at
least 1 [µs] once all 2 system
power have reached operating
condition power voltage.
The maximum period for
retaining the RESET state is
60 [s].



(4) I²C Bus
Start the I²C Bus control 1 [µs] or more
after inputting clock and releasing the RESET.



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