# TB67H301FTG

# Usage considerations


## Summary

The TB67H301FTG is a full-bridge DC motor driver with DMOS output transistors.

The low ON-resistance DMOS process and PWM control enables driving DC motors with high thermal efficiency.

Four operating modes are selectable via IN1 and IN2: clockwise (CW), counterclockwise (CCW), Short Brake and Stop.

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# 1. Differences between stop mode and standby mode of the TB67H301FTG

The TB67H301FTG can use the standby mode with STBY pin
As for the stop mode, the response speed from the state of output off to the state of output on of the forward and reverse direction operation is faster than standby mode. However, it cannot be released forcedly while protection functions (ISD and TSD) are enabled because the power supply current is larger than that of the standby mode.

**Table 1 Comparison of the characteristics and functions of standby mode and stop mode**

| Mode | Standby mode | Stop mode |
|---|---|---|
| Power supply current of VM pin | 1 μA (max) | 1.3 mA (typ.) |
| Power supply current of VCC pin | 1 μA (max) | 3 mA (typ.) |
| Response time | 16 μs (typ.) | 0.26 μs (typ.) |
| Release in protection function ON | ISD and TSD | No |

# 2. Power supply voltage

## (1) Operating power supply voltage range

The power supply voltage of VCC and VM are necessary.
The absolute maximum rating of VM is 40 V. However, the operating supply voltage should be within the range of 4.5 V to 38 V when it is actually used.
The absolute maximum rating of VCC is 6 V. However, the operating supply voltage should be within the range of 3.0 V to 5.5 V when it is actually used. In using constant current PWM control, VCC should be used within the range between 4.5 and 5.5 V.

## (2) Power ON/Power OFF

Though two power supplies of VCC and VM are necessary, the TB67H301FTG has no special procedures for turning on and off itself because the undervoltage lockout circuit (LVD) is incorporated. However, if the motor operates under the condition that the power supply voltage is unstable, the motor current is consumed, and the voltage cannot reach the specified power supply voltage. Then, the stable power supply voltage is not supplied and results in abnormal IC operations.
Therefore, it is recommended to run the motor after ensuring the IC turns on with the stable power supply in the state of output off. Then the motor rotational direction should be controlled by switching the inputs.
It is likewise recommended to turn off the IC after the motor movement is completely stopped.

# 3. Output current

Note that the absolute maximum output current rating of OUT1 and OUT2 must be kept under 3 A.
Also, the usage conditions such as the ambient temperature, presence or absence of a heatsink, board layout and IC mount technique have effect on increase and decrease of the available average output current. The TB67H301FTG must be used with the absolute maximum output current rating of 3 A when Tj = 150°C.

# 4. Control inputs

Even if there are pulse inputs to IN1, IN2, STBY, and VREF, they never seep into the power supply as long as VCC and VM power supply are turned off; therefore the TB67H301FTG will never be turned on.
Though it is in the standby mode, in case of High input with the lower voltage than the voltage of VCC pin or Low input with the higher voltage than the voltage of SGND pin, the power supply current of the VCC pin may increase to 1 μA or more.
For example, when the power supply voltage of VCC pin=5 V, control input: High = 3.3 V and STBY pin: Low = 0 V (standby mode), other inputs (IN1, IN2, and PWM pin): High = 3.3 V, then the power supply current of VCC pin becomes 1 μA or more.
So, it is recommended that the control input is configured same as the voltage of VCC, and other inputs are controlled to ground level in the standby mode. To release TSD and ISD, standby mode should be continued for 10 μs or more.

## 5. PWM control

The PWM input through the IN1 and IN2 pins controls the motor speed.

The IC internally generates the blank time when the upper and lower power transistors in the output circuit switch on and off so as to prevent the shoot-through current that occurs otherwise on overlap of the ON states of the upper and lower power transistors.

Therefore, the PWM control with the synchronous rectification is available without externally off time input.

Though the reference PWM frequency in the operational range is stated as 100 kHz, in actual operations, the output voltage may be distorted to the input even when the IC operates within the operating range as shown in the switching characteristics below.

The TB67H301FTG can support the frequency of over 100 kHz only as far as its output distortions to the inputs and the duty gaps are taken into account when it is used.

Note that the values of the following switching characteristics are given as typical values. The IC must be used with a sufficient safety margin because they vary with power supply voltages, temperatures, and IC variation.

### (1) Switching characteristics

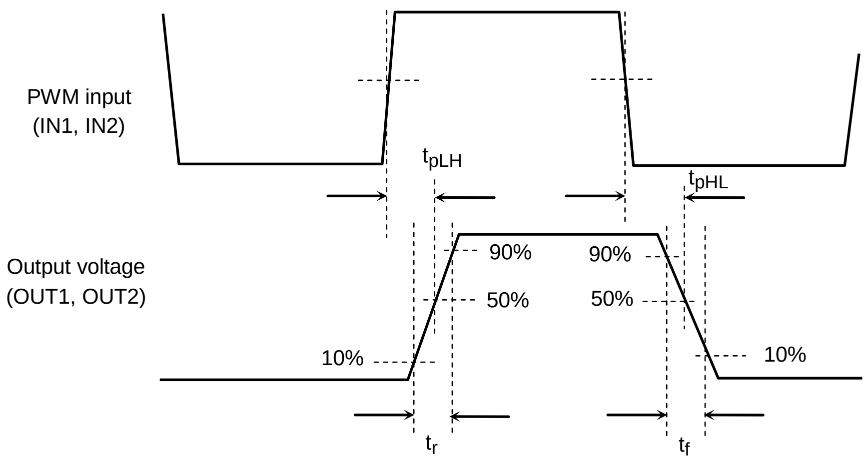



**Figure 1 Switching characteristics**

**Table 2 Switching characteristics**

Ta = 25°C ,VM = 24 V, VCC = 5 V, and No load

| Characteristics | Typ. value (for reference) | Unit |
|---|---|---|
| $t_{pLH}$ | 260 | ns |
| $t_{pHL}$ | 260 | |
| $t_r$ | 50 | |
| $t_f$ | 50 | |

Note 1: IN1/IN2 pin: IN1=IN2=HIGH; Short brake
IN1 = Low, IN2 = High or IN1 = Low, IN2 = High; Normal operation
Switching operation: low input of normal operation

Note 2: When the signal is input to IN1 (IN2) pin, it is recommended to provide intr and intf more than 10ns in order to avoid malfunction because of the input switching noise. For example, please connect the capacitor between IN1 (IN2) pin and GND.

## 6. Function table

**Figure 2 Function table of the TB67H301FTG**

| Input | | | Output | | | | Mode |
|---|---|---|---|---|---|---|---|
| STBY | IN1 | IN2 | OUT1 | OUT2 | ALERT | PSW | |
| H | H | H | L | L | L | H | Short brake |
| | L | H | L | H | L | H | Reverse (CCW)/Forward (CW) |
| | H | L | H | L | L | H | Forward (CW)/Reverse (CCW) |
| | L | L | OFF (Hi-Z) | OFF (Hi-Z) | L | H | Stop |
| L | — | — | OFF (Hi-Z) | OFF (Hi-Z) | OFF (Hi-Z) | OFF (Hi-Z) | Standby |

## 7. Application circuit example

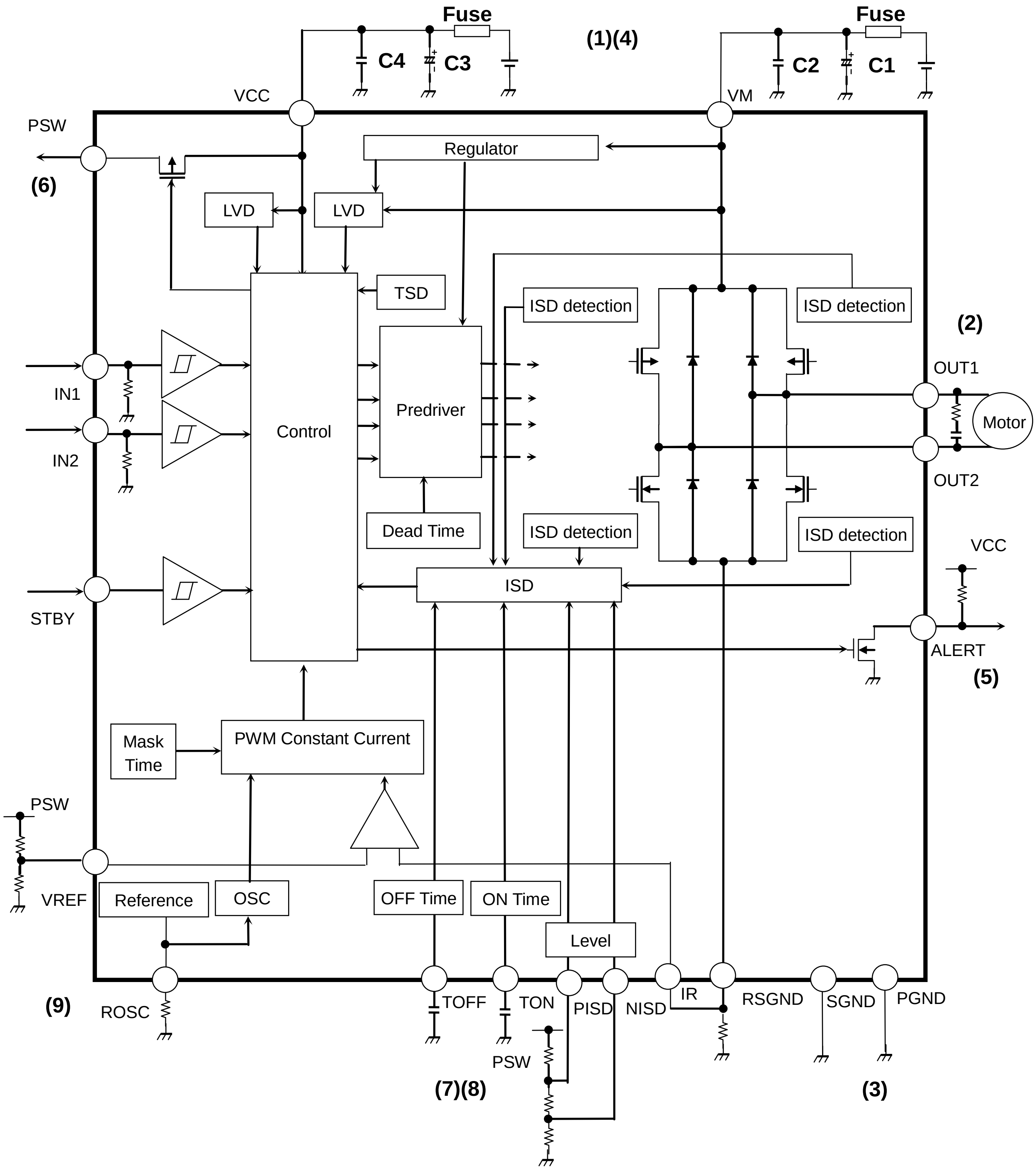



**Figure 3 Application circuit example**

### (1) Capacitors connected to the power supply pin

Connect the appropriate capacitor not to cause malfunction of the IC by the variation of the power supply and noise.

Connect the capacitors between VM and GND, and between VCC and GND as close to the IC as possible. Especially, the ceramic capacitor can reduce the variation of the power supply at the high frequency and the noise by connecting as close to the IC as possible.

**Table 3 Recommended Values**

| Characteristics | Symbol | Recommended Value | Remarks |
|---|---|---|---|
| VM – GND | C1 | 10 μF to 100 μF | Electrolytic capacitor |
| | C2 | 0.001 μF to 1 μF | Ceramic capacitor |
| VCC – GND | C3 | 1 μF to 10 μF | Electrolytic capacitor |
| | C4 | 0.001 μF to 1 μF | Ceramic capacitor |

In case the load of the motor is small and the variation of the power supply is almost nothing, electrical capacitor can be omitted and other capacitors which are not recommended can be used.

### (2) Capacitor and resistor between outputs

Connect the R1 resistor and the C3 capacitor only for removing the brush noise of the motor. If so, limit the current by using R1 because the outputs momentarily move to the short circuit mode when C3 is not charged. In case there is no influence of brush noise of the motor, they can be omitted.

### (3) Wiring of VM, VCC, OUT1, OUT2, RSGND, SGND, and PGND

The motor causes a large current flow through the TB67H301FTG. Therefore, sufficient space must be secured on designing the IC wiring pattern. Particularly for RSGND, SGND, and PGND, a space large enough for their connections to GND must be secured so as not to be affected by wiring impedance.

Design the pattern in considering the heat design because the back side of the IC has a role of heat radiation. (The back side should be connected to GND because it is connected to the backside chip electrically.)

### (4) Fuse

For preventing a continuous flow of a large current due to overcurrent or IC damages, an appropriate fuse must be placed in the power supply of the IC.

The IC may fail because of illegal use such as exceeding the absolute maximum ratings, incorrect wirings and abnormal pulse noise induced by wirings and loads. As a result, a large current continuously flows into the IC leads to smoking and ignition. To make these negative impacts as small as possible, appropriate control of the capacitance and weld time of the fuse as well as positioning of the fuse in the circuit is required.

The IC incorporates an overcurrent detection circuit (ISD). However, it does not necessarily protect the IC in any case. On activation of the ISD circuit, overcurrent conditions must be removed immediately. Depending on the usage and the use environment of the IC, like using it with the absolute maximum ratings being exceeded, the ISD circuit may not operate correctly; or the IC may be broken before the ISD circuit is activated. Even after the activation of the ISD circuit, the IC may be destroyed due to the IC heating if overcurrent continues flowing too long.

There is a concern that a secondary destruction of the IC due to continuous overcurrent may occur. Another concern is that the ISD circuit may not run due to its blank time, interacting with the output load conditions. Toshiba, therefore, describes in the specification that the ISD circuit does not necessarily run in any case as one of the usage considerations.

For instance, if a current that neither reaches the absolute maximum output current rating nor infringes the lower limit of the operating voltage of the ISD circuit continues flowing, the DMOS transistors in the output stage will be degraded. On the other hand, if once a current exceeding the absolute maximum output current rating flows into the DMOS transistors in the output stage, they are degraded as well. Therefore, even though the IC is not broken after single overcurrent detection, it may be broken after two or three times of overcurrent detection because repeated detections will deepen the DMOS degradation.

Toshiba recommends the use of a fuse in the power supply to cope with such a secondary destruction.

### (5) ALERT pin

The ALERT pin behaves as an open-drain output. It outputs high signal by connecting it to the pull-up resistor externally in the high impedance state.

In normal operation, it outputs low. In the standby mode, the thermal shutdown (TSD) circuit mode, the over current detection (ISD) circuit mode, and the undervoltage lockout (LVD) circuit mode, it is in the high impedance state and outputs high signal. Recommended pull-up resistor is between 10 kΩ and 100 kΩ. When ALERT pin is not used, it should be configured open or connected to GND.

### (6) PSW pin

The PSW pin behaves as an open-drain output. It outputs the voltage of VCC pin in the normal operation.

In the standby mode and the undervoltage lockout (LVD) circuit mode, it is in the high impedance state.

Waiting power is reduced by using it as a configured voltage of the external parts because the operation is synchronized with the standby mode.

So, use it as a configured voltage for PISD, NISD, and VREF pins.

### (7) Setting TON pin and TOFF pin

As for configuration of over current detection (ISD), TON pin can set detection time (ton) with the capacitor. TOFF pin can set stop time (toff) that corresponds to the period the operation returns automatically from the stop mode by the capacitor. They can be configured from following formulas.

ton(s) = 1.14×C×10 ˆ 4
toff(s) = C×10 ˆ 6
.

Latch mode can also be configured not to return operation automatically after over current detection. TOFF pin is connected to GND. It is released by setting standby mode to return to the normal operation.

Note 1: Configure the TON pin with the capacitor whose range is from 100 pF to 10 nF. Sufficient safety margin must be secured because an approximate calculation and an actual measured value have a tolerance.

Note 2: Configure the TOFF pin with the capacitor whose range is from 0.47 nF to 10 μF. Sufficient safety margin must be secured because an approximate calculation and an actual measured value have a tolerance.

Note 3: When the capacitor is connected to TOFF pin and the IC operates in the auto return mode, The IC may turn on and off repeatedly influenced by noise which is generated from large current detected by the over current detection circuit. So, it is recommended to use the IC in the latch mode. In case of using the IC in auto return mode, please evaluate it enough before using.

### (8) Setting PISD pin and NISD pin

One ISD detection feature is provided for each of the four output power transistors.

By setting the input voltage of the NISD pin and the PISD pin, the detection current can be set.

The setting values of Nch side and Pch side of the output power transistor have a small difference. Nch side can be set by NISD pin and Pch side can be set by PISD pin. As for Pch side, setting values of OUT1 and OUT 2 have a small difference.

There is no problem to use the IC by setting the voltages of PISD pin and NISD pin same if this small difference is allowed.

Please configure them by referring to the figure below.

Pay attention not to use the IC under the condition as follows; Setting voltage is 0.5 V or less and 3.5 V or more.

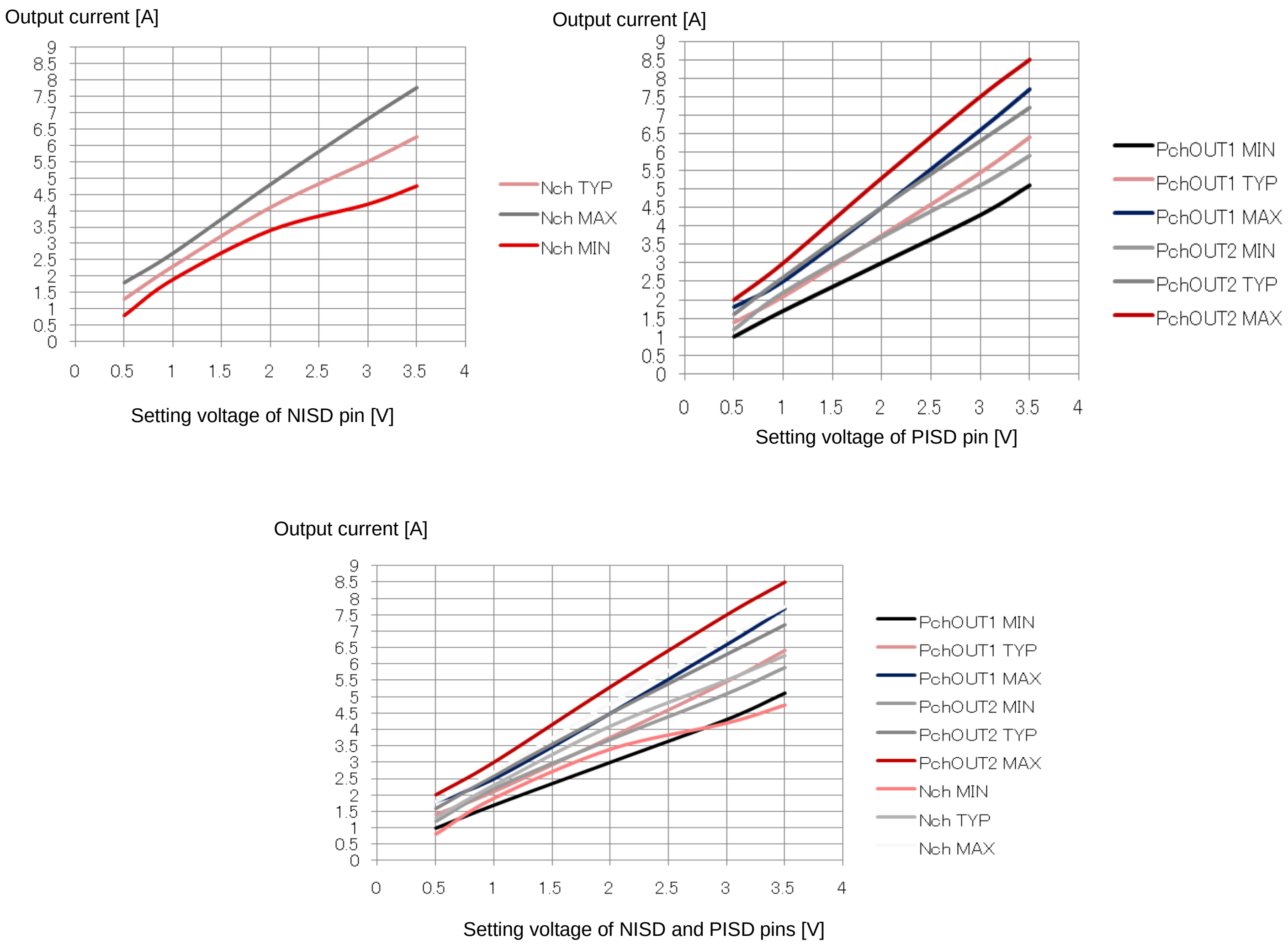



**Figure 4 Setting PISD pin and NISD pin**

In operating, there is a possibility that the current exceeds the absolute maximum ratings. It is an auxiliary circuit. It does not protect the IC from any over current caused by short-circuiting to the power supply, ground, or the load.

### (9) Calculations for Constant Current PWM Control of the RSGND and VREF Pins

The peak current in the constant current operation is determined by inputting the voltage to VREF pin. The peak current is calculated from the following equation.

IO = VREF/Rrsgnd [A] For example, when Rrsgnd = 0.2 Ω and VREF = 0.2 V, IO = 1 A.

After reaching the peak current, the IC operation moves to the constant current PWM drive mode by operating for the short-brake (discharge) time, which is determined by OSC frequency. OSC frequency can be configured by the resistance (Rosc) of ROSC pin.

The oscillation frequency is approximated by the following equation:

fosc [Hz] (typ.) = (24 × 10 ^ 10)/Rosc [Hz]

Short-brake time is calculated from the time equivalent to 39 counts adding the analog delay time. By the way, one count corresponds to quarter cycle of OSC frequency.

Minimum ON duty of the constant current PWM control corresponds to the minimum charge width. It is calculated from the time equivalent to 13 counts adding the analog delay time. By the way, one count corresponds to one cycle of OSC frequency.

Short-brake time = 4/fosc × 39 counts + A  A: Analog delay time (400 ns (typ.)

Minimum charge width = 1/fosc × 13 counts + B  B: Analog delay time (350 ns (typ.)

Example: When Rosc = 24 kΩ, fosc = 10 MHz. Then, short-brake time = 16 μs (typ.) and minimum charge width = 1.7 μs (typ.).

In case the IC does not operate with constant current PWM control, short-circuit VREF pin to PSW pin or VCC pin, and short-circuit RSGND pin to SGND pin without connecting the resistor of Rrsgnd. And ROSC pin should be connected to GND pin with the resistor of 24kΩ though the constant current PWM is not enabled.

Note 1: Use the IC by using Rosc whose range is from 12kΩ to 50kΩ because the approximate calculation and the actual measured value have a small tolerance shown in the below figure.

Note 2: If OSC frequency is configured too high, the switching loss of the output stages controlled by the PWM frequency becomes larger. However, note that if the OSC frequency is too low, the PWM frequency may fall within the audible range. Sufficient safety margin must be secured because the PWM frequency varies with the power supply voltage, temperature and IC variation.

Note 3: The voltage of RSGND pin should be 0.5 V or less though the current flows in the resistor of Rrsgnd.

Note 4: Detection resistance should be located close to RSGND pin and SGND pin not to be influenced by wire impedance because the voltage generated in the detection resistor is compared to the voltage of SGND pin (typ.).

Note 5: Sufficient safety margin must be secured for wire pattern not to have wire impedance because if wire impedance generates between RSGND pin and SGND pin, the resistance leads the constant current PWM drive like the detection resistance.

Note 6: In the constant current PWM control, though the current (IO) is tried to set small, minimum charge width is PWM controlled and the current is charged. So, if the voltage of 0 V is inputted to VREF pin, IO cannot be controlled to 0 A.

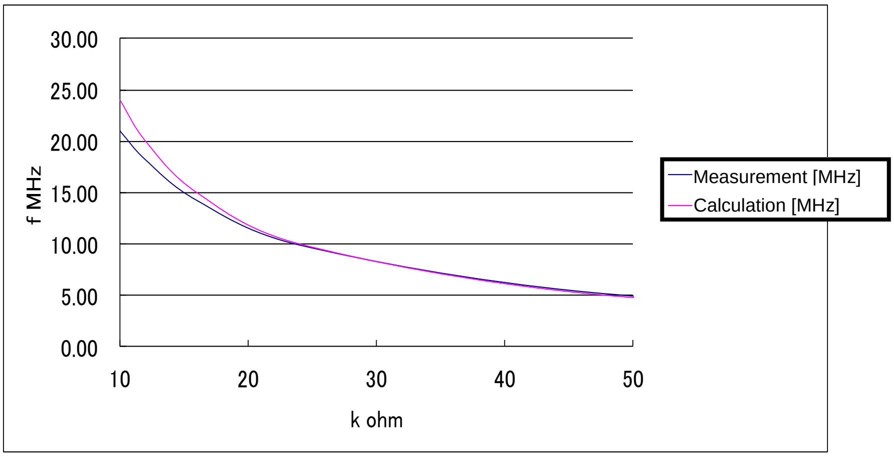



**Figure 5 Calculations for Constant Current PWM Control of the RSGND and VREF Pins**

**Example: Application circuit (ISD/TSD latch mode): Using the constant current PWM drive, output current: 0.93A (peak)**

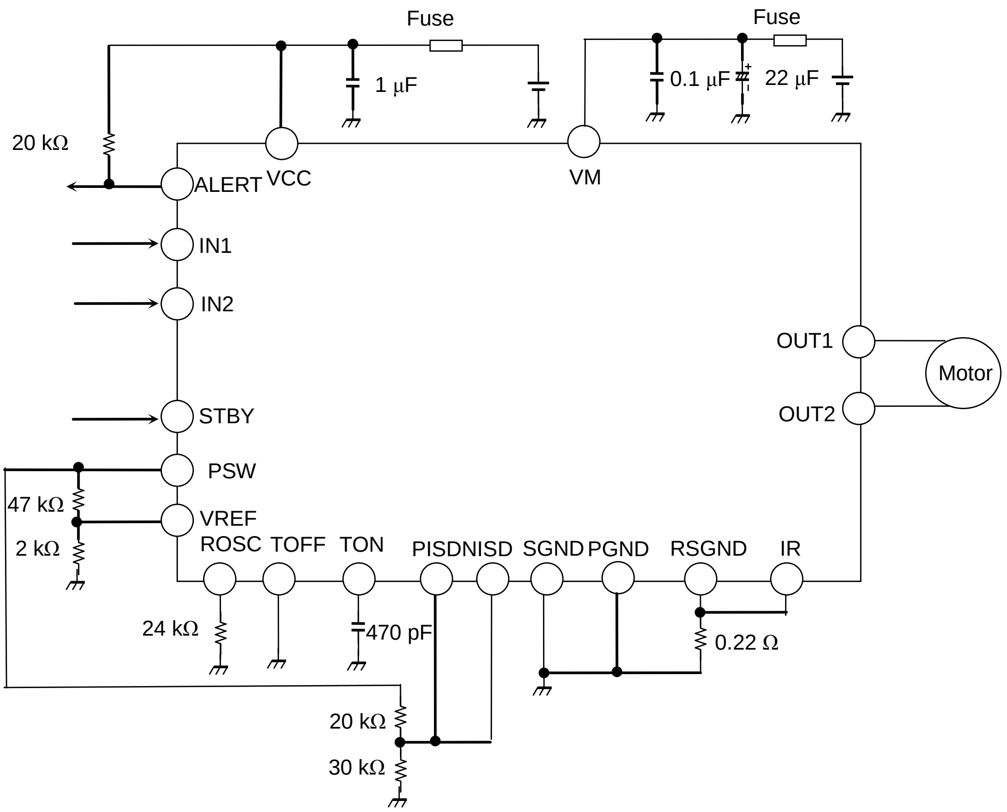



**Figure 6 Application circuit: Using the constant current PWM drive**

**Example: Application circuit (ISD/TSD latch mode): Not using the constant current PWM drive**

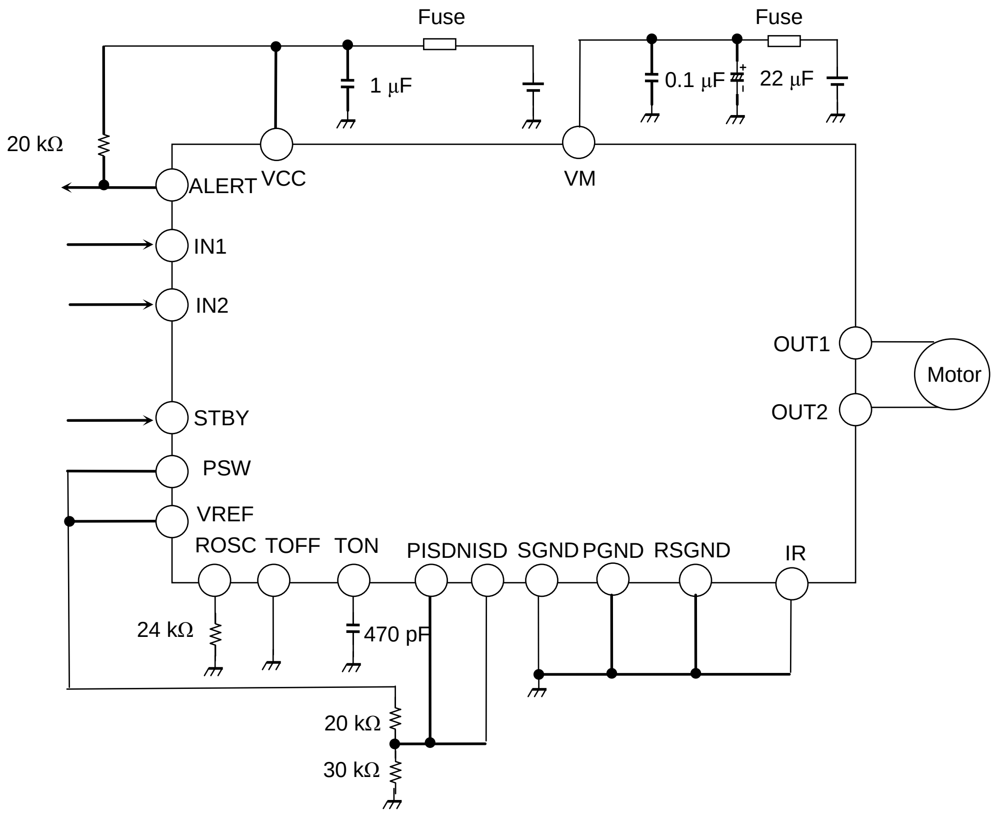



**Figure 7 Application circuit: Not using the constant current PWM drive**

# 8. Power dissipation

## (1) Calculation of power consumption

Power loss of the IC is calculated from below formula.
$P = VM \times IM + V_{CC} \times I_{CC} + I_O^2 \times (RONU + RONL)$

Example: When VM = 24 V, $V_{CC}$ = 5 V, and Output current $I_O$ = 0.5 A,
(IM, $I_{CC}$, RONU, and RONL: Refer to the data sheet, "Electrical characteristics")
P (typ.) = 24 V × 1.3 mA (typ.) + 5 V × 3 mA (typ.) + $(0.5\ A)^2$ × (0.6 Ω (typ.) + 0.4 Ω (typ.)) = 0.29 W
P (max) = 24 V × 5 mA (max) + 5 V × 7 mA (max) + $(0.5\ A)^2$ × (0.9Ω (typ.) + 0.6 Ω (typ.)) = 0.53 W

Example: VM = 24 V, $V_{CC}$ = 5 V, and output current $I_O$ = 3 A
P (typ.) = 24 V × 1.3 mA (typ.) + 5 V × 3 mA (typ.) + $(3\ A)^2$ × (0.6 Ω (typ.) + 0.4 Ω (typ.)) = 9.05 W
P (max) = 24 V × 5 mA (max) + 5 V × 7 mA (max) + $(3\ A)^2$ × (0.9 Ω (typ.) + 0.6 Ω (typ.)) = 13.66 W

## (2) Heat calculation 1

From the ambient temperature (Ta) and the thermal resistance ($R_{th\ (ja)}$), the junction temperature (Tj) is calculated from below formula.
$T_j = P \times R_{th\ (ja)} + Ta$

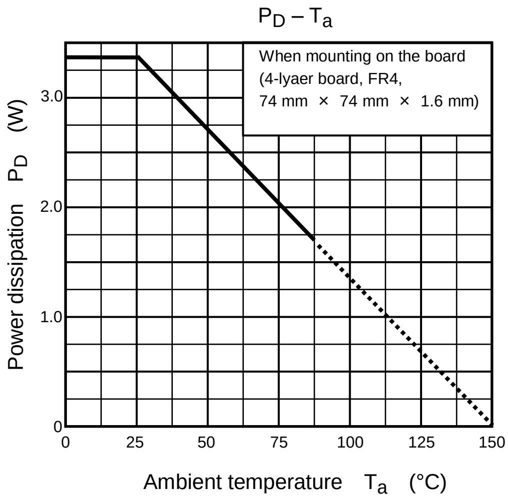
Example: In mounting board: Rth (ja) = 37.1°C/W (4-layer board, FR4, 74 mm × 74 mm × 1.6 mm)
When Ta = 50°C, P (max) = 0.53 W (($I_O$ = 0.5 A),
$T_j$ = 0.53 W × 37.1°C/W + 50°C = 69.7°C

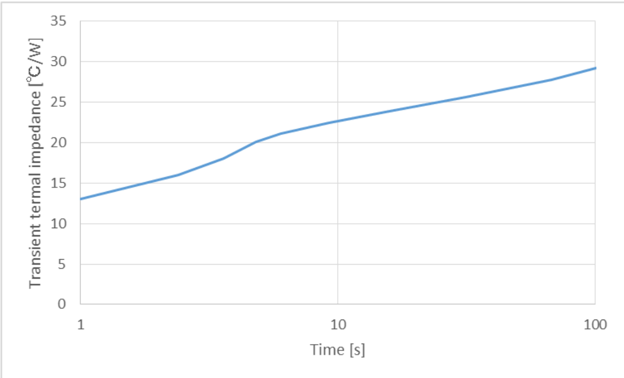
Transient thermal resistance in 0.1 s: $R_{th\ (j\text{-}a)}$ = approximately 13°C/W. (Refer to below figure)
When Ta = 50°C, P (typ.) = 9.05 W ($I_O$ = 3 A),
$T_j$ = 9.05 W × 13°C/W + 25°C = 142°C

## (3) Heat calculation 2

Under the conditions of mounting board written below, the heat resistance (Rth (jc)) between the junction and the surface of the package is about 3°C/W.
So, the junction temperature (Tj) can be calculated by measuring the surface temperature of the package (Tc).

Example: In mounting board: Rth (ja) = 37.1°C/W, Rth (jc) = approximately 3°C/W (4-layer board, FR4, 74mm × 74 mm × 1.6 mm)
When temperature of surface of the package (Tc) = 50℃ and power consumption (P) = 1 W,
$T_j$ = Tc + P × Rth (jc)
$T_j$ = 50℃ + 1W × 3°C/W = 53℃



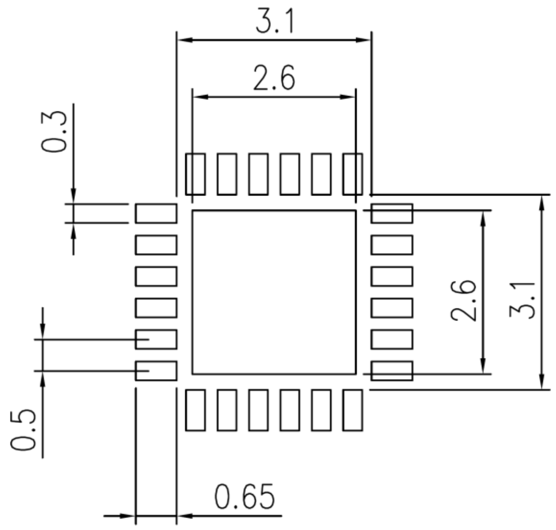
Transient thermal resistance

Note: Pay attention that $R_{th\ (ja)}$ and Rth (jc) depends on the usage conditions (mounting method of the board).
When ambient temperature is high, tolerable power consumption becomes small.
Please evaluate the IC under the condition that the junction temperature is 150°C or less and secure the sufficient safety margin in using the IC because above description is just a method of calculation.

## 9. Foot pattern example (for reference only)

P-WQFN24-0404-0.50-004

Unit: mm




Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only.
  TOSHIBA is not responsible for any incorrect or incomplete drawings and information.
- You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes.
- The drawing shown may not accurately represent the actual shape or dimensions.
- Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

**Fig.8 Foot pattern example**

Note: Design the pattern in consideration of the heat design because the back side has the role of heat radiation.

(The back side should be connected to GND because it is connected to the back of the chip electrically.)

## Notes on Contents

### 1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### 2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3. Timing Charts
Timing charts may be simplified for explanatory purposes.

### 4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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### 5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

## IC Usage Considerations
### Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

## Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature ($T_j$) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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