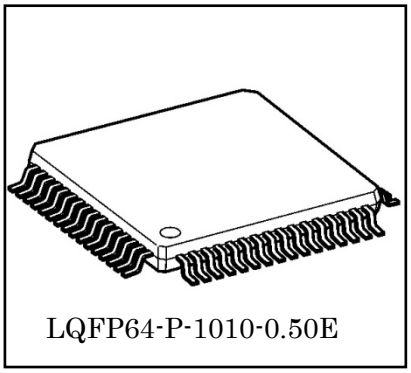
CMOS Digital Integrated Circuit Silicon Monolithic

TC90207FG

LVDS-Rx IC

1. Description

TC90207FG is LVDS-Rx IC for picture IF. Input signal is LVDS (4ch Data/1ch Clock), and output signal is LVTTL.



LQFP64-P-1010-0.50E

Weight: 0.35g (typ.)

2. Application

For picture IF IC.

3. Features

- LVDS input(4ch Data lane / 1ch Clock lane)
- LVTTL output(28bit Data, Clock)
- Power Down(LVDS-Rx, output pin is Low)
- Capable of LVTTL output Data swapping
  - Input Lane swap(Rx-A⇔Rx-D, Rx-B⇔Rx-D)
  - Output swap(DOUT[n]⇔DOUT[27-n])
  - 8bit RGB output swap
- Power supply: 3.3V, 1.5V
- Package: LQFP64-P-1010-0.50E

4. Block Diagram

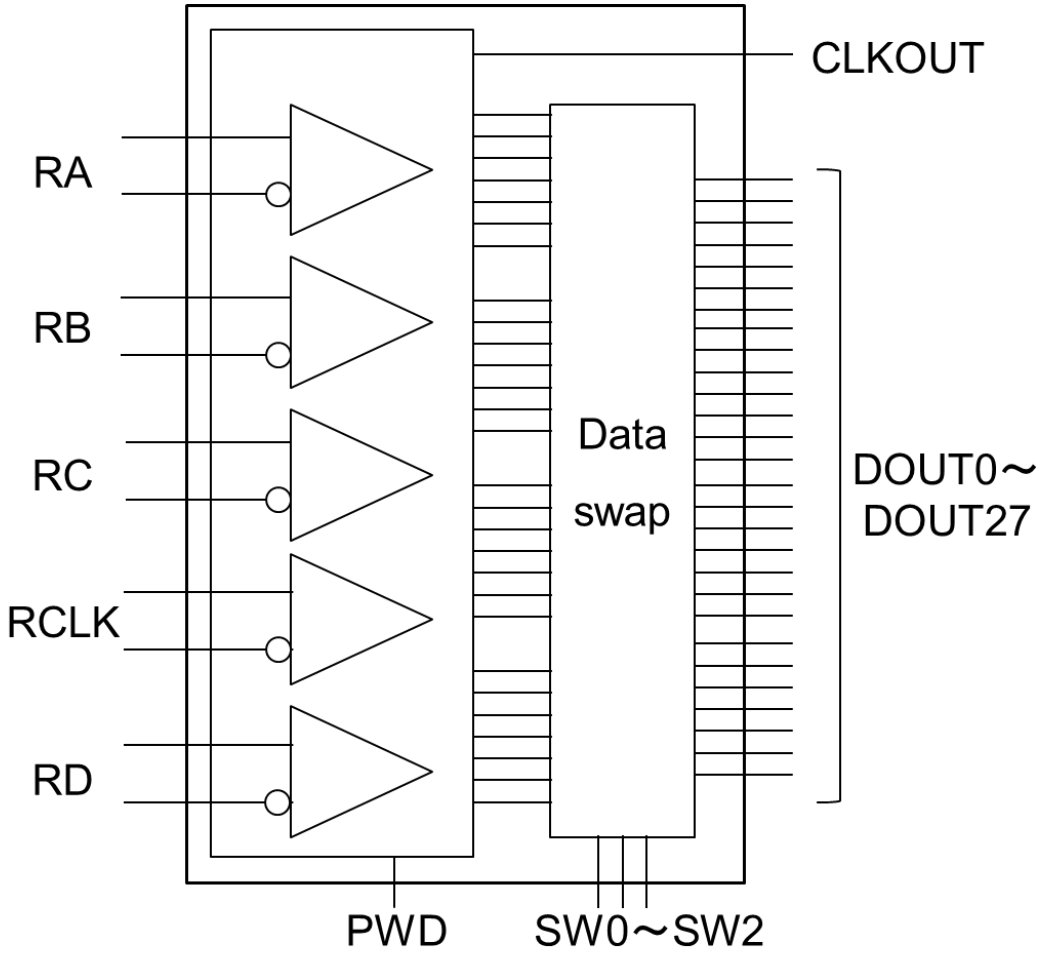


Figure 4.1 Block diagram

5. Pin Layout

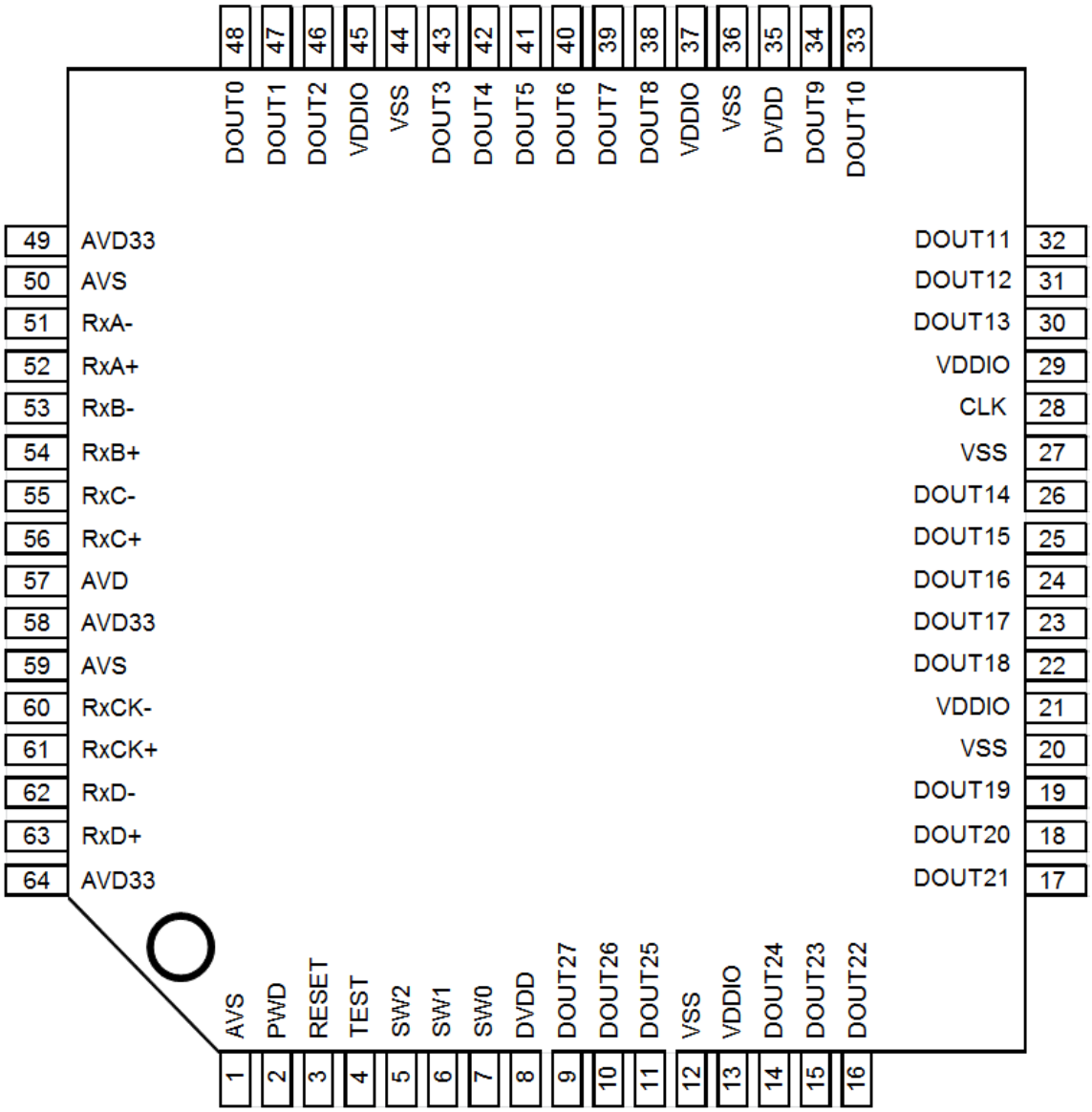


Figure 5.1 Pin Layout

6. Pin Description

Table 6.1 Pin Description

Pin Number	Name	I/O	Function	When unused
1	AVS	-	GND(LVDS-Rx)	-
2	PWD	In	Power down control (Low: Normal, High: Power Down)	GND
3	RESET	In	RESET Pin (Low: Reset, High: Normal)	-
4	TEST	In	TEST Pin (Low: Normal)	GND
5	SW2	In	Output data swapping control	GND
6	SW1	In	Output data swapping control	GND
7	SW0	In	Output data swapping control	GND
8	DVDD	-	1.5V Power Supply for Logic circuit	-
9	DOUT27	Out	Data output	Open
10	DOUT26	Out	Data output	Open
11	DOUT25	Out	Data output	Open
12	VSS	-	GND	-
13	VDDIO	-	3.3V Power Supply for I/O	-
14	DOUT24	Out	Data output	Open
15	DOUT23	Out	Data output	Open
16	DOUT22	Out	Data output	Open
17	DOUT21	Out	Data output	Open
18	DOUT20	Out	Data output	Open
19	DOUT19	Out	Data output	Open
20	VSS	-	GND	-
21	VDDIO	-	3.3V Power supply for I/O	-
22	DOUT18	Out	Data output	Open
23	DOUT17	Out	Data output	Open
24	DOUT16	Out	Data output	Open
25	DOUT15	Out	Data output	Open
26	DOUT14	Out	Data output	Open
27	VSS	-	GND	-
28	CLK	Out	Clock output	Open
29	VDDIO	-	3.3V Power Supply for I/O	-
30	DOUT13	Out	Data output	Open
31	DOUT12	Out	Data output	Open
32	DOUT11	Out	Data output	Open

Pin Number	Name	I/O	Function	When unused
33	DOUT10	Out	Data output	Open
34	DOUT9	Out	Data output	Open
35	DVDD	-	1.5V Power Supply for Logic circuit	-
36	VSS	-	GND	-
37	VDDIO	-	3.3V Power Supply for I/O	-
38	DOUT8	Out	Data output	Open
39	DOUT7	Out	Data output	Open
40	DOUT6	Out	Data output	Open
41	DOUT5	Out	Data output	Open
42	DOUT4	Out	Data output	Open
43	DOUT3	Out	Data output	Open
44	VSS	-	GND	-
45	VDDIO	-	3.3V Power Supply for I/O	-
46	DOUT2	Out	Data output	Open
47	DOUT1	Out	Data output	Open
48	DOUT0	Out	Data output	Open
49	AVD33	-	3.3V Power Supply for LVDS-Rx	-
50	AVS	-	GND (LVDS-Rx)	-
51	RxA-	In	LVDS Ach (-) input	GND
52	RxA+	In	LVDS Ach (+) input	GND
53	RxB-	In	LVDS Bch (-) input	GND
54	RxB+	In	LVDS Bch (+) input	GND
55	RxC-	In	LVDS Cch (-) input	GND
56	RxC+	In	LVDS Cch (+) input	GND
57	AVD	-	1.5V Power Supply for LVDS-Rx	-
58	AVD33	-	3.3V Power Supply for LVDS-Rx	-
59	AVS	-	GND (LVDS-Rx)	-
60	RxCK-	In	LVDS Clock (-) input	GND
61	RxCK+	In	LVDS Clock (+) input	GND
62	RxD-	In	LVDS Dch (-) input	GND
63	RxD+	In	LVDS Dch (+) input	GND
64	AVD33	-	3.3V Power Supply for LVDS-Rx	-

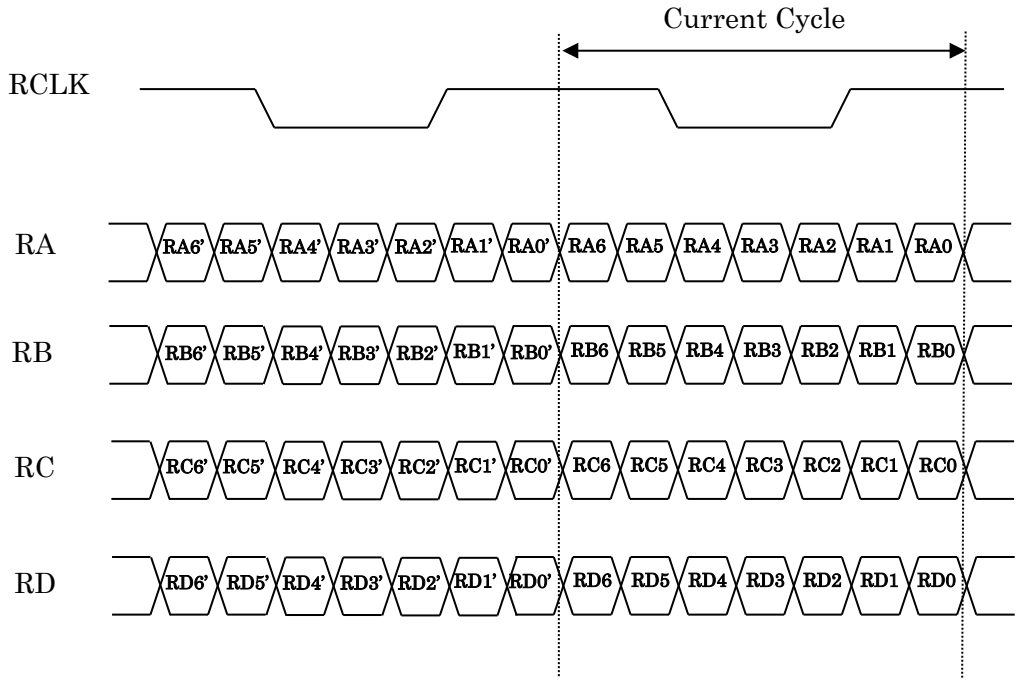
7. Functional description

7.1. LVDS signal input

LVDS data input interface takes differential signal input of 4 channels, and generates the clock frequency 7-multiplied for input clock by PLL circuit in receiver core. And it takes out signal in 7 bit of each channel by deserializer.

Therefore data of all 28 bits (7 bits x 4 channels) can be received.

Figure 7.1 LVDS Data arrangement



7.2. LVTTL output

Input LVDS signal is converted to LVTTL. It can swap output data like the following table by the L/H state of SW0-SW2 control pins.

Table 7.2 1 Description of data output pin

SW0	L	H	L	H	L	H	L	H
SW1	L	L	H	H	L	L	H	H
SW2	L	L	L	L	H	H	H	H
DOUT0	RA0	RD0	RD6	RA6	RC3	RB3	RD6	RA6
DOUT1	RA1	RD1	RD5	RA5	RC2	RB2	RC6	RB6
DOUT2	RA2	RD2	RD4	RA4	RC1	RB1	RC4	RB4
DOUT3	RA3	RD3	RD3	RA3	RC0	RB0	RC5	RB5
DOUT4	RA4	RD4	RD2	RA2	RB6	RC6	RD0	RA0
DOUT5	RA5	RD5	RD1	RA1	RB5	RC5	RD1	RA1
DOUT6	RA6	RD6	RD0	RA0	RD5	RA5	RA0	RD0
DOUT7	RB0	RC0	RC6	RB6	RD4	RA4	RA1	RD1
DOUT8	RB1	RC1	RC5	RB5	RB4	RC4	RA2	RD2
DOUT9	RB2	RC2	RC4	RB4	RB3	RC3	RA3	RD3
DOUT10	RB3	RC3	RC3	RB3	RB2	RC2	RA4	RD4
DOUT11	RB4	RC4	RC2	RB2	RB1	RC1	RA5	RD5
DOUT12	RB5	RC5	RC1	RB1	RB0	RC0	RD2	RA2
DOUT13	RB6	RC6	RC0	RB0	RA6	RD6	RD3	RA3
DOUT14	RC0	RB0	RB6	RC6	RD3	RA3	RA6	RD6
DOUT15	RC1	RB1	RB5	RC5	RD2	RA2	RB0	RC0
DOUT16	RC2	RB2	RB4	RC4	RA5	RD5	RB1	RC1
DOUT17	RC3	RB3	RB3	RC3	RA4	RD4	RB2	RC2
DOUT18	RC4	RB4	RB2	RC2	RA3	RD3	RB3	RC3
DOUT19	RC5	RB5	RB1	RC1	RA2	RD2	RB4	RC4
DOUT20	RC6	RB6	RB0	RC0	RA1	RD1	RD4	RA4
DOUT21	RD0	RA0	RA6	RD6	RA0	RD0	RD5	RA5
DOUT22	RD1	RA1	RA5	RD5	RD1	RA1	RB5	RC5
DOUT23	RD2	RA2	RA4	RD4	RD0	RA0	RB6	RC6
DOUT24	RD3	RA3	RA3	RD3	RC5	RB5	RC0	RB0
DOUT25	RD4	RA4	RA2	RD2	RC4	RB4	RC1	RB1
DOUT26	RD5	RA5	RA1	RD1	RC6	RB6	RC2	RB2
DOUT27	RD6	RA6	RA0	RD0	RD6	RA6	RC3	RB3
CLKOUT	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK

7.3. Power down

When the PWD pin is the High state, LVDS-Rx core is power down state, and LVTTL output is Low.

7.4. Reset control

Reset system: Asynchronous reset (Even if LVDS clock isn't input, it can control a reset.)
Reset period : Maintaining Low state for more than 1μs.

When normal operation, Reset pin is the high state.

8. Absolute maximum rating

The parameters listed in the following absolute maximum rating table are limit values for this product. Exceeding even one of these limit values even momentarily may cause damage to the product. Be sure to use it within the operating ratings.

Table 8.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Power supply1 (1.5V block)	VDD1	-0.3 to VSS+2.0	V
Power supply 2 (3.3V block)	VDD2	-0.3 to VSS+3.9	V
Input voltage (LVDS)	V_{LVDSIN}	-0.3 to VDD1+0.3	V
Input voltage (3.3V I/O)	V_{TTLIN}	-0.3 to VDD1+0.3	V
Potential difference between supply pins (1.5V block supply voltage pins)	ΔVDG1 (Note 1)	0.3	V
Potential difference between supply pins (3.3V block supply voltage pins)	ΔVDG2 (Note 1)	0.3	V
Power dissipation	P_D	1739	W
Operating temperature	T_{opr}	–40 to 85	°C
Storage temperature	T_{stg}	–50 to 125	°C

Note 1: For each of 1.5V and 3.3V, system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.
In addition, potential difference between all V_{SS} terminal must be under 0.01V in this status.
If using a temperature higher than Ta=25°C, reduce by 17.39mW per 1°C increase.
When Ta=85°C, maximum power dissipation is 696mW.

8.1. Allowable power dissipation

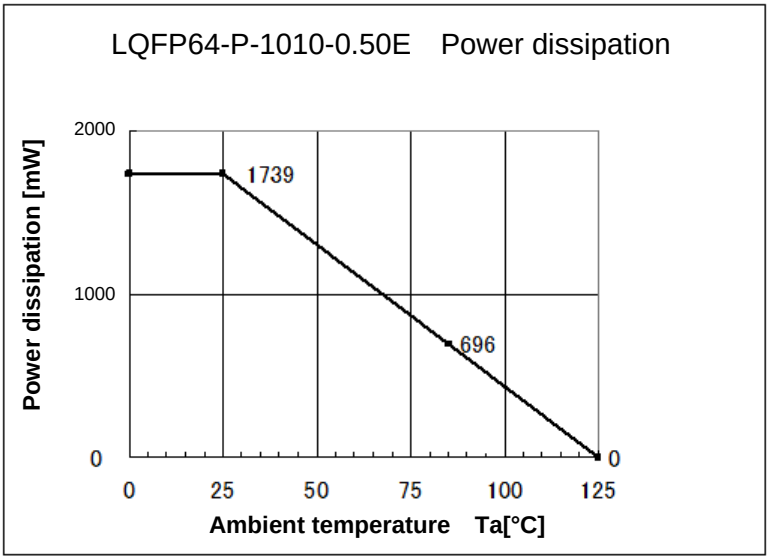


Figure 8.1 Allowable power dissipation

9. Operating conditions

The product may not operate normally if its rated supply voltage range is exceeded.
Once a rated supply voltage range is exceeded, the product may remain in a condition different from the previous condition even if it gets back to the rated range.
If a rated range is exceed, it is necessary to turn the product powor off and on again.

Table 9.1 Operating conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Digital block supply voltage (Note1)	VDD-D	1.4	1.5	1.6	V
I/O block supply voltage (Note 2)	VDD-IO	3.0	3.3	3.6	V
LVDS block supply voltage1 (Note 1)	VDD-L1	1.4	1.5	1.6	V
LVDS block supply voltage2 (Note 2)	VDD-L2	3.0	3.3	3.6	V
Operating temperature	Topr	-40		85	°C

Note 1: It's necessary to make the digital block supply voltage and the LVDS block supply voltage 1 the same electric potential mostly.

Note 2: It's necessary to make the I/O block supply voltage and the LVDS block supply voltage 2 the same electric potential mostly.

10. Electrical characteristics

Table 10.1 DC characteristics

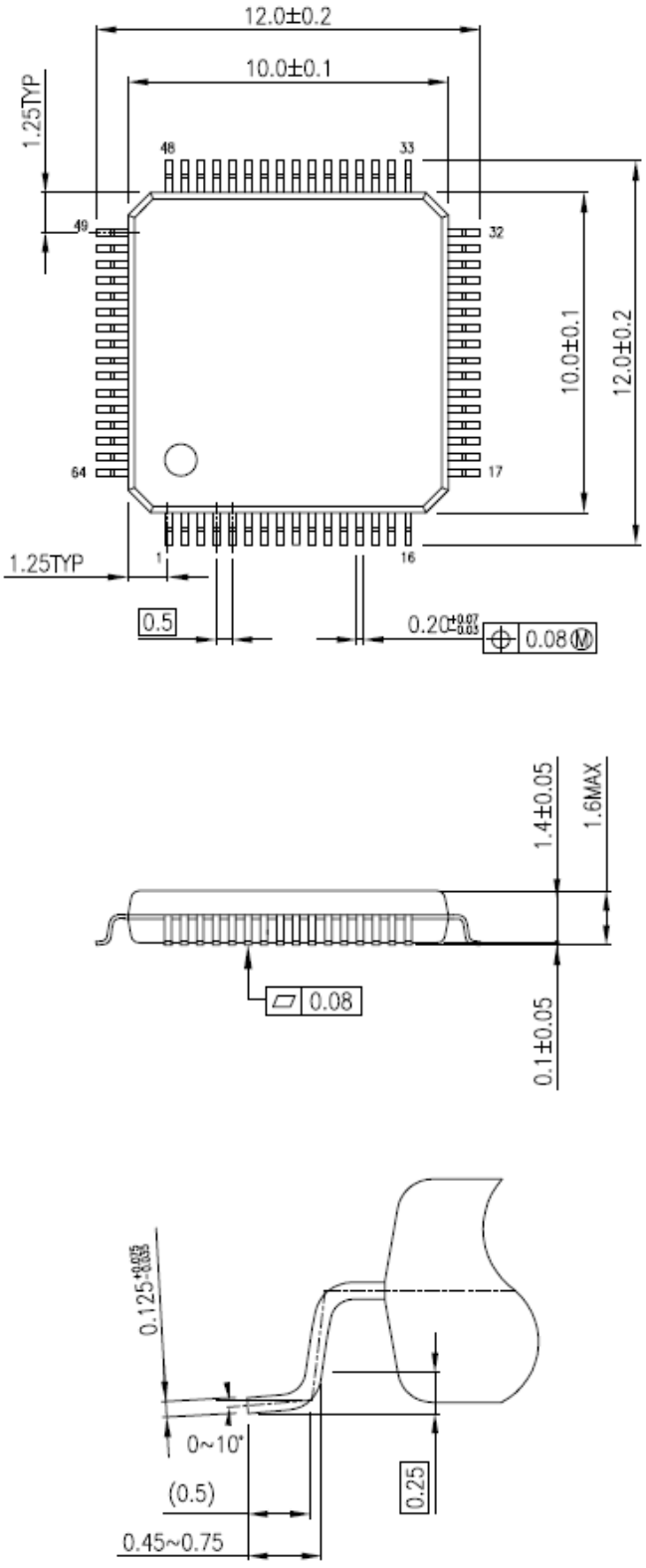
(Ta=-40 to 85°C,VDD1=1.50±0.1V, VDD2=3.30±0.3V)

Parameter	Symbol	Pin number	Min	Typ.	Max	Unit	Remarks
Power supply current	IDD1 (1.5V block)	57	—	—	10	mA	1.5V for LVDS
		8,35	—	—	10	mA	1.5V for digital block
	IDD2 (3.3V block)	49,58,64	—	—	60	mA	3.3V for LVDS
		13,21,29,37,45	—	—	70	mA	3.3V for I/O (Note 1)
Input voltage	VIH	2,3,5,6,7	VDD2×0.8	—	VDD2	V	3.3V block I/O input pin
	VIL	2,3,5,6,7	VSS	—	VDD2×0.2	V	
Input current	IIH	2,3,5,6,7	-10	—	10	μA	3.3V block I/O input pin
	IIL	2,3,5,6,7	-10	—	10	μA	
Output voltage	VOH	9,10,11,14,15,16, 17,18,19,22,23,24, 25,26,28,30,31,32, 33,34,38,39,40,41, 42,43,46,47,48	VDD2-0.6	—	VDD2	V	3.3V block I/O output pin with 4mA sink load
	VOL	9,10,11,14,15,16, 17,18,19,22,23,24, 25,26,28,30,31,32, 33,34,38,39,40,41, 42,43,46,47,48	VSS	—	0.4	V	
Differential input input voltage	VTH	51,52,53,54,55,56, 60,61,62,63	—	—	100	mV	Differential input pin Voc=1.2V
	VTL	51,52,53,54,55,56, 60,61,62,63	-100	—	—	mV	
Differential input input current	IIN	51,52,53,54,55,56, 60,61,62,63	-10	—	10	μA	—

Note 1: It depends on the load capacity for the current value of the 3.3V block voltage.
When the load capacity is high, there is a possibility beyond the mentioned maximum.

11. Package

LQFP64-P-1010-0.50E Unit: mm



Weight: 0.35g (typ.)

12. Revision history

Rev.	Date	Content
1.00	2016/02/24	First edition (Summary)

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