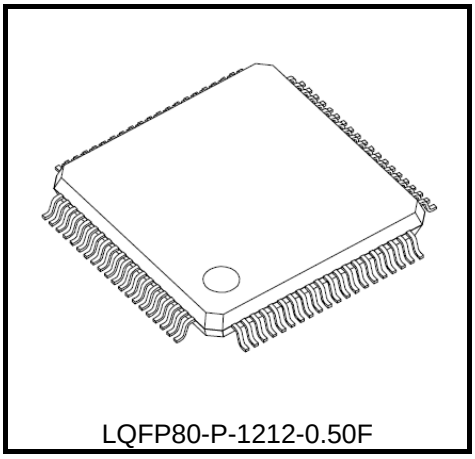
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90205FG

Picture quality improver IC embedded T-Con signal generation

1. Overview

TC90205FG has picture quality improver (Horizontal lower bit expander, Edge Enhancement, Color adjustment, Contrast adjustment, etc.) for input digital RGB video signal (6bit/8bit), and it outputs digital RGB video signal (6bit/8bit). Timing control signal for panel operating are outputted with RGB video signal.



LQFP80-P-1212-0.50F

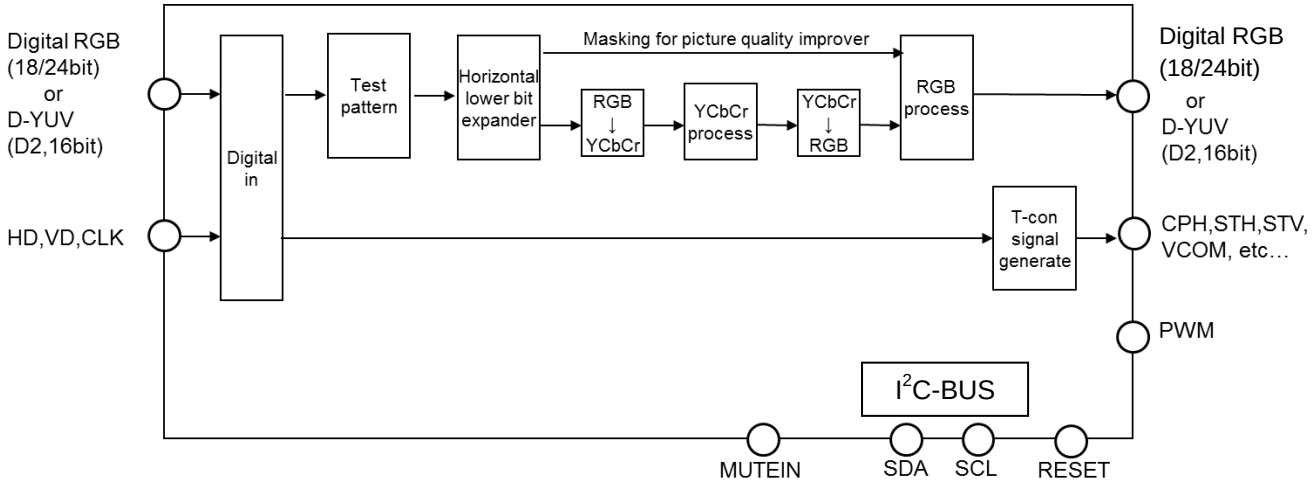
Weight: 0.49 g (Typ.)

1.1 Features

1. Input/Output video signal format
   Digital RGB (WVGA: 800x480)
   ITU-R BT.601 (Digital YUV (D2(480p): 720x480))
2. Operation frequency
   WVGA 30 to 40MHz
   D2 27MHz
3. Input/Output video signal bit
   Digital RGB (Input=6/8bit, Output=6/8bit)
   Digital YUV (Input/Output=8bit)
4. Picture quality improver
   Horizontal lower bit expander
   < Y signal process>
   HVD Enhancer
   Sharpness, LTI / Noise canceller
   Static Y-gamma correction
   Dynamic Y-gamma correction
   Contrast, Brightness
   < Color signal process>
   CTI / Noise canceller
   C gain correction with Y-gamma correction
   Color management
   Tint
   Cb/Cr gain adjustment, Cb/Cr offset adjustment
   <RGB signal process>
   Offset adjustment, Gain adjustment
   RGB gamma correction
   Dither, FRC (Frame rate control)
5. Timing control pulse output for LCD panel
6. PWM signal output
7. I^2C-BUS control
8. Package
   LQFP80-P-1212-0.50F
9. Power supply
   3.3V, 1.5V
10. Operation temperature
    -40°C to 85°C

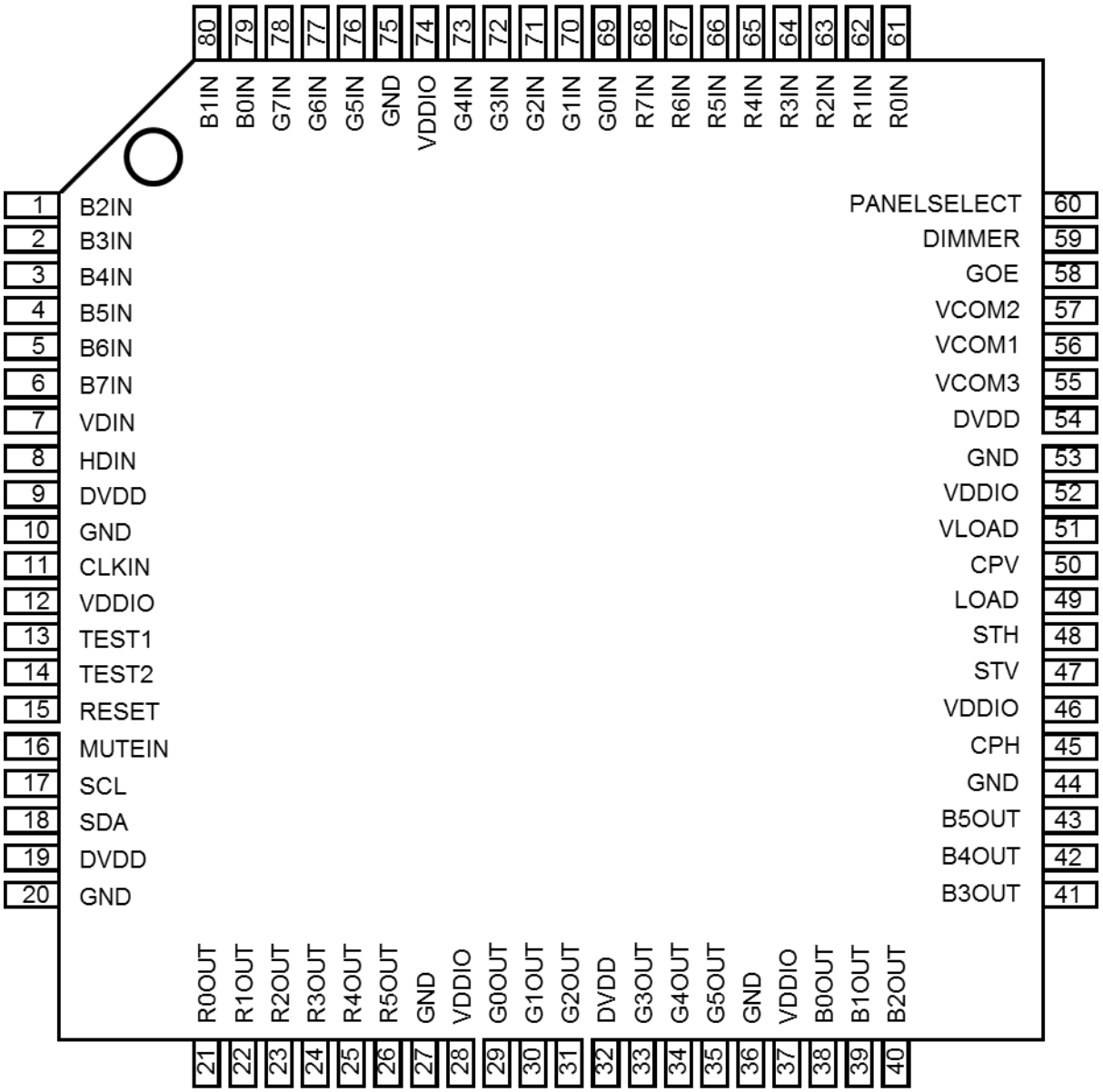
2. Block diagram

The function block, the circuit and the terminal in the block diagrams are omitted or simplified in order to explain the function.



3. Pin layout

Package TOP VIEW



4. Pin description

Pin No.	Pin name	Block	IO	Function	Standard withstand voltage[V]
1	B2IN	Digital IN	Input	Digital RGB input (B2)	3.3
2	B3IN	Digital IN	Input	Digital RGB input (B3)	3.3
3	B4IN	Digital IN	Input	Digital RGB input (B4)	3.3
4	B5IN	Digital IN	Input	Digital RGB input (B5)	3.3
5	B6IN	Digital IN	Input	Digital RGB input (B6)	3.3
6	B7IN	Digital IN	Input	Digital RGB input (B7)	3.3
7	VDIN	Digital IN	Input	Digital RGB input (Vertical sync signal)	3.3
8	HDIN	Digital IN	Input	Digital RGB input (Horizontal sync signal)	3.3
9	DVDD	Power	-	1.5V power supply for logic block	-
10	GND	Power	-	GND	-
11	CLKIN	Digital IN	Input	Digital RGB input (Clock signal)	3.3
12	VDDIO	Power	-	3.3V power supply for I/O block	-
13	TEST1	TEST	Input	For TEST	3.3
14	TEST2	TEST	Input	For TEST (High: Internal clock mode, Low: Normal mode)	3.3
15	RESET	RESET	Input	Reset control	3.3
16	MUTEIN	MUTE	Input	Mute control	3.3
17	SCL	I^2C	Input	I^2C-BUS control (SCL)	5
18	SDA	I^2C	I/O	I^2C-BUS control (SDA)	5
19	DVDD	Power	-	1.5V power supply for logic block	-
20	GND	Power	-	GND	-
21	R0OUT	Digital OUT	Output	Digital RGB output (R0)	3.3
22	R1OUT	Digital OUT	Output	Digital RGB output (R1)	3.3
23	R2OUT	Digital OUT	Output	Digital RGB output (R2)	3.3
24	R3OUT	Digital OUT	Output	Digital RGB output (R3)	3.3
25	R4OUT	Digital OUT	Output	Digital RGB output (R4)	3.3
26	R5OUT	Digital OUT	Output	Digital RGB output (R5)	3.3
27	GND	Power	-	GND	-
28	VDDIO	Power	-	3.3V power supply for I/O block	-
29	G0OUT	Digital OUT	Output	Digital RGB output (G0)	3.3
30	G1OUT	Digital OUT	Output	Digital RGB output (G1)	3.3
31	G2OUT	Digital OUT	Output	Digital RGB output (G2)	3.3
32	DVDD	Power	-	1.5V power supply for logic block	-
33	G3OUT	Digital OUT	Output	Digital RGB output (G3)	3.3
34	G4OUT	Digital OUT	Output	Digital RGB output (G4)	3.3
35	G5OUT	Digital OUT	Output	Digital RGB output (G5)	3.3
36	GND	Power	-	GND	-
37	VDDIO	Power	-	3.3V power supply for I/O block	-
38	B0OUT	Digital OUT	Output	Digital RGB output (B0)	3.3
39	B1OUT	Digital OUT	Output	Digital RGB output (B1)	3.3
40	B2OUT	Digital OUT	Output	Digital RGB output (B2)	3.3

Pin No.	Pin name	Block	IO	Function	Standard withstand voltage[V]
41	B3OUT	Digital OUT	Output	Digital RGB output (B3)	3.3
42	B4OUT	Digital OUT	Output	Digital RGB output (B4)	3.3
43	B5OUT	Digital OUT	Output	Digital RGB output (B5)	3.3
44	GND	Power	-	GND	-
45	CPH	LCD control	Output	Control signal for LCD panel (Horizontal clock signal)	3.3
46	VDDIO	Power	-	3.3V power supply for I/O block	-
47	STV	LCD control	Output	Control signal for LCD panel (Vertical start pulse for writing)	3.3
48	STH	LCD control	Output	Control signal for LCD panel (Horizontal start pulse for writing)	3.3
49	LOAD	LCD control	Output	Control signal for LCD panel (Horizontal Enable pulse for writing)	3.3
50	CPV	LCD control	Output	Control signal for LCD panel (Vertical clock signal)	3.3
51	VLOAD	LCD control	Output	Control signal for LCD panel (Vertical Enable pulse for writing)	3.3
52	VDDIO	Power	-	3.3V power supply for I/O block	-
53	GND	Power	-	GND	-
54	DVDD	Power	-	1.5V power supply for logic block	-
55	VCOM3	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 3)	3.3
56	VCOM1	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 1)	3.3
57	VCOM2	LCD control	Output	Control signal for LCD panel (Output voltage for common erector 2)	3.3
58	GOE	LCD control	Output	Control signal for LCD panel (Panel reset signal)	3.3
59	DIMMER	PWM	Output	PWM signal output	3.3
60	PANELSELECT	LCD control	Input	Control signal for LCD panel (Polarity select for GOE signal)	3.3
61	R0IN	Digital IN	Input	Digital RGB input (R0)	3.3
62	R1IN	Digital IN	Input	Digital RGB input (R1)	3.3
63	R2IN	Digital IN	Input	Digital RGB input (R2)	3.3
64	R3IN	Digital IN	Input	Digital RGB input (R3)	3.3
65	R4IN	Digital IN	Input	Digital RGB input (R4)	3.3
66	R5IN	Digital IN	Input	Digital RGB input (R5)	3.3
67	R6IN	Digital IN	Input	Digital RGB input (R6)	3.3
68	R7IN	Digital IN	Input	Digital RGB input (R7)	3.3
69	G0IN	Digital IN	Input	Digital RGB input (G0)	3.3
70	G1IN	Digital IN	Input	Digital RGB input (G1)	3.3
71	G2IN	Digital IN	Input	Digital RGB input (G2)	3.3
72	G3IN	Digital IN	Input	Digital RGB input (G3)	3.3
73	G4IN	Digital IN	Input	Digital RGB input (G4)	3.3
74	VDDIO	Power	-	3.3V power supply for I/O block	-
75	GND	Power	-	GND	-
76	G5IN	Digital IN	Input	Digital RGB input (G5)	3.3
77	G6IN	Digital IN	Input	Digital RGB input (G6)	3.3
78	G7IN	Digital IN	Input	Digital RGB input (G7)	3.3
79	B0IN	Digital IN	Input	Digital RGB input (B0)	3.3
80	B1IN	Digital IN	Input	Digital RGB input (B1)	3.3

5. Function

5.1 Video signal input

5.1.1 Digital RGB signal input

Format : Digital RGB (6bit or 8bit)
Timing signal : HD, VD, Clock
Resolution : WVGA (800x480, 40MHz (max))

5.1.2 Digital YUV signal input

Format : Digital YUV (Y: 8bit, Cb/Cr: 8bit)
Timing signal : HD, VD, Clock
Resolution : D2 (480p) (720x480, 27MHz)

5.1.3 Restriction of input signal

- HD and VD signal input are inputted as same polarity.
- Restriction of HD and VD signal input is described as below.

Item	Symbol	Min	Unit
Horizontal front porch width	Hfp	4	clk
Horizontal back porch width	Hbp	1	clk
Horizontal blanking width	Hblank	16	clk
Horizontal sync (HD) width	HDwd	1	clk
Vertical front porch width	Vfp	3	line
Vertical back porch width	Vbp	2	line
Vertical blanking width	Vblank	5	line
Vertical sync (VD) width	VDwd	1	line

Front porch width: width between the end point of previous data enable and the front edge of sync signal
Back porch width: width between the front edge of sync signal and the start point of data enable
Blanking width : width between the end point of previous data enable and the start point of data enable

Note: This LSI doesn't operation when clock (for video signal input) is stopped, because this LSI is operated by clock (for video signal input).

5.1.4 Pin of video signal input

Pin No.	Pin Name	RGB				480P			
61	R0IN	R0	B0	R7	B7				
62	R1IN	R1	B1	R6	B6				
63	R2IN	R2	B2	R5	B5				
64	R3IN	R3	B3	R4	B4				
65	R4IN	R4	B4	R3	B3				
66	R5IN	R5	B5	R2	B2				
67	R6IN	R6	B6	R1	B1				
68	R7IN	R7	B7	R0	B0				
69	G0IN	G0	G0	G7	G7	Y0	C0	Y7	C7
70	G1IN	G1	G1	G6	G6	Y1	C1	Y6	C6
71	G2IN	G2	G2	G5	G5	Y2	C2	Y5	C5
72	G3IN	G3	G3	G4	G4	Y3	C3	Y4	C4
73	G4IN	G4	G4	G3	G3	Y4	C4	Y3	C3
76	G5IN	G5	G5	G2	G2	Y5	C5	Y2	C2
77	G6IN	G6	G6	G1	G1	Y6	C6	Y1	C1
78	G7IN	G7	G7	G0	G0	Y7	C7	Y0	C0
79	B0IN	B0	R0	B7	R7	C0	Y0	C7	Y7
80	B1IN	B1	R1	B6	R6	C1	Y1	C6	Y6
1	B2IN	B2	R2	B5	R5	C2	Y2	C5	Y5
2	B3IN	B3	R3	B4	R4	C3	Y3	C4	Y4
3	B4IN	B4	R4	B3	R3	C4	Y4	C3	Y3
4	B5IN	B5	R5	B2	R2	C5	Y5	C2	Y2
5	B6IN	B6	R6	B1	R1	C6	Y6	C1	Y1
6	B7IN	B7	R7	B0	R0	C7	Y7	C0	Y0
DMODE[2:0]		110				111			
IPIN_SEL[1]		0	0	1	1	0	0	1	1
IPIN_SEL[0]		0	1	0	1	0	1	0	1

5.2 Video signal output

5.2.1 Digital RGB signal (when inputting Digital RGB signal)

Video signal: Digital RGB signal (6bit or 8bit)
Timing signal (when outputting RGB 6bit): CPH, STH, LOAD, CPV, VLOAD/DE, STV, VCOM1, VCOM2, VCOM3, GOE
Timing signal (when outputting RGB 8bit): CPH, STH/DE, STV

5.2.2 Digital YUV signal (when inputting Digital YUV signal)

Video signal: Digital YUV signal (Y: 8bit, Cb/Cr: 8bit)
Timing signal: HD, VD, DE, CLOCK
Resolution: D2 (480p; 720x480, 27MHz)

5.3 Timing control signal output for LCD panel

Timing control signal is outputted with reference to the front edge of data enable output.
Timing control signal is restricted by the back porch width of HD/VD input.

< Horizontal >
The horizontal start phase for panel control signals is limited to width of horizontal back porch for D-RGB input setting.
Output horizontal back porch = input back porch [clk]

< Vertical >
The vertical start phase for panel control signals is limited to width of vertical back porch for D-RGB input setting.
Output vertical back porch = input back porch [line]

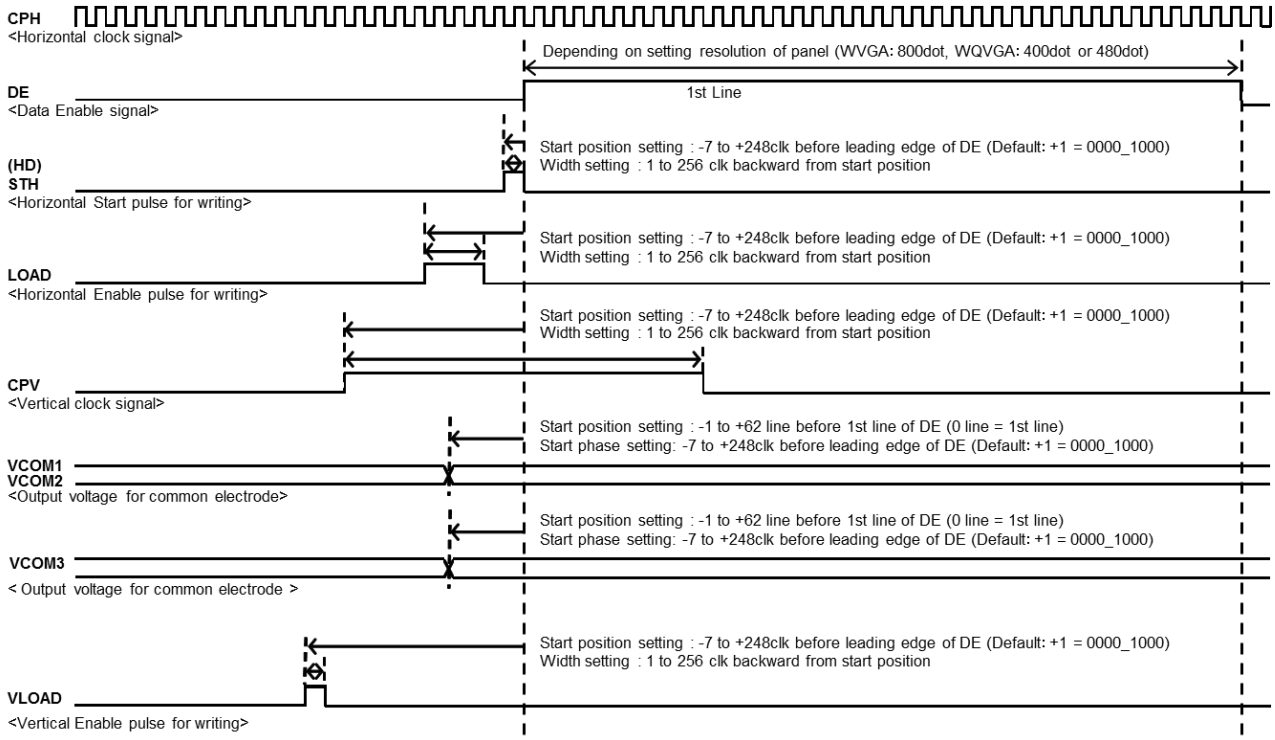
	Pin		Signal Name		Register setting				
	Pin name	I/O	Standard mode	Other mode	Start phase	Start line	Pulse width	Polarity	Add. pulse
1	CPH	O	Clock	CPH	-	-	-	○	-
2	STH	O	HD	STH	○	-	○	○	-
3	LOAD	O	-	LOAD	○	-	○	○	-
4	CPV	O	-	CPV	○	-	○	○	-
5	STV1	O	VD	STV	○	○	○ [line]	○	-
6	VCOM1	O	-	VCOM1	○	○	-	-	-
7	VCOM2	O	-	VCOM2	Same as VCOM1		-	○※1	-
8	VCOM3	O	-	VCOM3	○	○	-	○※1	-
9	VLOAD	O	-/DE	VLOAD/DE	○	○	○	-	-
10	GOE	O	-	GOE	○※2	○※2	○※2	-	○※2
11	PANELSELECT	I	-	PANELSELECT	-	-	-	-	-

*1: Invert for VCOM1

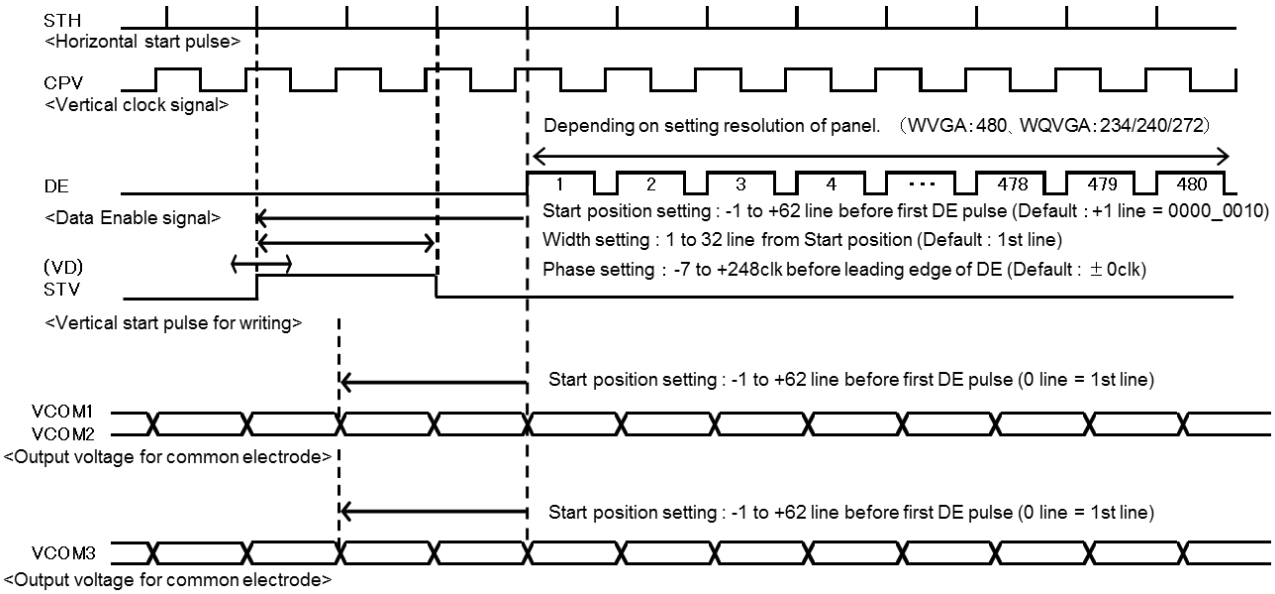
*2: Same as VLOAD setting

Note: Slave address of I^2C-BUS is changed, when status of PANELSELECT pin is changed for switching the polarity of GOE signal output.

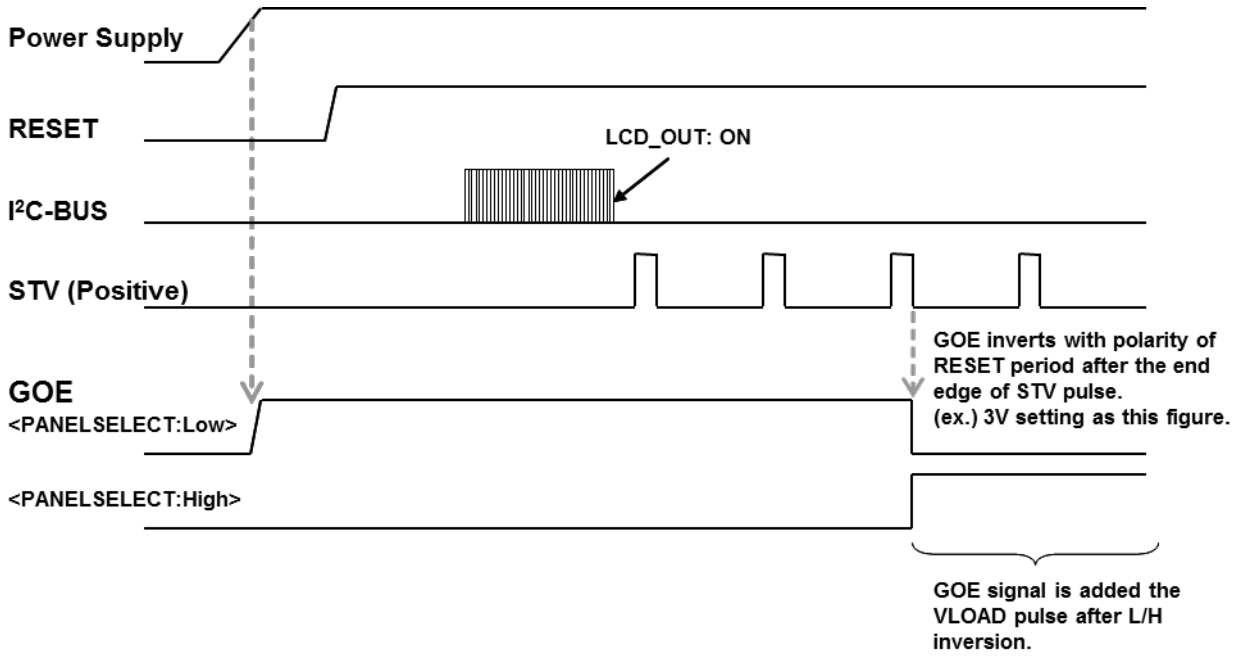
<Horizontal>


CPH
<Horizontal clock signal>
Depending on setting resolution of panel (WVGA: 800dot, WQVGA: 400dot or 480dot)
DE
<Data Enable signal>
1st Line
Start position setting : -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
Width setting : 1 to 256 clk backward from start position
(HD)
STH
<Horizontal Start pulse for writing>
Start position setting : -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
Width setting : 1 to 256 clk backward from start position
LOAD
<Horizontal Enable pulse for writing>
Start position setting : -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
Width setting : 1 to 256 clk backward from start position
CPV
<Vertical clock signal>
Start position setting : -1 to +62 line before 1st line of DE (0 line = 1st line)
Start phase setting: -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
VCOM1
VCOM2
<Output voltage for common electrode>
Start position setting : -1 to +62 line before 1st line of DE (0 line = 1st line)
Start phase setting: -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
VCOM3
< Output voltage for common electrode >
Start position setting : -7 to +248clk before leading edge of DE (Default: +1 = 0000_1000)
Width setting : 1 to 256 clk backward from start position
VLOAD
<Vertical Enable pulse for writing>

<Vertical>


STH
<Horizontal start pulse>
CPV
<Vertical clock signal>
Depending on setting resolution of panel. （WVGA:480、WQVGA:234/240/272）
DE
1
2
3
4
・・・
478
479
480
<Data Enable signal>
Start position setting : -1 to +62 line before first DE pulse (Default : +1 line = 0000_0010)
Width setting : 1 to 32 line from Start position (Default : 1st line)
Phase setting : -7 to +248clk before leading edge of DE (Default : ±0clk)
(VD)
STV
<Vertical start pulse for writing>
Start position setting : -1 to +62 line before first DE pulse (0 line = 1st line)
VCOM1
VCOM2
<Output voltage for common electrode>
Start position setting : -1 to +62 line before first DE pulse (0 line = 1st line)
VCOM3
<Output voltage for common electrode>

<Power on and start sequence>



5.4 Terminal assignment of the output signal

-Data signal output

When 8bit-RGB signal output, the lower 2bit is outputted from the timing signal output pin.

Notes**:** When 8bit-RGB signal output, the register “OPIN_SEL[1]” cannot use.

Pin No.	Pin Name	RGB				480P			
21	R0OUT	R0	B0	R5	B5	-	-	-	-
22	R0OUT	R1	B1	R4	B4	-	-	-	-
23	R0OUT	R2	B2	R3	B3	Y0	C0	Y7	C7
24	R0OUT	R3	B3	R2	B2	Y1	C1	Y6	C6
25	R0OUT	R4	B4	R1	B1	Y2	C2	Y5	C5
26	R0OUT	R5	B5	R0	B0	Y3	C3	Y4	C4
29	G0OUT	G0	G0	G5	G5	Y4	C4	Y3	C3
30	G0OUT	G1	G1	G4	G4	Y5	C5	Y2	C2
31	G0OUT	G2	G2	G3	G3	Y6	C6	Y1	C1
33	G0OUT	G3	G3	G2	G2	Y7	C7	Y0	C0
34	G0OUT	G4	G4	G1	G1	C0	Y0	C7	Y7
35	G0OUT	G5	G5	G0	G0	C1	Y1	C6	Y6
38	B0OUT	B0	R0	B5	R5	C2	Y2	C5	Y5
39	B0OUT	B1	R1	B4	R4	C3	Y3	C4	Y4
40	B0OUT	B2	R2	B3	R3	C4	Y4	C3	Y3
41	B0OUT	B3	R3	B2	R2	C5	Y5	C2	Y2
42	B0OUT	B4	R4	B1	R1	C6	Y6	C1	Y1
43	B0OUT	B5	R5	B0	R0	C7	Y7	C0	Y0
OPIN_SEL[1]		0	0	1	1	0	0	1	1
OPIN_SEL[2]		0	1	0	1	0	1	0	1

-Timing signal output

46	CPH	CPH	CPH	CPH	CPH	CPH	CPH	CPH	CPH
47	STV	STV	STV	VD	VD	STV	STV	STV	STV
48	STH	STH	STH	HD	HD	STH	DE	STH	DE
49	LOAD	LOAD	LOAD	Low fixed	Low fixed	R[-1]	R[-1]	R[-1]	R[-1]
50	CPV	CPV	CPV	Low fixed	Low fixed	R[-2](LSB)	R[-2](LSB)	R[-2](LSB)	R[-2](LSB)
51	VLOAD	VLOAD	DE	Low fixed	DE	G[-1]	G[-1]	G[-1]	G[-1]
55	VCOM3	VCOM3	VCOM3	Low fixed	Low fixed	G[-2](LSB)	G[-2](LSB)	G[-2](LSB)	G[-2](LSB)
56	VCOM1	VCOM1	VCOM1	Low fixed	Low fixed	B[-1]	B[-1]	B[-1]	B[-1]
57	VCOM2	VCOM2	VCOM2	Low fixed	Low fixed	B[-2](LSB)	B[-2](LSB)	B[-2](LSB)	B[-2](LSB)
LCD Out Mode		0	0	0	0	1	1	1	1
8BITOUT		0	0	1	1	0	0	1	1
EN_SEL		0	1	0	1	0	1	0	1

6. Absolute maximum rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the absolute maximum rating may result in destruction, degradation or other damage to the IC and other components.

When designing applications for this IC, be sure that none of the absolute maximum rating values will ever be exceeded.

Item	Corresponding terminal	Symbol	Rating	Unit
Power voltage1 (1.5V system)	9,19,32,54	VDD1	-0.3 to VSS+2.0	V
Power voltage2 (3.3V system)	12,28,37,46,52,74	VDD2	-0.3 to VSS+3.9	V
Input voltage (3.3V system)	1,2,3,4,5,6,7,8,11,13,14, 15,16,60,61,62,63,64,65, 66,67,68,69,70,71,72,73, 76,77,78,79,80	VIN2	-0.3 to VDD2+0.3	V
Input voltage (3.3V system, 5V withstand voltage)	17,18	VIN4 (Note 1)	-0.3 to VSS+5.5	V
Potential difference between power pins (between 1.5V system power pins)	9,19,32,54	ΔVDG1 (Note 2)	0.3	V
Potential difference between power pins (between 3.3V system power pins)	12,28,37,46,52,74	ΔVDG2 (Note 3)	0.3	V
Power dissipation	-	PD (Note 4)	1553	mW
Storage temperature	-	Tstg	-40 to 125	°C

Note 1**:** The withstand voltage for pins (SCL, SDA) is 5V.

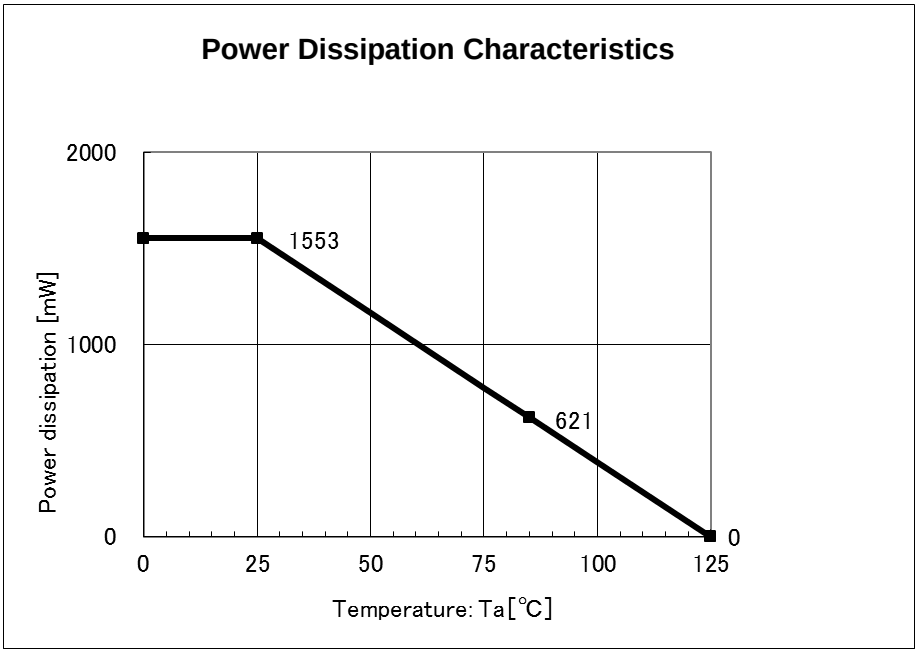
Note 2**:** Make sure that the maximum potential difference between each 1.5V system VDD pin (group) does not exceed the rating when connecting (shorting) a 1.5V system VDD pin with a pin of the same group using the same potential difference. And, keep the maximum potential difference between all VSS pins within 0.01 V.

Note 3**:** Make sure that the maximum potential difference between each 3.3V system VDD pin (group) does not exceed the rating when connecting (shorting) a 3.3V system VDD pin with a pin of the same group using the same potential difference. And, keep the maximum potential difference between all VSS pins within 0.01 V.

Note 4**:** If using a temperature higher than Ta = 25°C, reduce by 15.53mW per 1°C increase (When Ta = 85°C, maximum power dissipation is 621mW.)

6.1 Power Dissipation Characteristics

If using a temperature higher than Ta = 25°C, reduce by 15.53 mW per 1°C increase.
When Ta = 85°C, maximum power dissipation is 621 mW.



7. Operation condition

Cannot guarantee operation of TC90205FG, when the recommendation power supply voltage range (1.4V to1.6V, 3.0V to 3.6V) is exceeded. Please use within the specified operating conditions.
When it returns from the over range, it differs from a previous condition.
Then, it must be turned off and power on again.

Item	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power supply for digital block	9,19,32,54	VDD-D	1.4	1.5	1.6	V
Power supply for I/O block	12,28.37,46,52,74	VDD-IO	3.0	3.3	3.6	V
Operating temperature	-	Topr	-40	-	85	°C

8. Electrical characteristic

8.1 DC characteristic

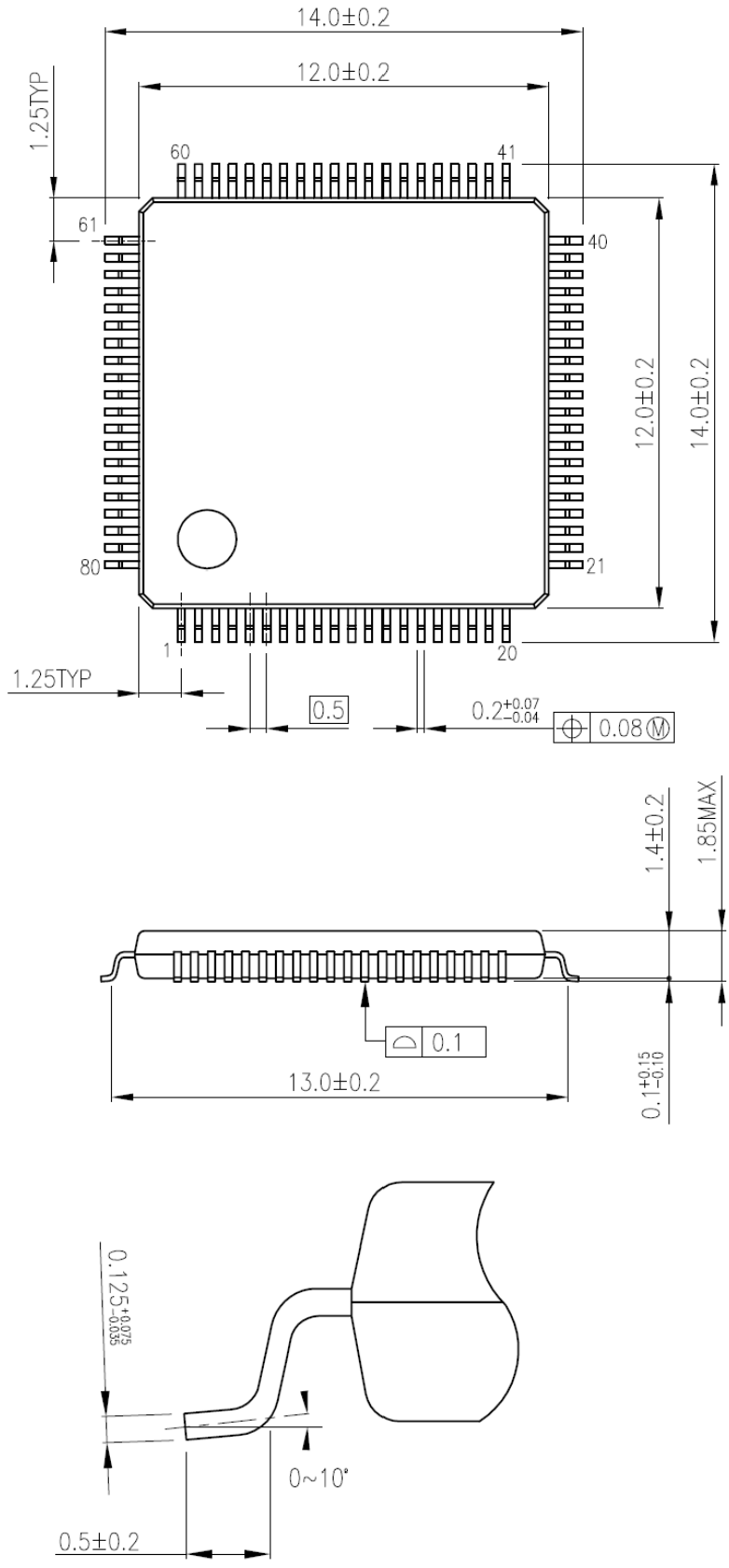
(Ta=25°C, VDD1=1.50±0.1V, VDD2=3.30±0.3V)

Item	Terminal No.	Symbol	Min	Typ.	Max	Unit	Notes
Power supply current	9,19,32,54	IDD1	-	40	65	mA	1.5V system When 33MHz operation
	12,28,37,46,52,74	IDD2	-	40	65	mA	3.3V system When 33MHz operation (Note 1)
Input voltage	1,2,3,4,5,6,7,8,11,13,14,15,16,60,61,62,63,64,65,66,67,68,69,70,71,72,73,76,77,78,79,80	VIH	VDD2 x0.8		VDD	V	I/O input terminal of 3.3V system
	17,18						I/O input terminal of 3.3V system with 5V tolerant
	1,2,3,4,5,6,7,8,11,13,14,15,16,60,61,62,63,64,65,66,67,68,69,70,71,72,73,76,77,78,79,80	VIL	VSS		VDD2 x0.2	V	I/O input terminal of 3.3V system
	17,18						I/O input terminal of 3.3V system with 5V tolerant
Input current	1,2,3,4,5,6,7,8,11,13,14,15,16,60,61,62,63,64,65,66,67,68,69,70,71,72,73,76,77,78,79,80	IIH	-10		10	μA	I/O input terminal of 3.3V system
	17,18						I/O input terminal of 3.3V system with 5V tolerant
	1,2,3,4,5,6,7,8,11,13,14,15,16,60,61,62,63,64,65,66,67,68,69,70,71,72,73,76,77,78,79,80	IIL	-10		10	μA	I/O input terminal of 3.3V system
	17,18						I/O input terminal of 3.3V system with 5V tolerant
Output voltage	21,22,23,24,25,26,29,30,31,33,34,35,38,39,40,41,42,43,45,47,48,49,50,51,55,56,57,58,59	VOH	VDD2 -0.6	—	VDD2	V	I/O output terminal of 3.3V system when load current 4mA
		VOL	VSS	—	0.4	V	I/O output terminal of 3.3V system when load current 4mA
	18					V	I/O output terminal of 3.3V system with 5V tolerant when load current 4mA

Note 1: The power supply current of 3.3V systems depends on the load capacity of the LCD panel connected with this IC.
When the load capacity of the LCD panel is large value, the power supply current of 3.3V systems may exceed the above described maximum value.

9. Package

LQFP80-P-1212-0.50F Unit: mm



Weight: 0.49 g (typ.)

10. Revision history

Date	Revision	Content
2016/04/25	1.00	First Edition

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