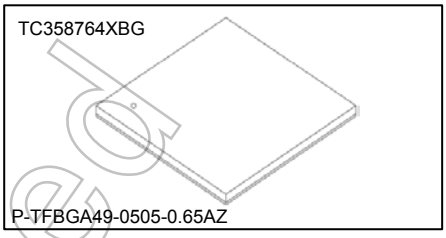
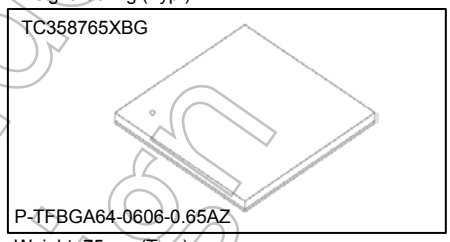
CMOS Digital Integrated Circuit Silicon Monolithic

TC358764XBG/TC358765XBG

Mobile Peripheral Devices



Weight: 53 mg (Typ.)



Weight: 75 mg (Typ.)

Overview

The primary function of TC358764XBG/TC358765XBG is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1366×768 24-bit pixel resolution for single-link LVDS and up to WUXGA (1920x1200 18-bit pixels) resolution for dual-link LVDS. As a secondary function, the chip also supports an I^2C Master which is controlled by the DSI link; this may be used as an interface to any other control functions through I^2C. The chip can be configured through the DSI link by sending write register commands through DSI Generic Long Write-packets. It can also be configured through the I^2C Slave interface.

Features

- **DSI Receiver**
  - ✧ Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
  - ✧ Maximum bit rate of 800 Mbps/lane
  - ✧ Video input data formats:
    - RGB565 16 bits per pixel
    - RGB666 18 bits per pixel
    - RGB666 loosely packed 24 bits per pixel
    - RGB888 24 bits per pixel.
  - ✧ Video frame size:
    - Up to 1366×768 24-bit/pixel resolution to single-link LVDS display panel
    - Up to WUXGA resolutions (1920×1200 18-bit pixels) to dual-link LVDS display panel
  - ✧ Supports Video Stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set
  - ✧ Supports the path for Host to control the on-chip I^2C Master
- **LVDS FPD Link Transmitter**
  - ✧ Supports single-link or dual-link
  - ✧ Maximum pixel clock frequency of 85 MHz
  - ✧ Maximum throughput of 297.5 MBytes/sec for single-link or 595 Mbytes/sec for dual-link
  - ✧ Supports display up to 1366×768 24-bit/pixel resolution for single-link, or up to WUXGA (18 bit/pixel) resolutions for dual-link
  - ✧ Supports the following pixel formats:
    - RGB666 18 bits per pixel
    - RGB888 24 bits per pixel
  - ✧ Flexible mapping of parallel data input bit ordering
  - ✧ Supports power-down
- **System Operation**
  - ✧ Host configures the chip through DSI link
  - ✧ Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
  - ✧ Includes an I^2C Master function which is controlled by Host through DSI link (multi-master is not supported)
  - ✧ Power management features to save power
  - ✧ Configuration registers is also accessible through I^2C Slave interface
- **Clock Source**
  - ✧ LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
  - ✧ A built-in PLL generates the high-speed LVDS serializing clock requiring no external components
- **Digital Input/Output Signals**
  - ✧ All Digital Input signals are 3.3V tolerant
  - ✧ All Digital Output signals can output ranging from 1.8V to 3.3V depending on IO supply voltage
- **Power supply**
  - ✧ MIPI® DSI D-PHY: 1.2 V
  - ✧ LVDS PHY: 3.3 V
  - ✧ I/O: 1.8 V - 3.3V (all IO supply pins must be same level)
  - ✧ Digital Core: 1.2 V
- **Power Consumption**
  - ✧ Power –down mode is achieved by:
    1. Disable PLL (0x04A0[8] = 1) and LVDS (0x049C[0] = 0) after stopping video stream (in DSI LP11 state)
    2. Drive DSI Data Lanes to LP00 state
    3. Stop DSIClk and/or RefClk

✧ Power-down mode : Power Consumption: to 55 µW
- DSI-RX: 10.39 µA
- LVDS_1.2V: 3.10 µA
- LVDS_3.3V: 0.015 µA
- CORE: 31.96 µA
- IOs_1.8V: 0.15 µA

✧ Normal Operation (2-DSI Data lane @ 200 MHz, Single LVDS @ 27 MHz): to 157.58 mW
- DSI-RX 2 lanes 8.25 mA
- LVDS_3.3V: 42.68 mA
- LVDS_1.2V: 1.25 mA
- CORE 4.34 mA
- IOs_1.8V 0.067 mA

✧ Normal Operation (2-DSI Data lane @ 314 MHz, Dual LVDS @ 44.25 MHz each): to 259.16 mW
- DSI-RX 2 lanes: 9.77 mA
- LVDS_3.3V: 69.63 mA
- LVDS_1.2V: 7.78 mA
- CORE: 6.83 mA
- IOs_1.8V: 0.061 mA

- **Packaging Information**

✧ TC358765XBG : BGA64 (0.65mm ball pitch)
- Supports DSI-RX 4-data-lanes + Dual-Link LVDS-TX
- 6.0mm × 6.0mm × 1.2mm

✧ TC358764XBG : BGA49 (0.65mm ball pitch)
- Supports DSI-RX 4-data-lanes + Single-Link LVDS-TX
- 5.0mm × 5.0mm × 1.2mm

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Precautions and Usage Considerations Specific to Application Specific Standard Products and General-Purpose Linear Ics

Design

⚠ CAUTION

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. For details on how to connect a protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.

Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the Thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

Mounting

Installation to Heat Sink

Please install the power IC to the heat sink not to apply excessive mechanical stress to the IC. Excessive mechanical stress can lead to package cracks, resulting in a reduction in reliability or breakdown of internal IC chip. In addition, depending on the IC, the use of silicon rubber may be prohibited. Check whether the use of silicon rubber is prohibited for the IC you intend to use, or not. For details of power IC heat radiation design and heat sink installation, refer to individual technical datasheets or IC databooks.

Also please refer to ”RESTRICTIONS ON PRODUCT USE”.

REFERENCES

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8. Toshiba LVDS183 CMOS5LA (TC320) 3.3V Cell Information, V1r2, 9/8/2008
9. Toshiba Dual Link LVDS Transmitter CMOS5LA 85MHz Application Note, V. 1.5, 12/2/2008

1. Introduction

The TC358764XBG/TC358765XBG Functional Specification defines operation of the DSI-to-LVDS chip.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1366×768 24-bit pixel resolution for single-link LVDS and up to WUXGA (1920×1200 18-bit pixels) resolution for dual-link LVDS. As a secondary function, the chip also supports an I^2C Master which is controlled by the DSI link; this may be used as an interface to any other control functions through I^2C.

The chip can be configured through the DSI link by sending write register commands through DSI Generic Long Write-packets. It can also be configured through the I^2C Slave interface.

This specification provides description of two chip versions:

TC358764XBG: In BGA49 package, it supports DSI-RX with up to 4 data lanes, and outputs to Single-Link LVDS.

TC358765XBG: In BGA64 package, it supports DSI-RX with up to 4 data lanes, and outputs to Dual-Link LVDS.

1.1. Scope

This document details the operation of the chip, description of each major function that the chip supports, description of the configuration register set, and includes pinout, package, and electrical characteristics information.

1.2. Purpose

This document serves as the vehicle for exchanging detailed technical information of the DSI-TO-LVDS chip and its usage within the target application systems at the customer side. It also serves as the chip functional specification for design implementation and verification.

2. Device Overview

The DSI-TO-LVDS chip functions primarily as a DSI-to-LVDS communication protocol bridge, enabling video streaming from a Host processor over DSI link to drive LVDS-compatible display panels. In other words, the chip receives video stream input through its DSI receiver (DSI-RX), buffers the received pixel data in a buffer, and then re-transmits the video stream out through the LVDS transmitter.

As a secondary function, the chip also ports an I^2C Master which is controlled by the DSI link; this may be used as a programming interface to other peripherals in the system.

The chip is configured through the DSI link. Alternatively, it can optionally be configured through the I^2C Slave interface; in such case, the I^2C Master function would be disabled.

The reference video pixel clock for the LVDS link is sourced either from an external clock via input pin EXTCLK or derived from DSICLK. The chip integrates a PLL which synthesizes the high-speed clock for use solely to serialize video data over the LVDS link.

The DSI-RX receiver supports from 1- to 4-Lane configurations at bit rate up to 800 Mbps per lane. Host can transmit video in video mode. In video mode, Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only 1024-pixel of video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The LVDS transmitter supports a clock frequency of up to 85 MHz for either single- or dual-link. Correspondingly, the LVDS throughput is up to 297.5 Mbytes/sec for single-link or 595 Mbytes/sec for dual-link.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link.

3. Features

- **DSI Receiver**
  - ✧ Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
  - ✧ Maximum bit rate of 800 Mbps/lane
  - ✧ Video input data formats:
    - RGB565 16 bits per pixel
    - RGB666 18 bits per pixel
    - RGB666 loosely packed 24 bits per pixel
    - RGB888 24 bits per pixel
  - ✧ Video frame size:
    - Up to 1366×768 24-bit/pixel resolution to single-link LVDS display panel
    - Up to WUXGA resolutions (1920×1200 18-bit pixels) to dual-link LVDS display panel
  - ✧ Supports Video Stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set
  - ✧ Supports the path for Host to control the on-chip I^2C Master

- **LVDS FPD Link Transmitter**
  - ✧ Supports single-link or dual-link
  - ✧ Maximum pixel clock frequency of 85 MHz
  - ✧ Maximum throughput of 297.5 MBytes/sec for single-link or 595 Mbytes/sec for dual-link
  - ✧ Supports display up to 1366×768 24-bit/pixel resolution for single-link, or up to WUXGA (18 bit/pixel) resolutions for dual-link
  - ✧ Supports the following pixel formats:
    - RGB666 18 bits per pixel
    - RGB888 24 bits per pixel.
  - ✧ Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality equivalent to that of an RGB888 24-bit panel
  - ✧ Flexible mapping of parallel data input bit ordering
  - ✧ Supports power-down

- **System Operation**
  - ✧ Host configures the chip through DSI link
  - ✧ Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
  - ✧ Includes an I^2C Master function which is controlled by Host through DSI link (multi-master is not supported)
  - ✧ Power management features to save power
  - ✧ Configuration registers is also accessible through I^2C Slave interface

- **Clock Source**
  - ✧ LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
  - ✧ A built-in PLL generates the high-speed LVDS serializing clock requiring no external components

- **Digital Input/Output Signals**
  - ✧ All Digital Input signals are 3.3V tolerant
  - ✧ All Digital Output signals can output ranging from 1.8V to 3.3V depending on IO supply voltage

- **Power supply**
  - ✧ MIPI® DSI D-PHY: 1.2 V
  - ✧ LVDS PHY: 3.3 V
  - ✧ I/O: 1.8 V - 3.3V (all IO supply pins must be same level)
  - ✧ Digital Core: 1.2 V

- **Power** Consumption
  - ✧ Power –down mode is achieved by:
    1. Disable PLL (0x04A0[8] = 1) and LVDS (0x049C[0] = 0) after stopping video stream (in DSI LP11 state)
    2. Drive DSI Data Lanes to LP00 state
    3. Stop DSIClk and/or RefClk
  - ✧ Power-down mode : Power Consumption: to 55 µW
    - DSI-RX: 10.39 µA
    - LVDS_1.2V: 3.10 µA
    - LVDS_3.3V: 0.015 µA
    - CORE: 31.96 µA
    - IOs_1.8V: 0.15 µA
  - ✧ Normal Operation (2-DSI Data lane @ 200 MHz, Single LVDS @ 27 MHz): to 157.58 mW
    - DSI-RX 2 lanes 8.25 mA
    - LVDS_3.3V: 42.68 mA
    - LVDS_1.2V: 1.25 mA
    - CORE: 4.34 mA
    - IOs_1.8V: 0.067 mA
  - ✧ Normal Operation (2-DSI Data lane @ 314 MHz, Dual LVDS @ 44.25 MHz each): to 259.16 mW
    - DSI-RX 2 lanes 9.77 mA
    - LVDS_3.3V: 69.63 mA
    - LVDS_1.2V: 7.78 mA
    - CORE: 6.83 mA
    - IOs_1.8V: 0.061 mA

- **Packaging Information**
  - ✧ TC358765XBG : BGA64 (0.65mm ball pitch)
    - Supports DSI-RX 4-data-lanes + Dual-Link LVDS-TX
    - 6.0mm × 6.0mm × 1.2mm
  - ✧ TC358764XBG : BGA49 (0.65mm ball pitch)
    - Supports DSI-RX 4-data-lanes + Single-Link LVDS-TX
    - 5.0mm × 5.0mm × 1.2mm

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

4. Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8
VSS_LVDS2_12	LVTX2A	LVTX2B	LVTX2C	LVTX2DN	LVTX2EN	VSS_LVDS2_33	VSS_LVDS1_12
B1	B2	B3	B4	B5	B6	B7	B8
VDD_LVDS2_12	LVTX2A	LVTX2B	LVTX2C	LVTX2DP	LVTX2EP	VDD_LVDS2_33	VDD_LVDS1_12
C1	C2	C3	C4	C5	C6	C7	C8
VSSI	VDDI	GPIO	GPIO3	VDD_LVDS2_33	VSS_LVDS2_33	LVTX1AP	LVTX1AN
D1	D2	D3	D4	D5	D6	D7	D8
EXTCL	GPIO	GPIO	RESX	TM	VDD_LVDS1_33	LVTX1BP	LVTX1BN
E1	E2	E3	E4	E5	E6	E7	E8
VSS	VDD	GPIO	VDDC	VSSC	VSS_LVDS1_3	LVTX1CP	LVTX1CN
F1	F2	F3	F4	F5	F6	F7	F8
VSSI	VDDI	VDD_MIP	VSS_MIP	VSS_MIP	VDD_MIPI	LVTX1DP	LVTX1DN
G1	G2	G3	G4	G5	G6	G7	G8
I2C_SCL	DSRXD0	DSRXD1	DSRXC	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
H1	H2	H3	H4	H5	H6	H7	H8
I2C_SD	DSRXD0	DSRXD1	DSRXC	DSRXD2M	DSRXD3M	VDD_LVDS1_33	VSS_LVDS1_33

Figure 4.1 TC358765XBG Pin Layout (BGA64 – Top View)

A1	A2	A3	A4	A5	A6	A7
VSSIO	VDDIO	RESX	GPIO0	VSSC	VDDC	VSSC
B1	B2	B3	B4	B5	B6	B7
EXTCLK	VDDC	VSSC	TM	VDD_LVDS1_12	LVTX1AP	LVTX1AN
C1	C2	C3	C4	C5	C6	C7
I2C_SDA	GPIO3	GPIO2	GPIO1	VSS_LVDS1_12	LVTX1BP	LVTX1BN
D1	D2	D3	D4	D5	D6	D7
I2C_SCL	GPIO4	VSS_MIPI	VDD_MIPI	VSS_LVDS1_33	LVTX1CP	LVTX1CN
E1	E2	E3	E4	E5	E6	E7
VDDIO	VSSIO	VSS_MIPI	VDD_MIPI	VDD_LVDS1_33	LVTX1DP	LVTX1DN
F1	F2	F3	F4	F5	F6	F7
DSRXD0P	DSRXD1P	DSRXCP	DSRXD2P	DSRXD3P	LVTX1EP	LVTX1EN
G1	G2	G3	G4	G5	G6	G7
DSRXD0M	DSRXD1M	DSRXCM	DSRXD2M	DSRXD3M	VDD_LVDS1_33	VSS_LVDS1_33

Figure 4.2 TC358764XBG Pin Layout (BGA49 – Top View)

4.1. TC358765XBG BGA64 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	1.2 V
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	1.2 V
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 – negative	1.2 V
	VDD_MIPI	Power	2	MIPI® Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI® Analog Ground	GND
1st-Link LVDS-TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	3.3 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	3.3 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	3.3 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	3.3 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	3.3 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	3.3 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	3.3 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	3.3 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	3.3 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E – negative	3.3 V
	VDD_LVDS1_33	Power	2	First-link LVDS 3.3V Power Supply	3.3 V
	VSS_LVDS1_33	Ground	2	First-link LVDS 3.3V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	GND
2nd-Link LVDS-TX IF	LVTX2AP	LVDS-PHY	1	LVDS second-link data channel A - positive	3.3 V
	LVTX2AN	LVDS-PHY	1	LVDS second-link data channel A - negative	3.3 V
	LVTX2BP	LVDS-PHY	1	LVDS second-link data channel B - positive	3.3 V
	LVTX2BN	LVDS-PHY	1	LVDS second-link data channel B - negative	3.3 V
	LVTX2CP	LVDS-PHY	1	LVDS second-link data channel C - positive	3.3 V
	LVTX2CN	LVDS-PHY	1	LVDS second-link data channel C - negative	3.3 V
	LVTX2DP	LVDS-PHY	1	LVDS second-link data channel D (Clock) - positive	3.3 V
	LVTX2DN	LVDS-PHY	1	LVDS second-link data channel D (Clock) - negative	3.3 V
	LVTX2EP	LVDS-PHY	1	LVDS second-link data channel E - positive	3.3 V
	LVTX2EN	LVDS-PHY	1	LVDS second-link data channel E – negative	3.3 V
	VDD_LVDS2_33	Power	2	Second-link LVDS 3.3V Power Supply	3.3 V
	VSS_LVDS2_33	Ground	2	Second-link LVDS 3.3V Ground	GND
	VDD_LVDS2_12	Power	1	Second-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS2_12	Ground	1	Second-link LVDS 1.2V Ground	GND
I2C IF	I2C_SCL	S-OD	1	I^2C Master or Slave interface clock signal	1.8V-3.3V
	I2C_SDA	S-OD	1	I^2C Master or Slave interface data signal	1.8V-3.3V

GPIO	GPIO[4:0]	N_{PD}	5	GPIO bits 4-0	1.8V-3.3V
SYSTEM	RESX	N	1	Hardware reset, low active	1.8V-3.3V
	EXTCLK	N	1	External pixel clock source	1.8V-3.3V
	TM	N_{PD}	1	Test mode select	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	1.8-3.3V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	2	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO

N_{PD}: Normal IO with weak Internal Pull-Down

N_{PU}: Normal IO with weak Internal Pull-Up

S-OD: Pseudo open-drain output, schmitt input

SCHMIDTT: Fail Safe schmitt input buffer

DSI-PHY: front-end analog IO for DSI

LVDS-PHY: front-end analog IO for LVDS

A: Analog pad

4.2. TC358765XBG BGA64 Pin Count Summary

Table 4.1 TC358765XBG BGA64 Pin Count Summary

Group Name	Pin Count	Notes
DSI-RX IF	14	Include DSI Power & Ground
1st-Link /2nd-Link LVDS-TX IF	32	Include LVDS Power & Ground
I2C IF	2	-
GPIO	5	-
SYSTEM (POWER)	11	-
Total Pin Count	**64**	

4.3. TC358764XBG Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	1.2 V
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	1.2 V
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 - negative	1.2 V
	VDD_MIPI	Power	2	MIPI® Analog Power Supply	1.2 V
	VSS_MIPI	Ground	2	MIPI® Analog Ground	GND
LVDS-TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	3.3 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	3.3 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	3.3 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	3.3 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	3.3 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	3.3 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	3.3 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	3.3 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	3.3 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E – negative	3.3 V
	VDD_LVDS1_33	Power	2	First-link LVDS 3.3V Power Supply	3.3 V
	VSS_LVDS1_33	Ground	2	First-link LVDS 3.3V Ground	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	GND
I2C IF	I2C_SCL	S-OD	1	I^2C Master or Slave interface clock signal	1.8V-3.3V
	I2C_SDA	S-OD	1	I^2C Master or Slave interface data signal	1.8V-3.3V
GPIO	GPIO[4:0]	N	5	GPIO bits 4-0	1.8V-3.3V
SYSTEM	RESX	N	1	Hardware reset, low active	1.8V-3.3V
	EXTCLK	N	1	External pixel clock source	1.8V-3.3V
	TM	N	1	Test mode select	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	1.8-3.3V
	VSSIO	Ground	2	IO Ground	GND
	VDDC	Power	2	Digital Core Power Supply	1.2 V
	VSSC	Ground	3	Digital Core Ground	GND

Buffer Type Abbreviation:

N: Normal IO
S-OD: Pseudo open-drain output, schmitt input
SCHMIDTT: Fail Safe schmitt input buffer
DSI-PHY: front-end analog IO for DSI
LVDS-PHY: front-end analog IO for LVDS
A: Analog pad

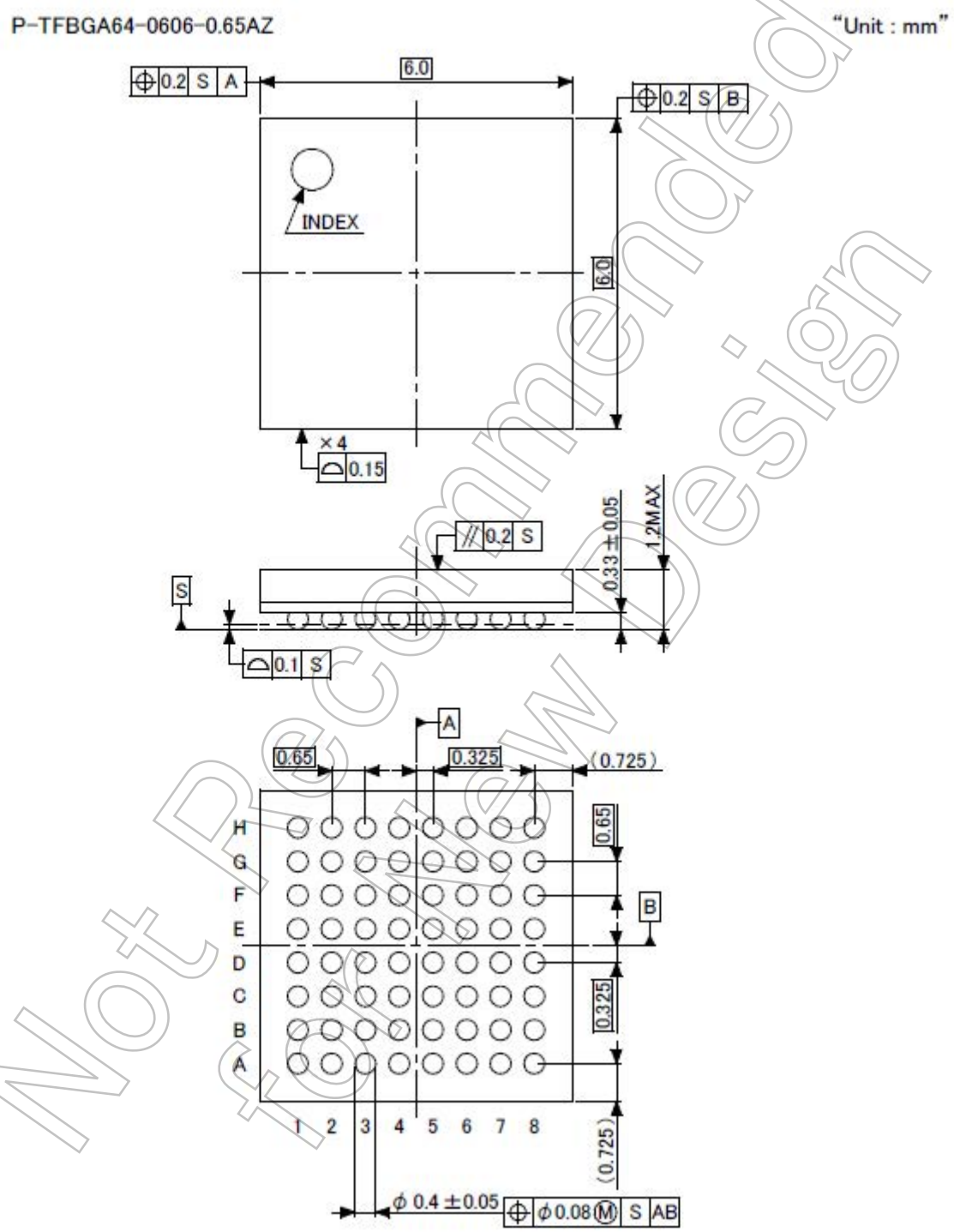
4.4. TC358764XBG BGA49 Pin Count Summary

Table 4.2 TC358764XBG BGA49 Pin Count Summary

Group Name	Pin Count	Notes
DSI-RX IF	14	Include DSI Power & Ground
LVDS-TX IF	16	Include LVDS Power & Ground
I2C IF	2	-
GPIO	5	-
SYSTEM (POWER)	12	-
Total Pin Count	**49**	

5. Package

All values are in mm unit.



Weight: 75 mg (Typ.)

Figure 5.1 P-TFBGA64-0606-0.65AZ (TC358765XBG) Package Drawing

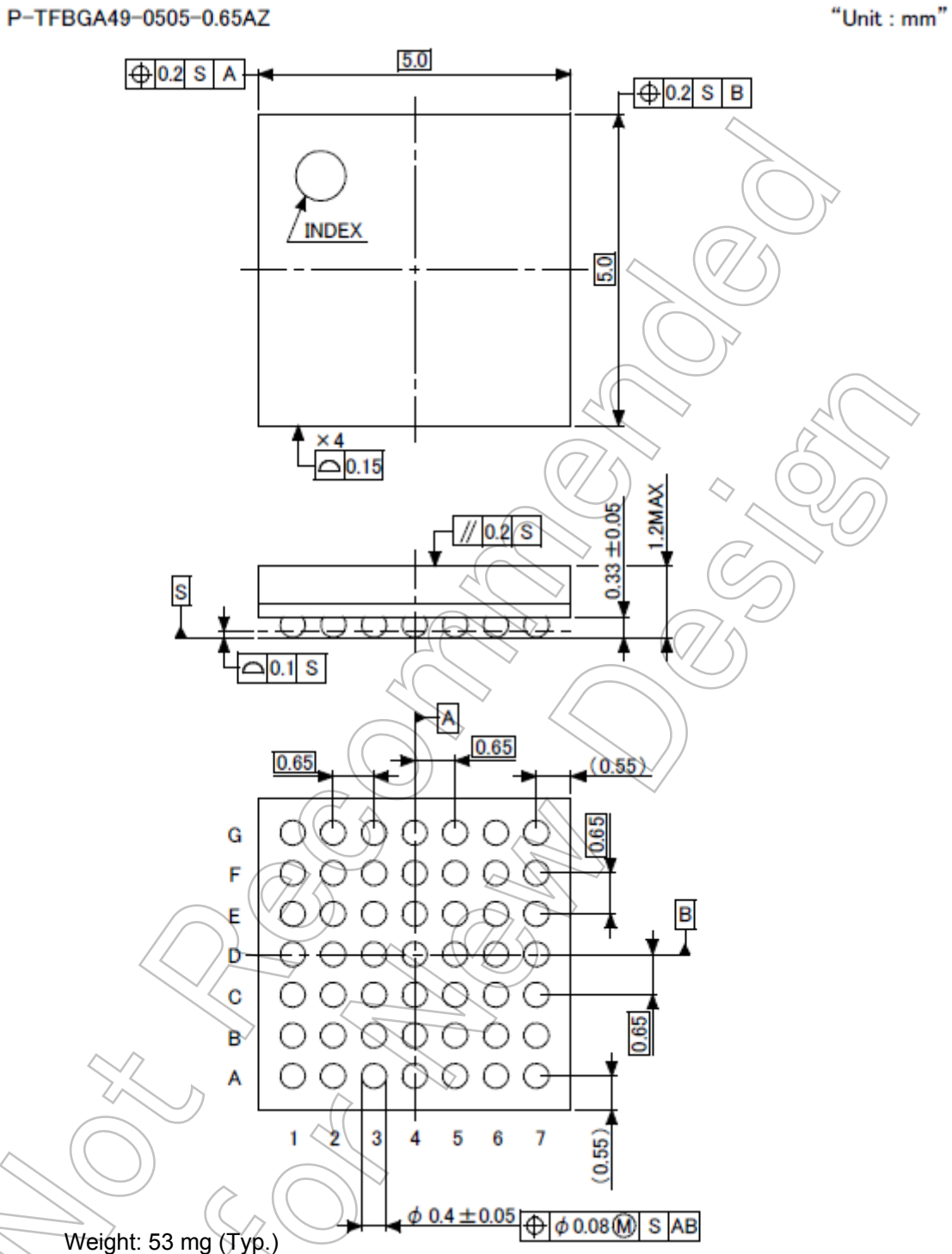


Figure 5.2 P-TFBGA49-0505-0.65AZ (TC358764XBG) Package Drawing

Table 5.1 DSI-TO-LVDS Package Information Summary

Package Type	Comment
BGA64 (TC358765XBG)	0.65 mm ball pitch
BGA49 (TC358764XBG)	0.65 mm ball pitch

6. Electrical characteristics

6.1. Absolute Maximum Ratings

Operating ambient Temperature range: Ta = -30°C - +85°C

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V – MIPI® DSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3V – LVDS PHY)	VDD_LVDS1_33, VDD_LVDS2_33	-0.3 to +3.9	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS1_12 VDD_LVDS2_12	-0.3 to +1.8	V
Input voltage (DSI I/O)	V_{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI I/O)	V_{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO+0.3	V
Output voltage (LVDS Driver)	V_{OUT_LVDS}	-0.3 to VDD_LVDS_33+0.3	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-40 to +125	°C

6.2. Operating Conditions

Table 6.2 TC358764XBG Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS1_12	1.1	1.2	1.3	V
Supply voltage (3.3V – LVDS PHY)	VDD_LVDS1_33	3.0	3.3	3.6	V
Supply voltage (1.2V – MIPI®-DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T_a	-30	+25	+85	°C
Supply Noise Voltage	V_{SN}	-	-	100	mV_{pp}

Table 6.3 TC358765XBG Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS1_12 VDD_LVDS2_12	1.1	1.2	1.3	V
Supply voltage (3.3V – LVDS PHY)	VDD_LVDS1_33 VDD_LVDS2_33	3.0	3.3	3.6	V
Supply voltage (1.2V – MIPI®-DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	T_a	-30	+25	+85	°C
Supply Noise Voltage	V_{SN}	-	-	100	mV_{pp}

6.3. DC Electrical Specification

All typical values are at normal operating conditions unless otherwise specified.

6.3.1. Normal CMOS I/Os DC Specifications

Table 6.4 Normal CMOS IOs DC Specifications

Parameter – CMOS I/Os	Symbol	Conditions	Min	Typ.	Max	Unit
Input voltage, High level Input Note1	V_{IH}	-	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level Input Note1	V_{IL}	-	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note 1,2	V_{IHS}	-	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note 1,2	V_{ILS}	-	0	-	0.3 VDDIO	V
Output voltage, High level Note1, 2	V_{OH}	I_{OH} = -0.4mA	0.8 VDDIO	-	VDDIO	V
Output voltage, Low level Note1, 2	V_{OL}	I_{OL} = 2mA	0	-	0.2 VDDIO	V
Input leakage current, High level on Normal pin or Pull-up I/O pin	I_{ILH1} (Note4)	V_{IN} = +VDDIO, VDDIO = 3.6V	-10	-	10	µA
Input leakage current, High level on Pull-down I/O pin	I_{ILH2} (Note4)	V_{IN} = +VDDIO, VDDIO = 3.6V	-	-	100	µA
Input leakage current, Low level On Normal pin or Pull-down I/O pin	I_{ILL1} (Note5)	V_{IN} = 0V, VDDIO = 3.6V	-10	-	10	µA
Input leakage current, Low level On Pull-up I/O pin	I_{ILL2} (Note5)	V_{IN} = 0V, VDDIO = 3.6V	-	-	-200	µA

Note1: Each power source is operating within recommended operating condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4: Normal pin or Pull-up I/O pin applied VDDIO supply voltage to Vin (input voltage)

Note5: Normal pin, or Pull-down I/O pin applied VSSIO (0V) to Vin (input voltage)

6.3.2. DSI Differential I/Os DC Specifications

6.3.2.1. LP Transmitter

The low power transmitter is used for driving the lines in all low-power operating modes. The DC characteristics of the LP transmitter are given below.

Table 6.5 DSI LP Transmitter DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V
Thevenin output low level	V_{OL}	-50	-	50	mV
Output impedance of the LP transmitter	Z_{OLP}	110	-	-	Ω

6.3.2.2. HS Receiver

The high-speed receiver is a differential line receiver with a switch able parallel input termination. It is used to receive data during high speed transmission from the host. The DC characteristics of the HS receiver are given below.

Table 6.6 DSI HS Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}		-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV
Differential input impedance	Z_{ID}	80	100	125	Ω

6.3.2.3. LP Receiver

The low-power receiver is used to detect the Low-Power state on each pin. It is used to receive data during low speed transmission from the host. The DC characteristics of the LP receiver are given below.

Table 6.7 DSI LP Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	-	-	550	mV

6.3.3. LVDS Transmitter DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Output voltage High Normal range (RLOAD = 100Ω±1%)	V_{OH}	-	-	1600	mV
Output voltage High Reduced range (RLOAD = 100Ω±1%)	V_{OH}	-	-	1500	mV
Output voltage Low Normal range (RLOAD = 100Ω±1%)	V_{OL}	900	-	-	mV
Output voltage Low Reduced range (RLOAD = 100Ω±1%)	V_{OL}	1000	-	-	mV
Output differential voltage Normal (RLOAD = 100Ω±1%)	$\|V_{OD}\|$	250	-	450	mV
Output differential voltage Reduced (RLOAD = 100Ω±1%)	$\|V_{OD}\|$	150	-	300	mV
Output Offset Voltage (Normal and Reduce range) (RLOAD = 100Ω±1%)	V_{OS}	1125	1250	1375	mV
Change in |VOD| between "0" and "1" (RLOAD = 100Ω±1%)	ΔV_{OD}	-	-	30	mV
Output offset voltage (RLOAD = 100Ω±1%)	ΔV_{OS}	-	-	25	mV
Output current (Driver shorted together)	I_{sab}	-	-	12	mA
Output current (Driver shorted to ground)	I_{sab}, I_{sb}	-	-	30	mA

6.3.4. LVDS Transmitter Supply Current

Parameter	Symbol	Min	Typ.	Max	Unit
Transmitter supply current (Clk + 4 data lanes) (75MHz – 3.3V supply current)	I_{TCCW}	-	45	65	mA
Transmitter power down supply current	I_{TCCS}	-	5	500	µA

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.281	2014-04-21	Newly released
1.282	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.31a	2017-10-13	Changed header, footer and the last page. Changed corporate name.
1.33	2018-04-04	Remove LVDS Clock Polarity function.

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