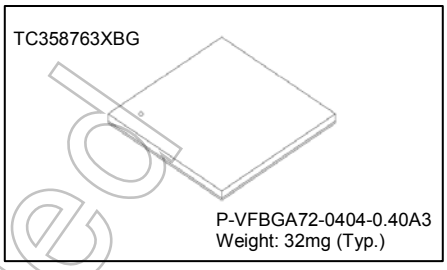
CMOS Digital Integrated Circuit Silicon Monolithic

TC358763XBG

Mobile Peripheral Devices



Overview

TC358763XBG provides data conversion between multiple input formats to a specified output format for mobile display systems. As the middle-range to high-end mobile phone sets are going to integrate higher-resolution, wider color depth, and larger size display in the clam-shell style body, connection between base body and display system is getting more difficult

TC358763XBG supports MIPI® DSI (Display Serial Interface) as a LCD interface. TC358763XBG also supports conventional LCD interface protocols; MIPI-DPI (Display Port Interface), MIPI-DBI (Display Bus Interface) as Host interface.

TC358763XBG can support 24-bit RGB Color format up to XGA size LCD module, when DPI is selected as Host interface. It also supports many different color format, and different LCD resolutions.

By using latest power saving technology, TC358763XBG can be controlled to minimize the power consumption in the target system.

Features

- LCD module interface
  - MIPI DSI-TX Data 3-lane, CLK 1-lane with data rates up to 500Mbps/lane
  - ✧ Support up to XGA size LCD panel. (When DPI is selected as host interface)
  - ✧ Output format: RGB888, RGB666 and RGB565.
  - ✧ Maximum LCD resolution setting size: 1024 × 1024
- Host interface
  - ✧ MIPI DPI 24-bit bus interface
  - ✧ MIPI DBI Type-B 16-bit bus interface
  - ✧ Serial input interface
    - 3 or 4-wire 8-bit SPI synchronous transfer
    - 3-wire 9-bit SSI synchronous transfer
- Peripheral control ports
  - ✧ SPI or SSI serial I/F ports
  - ✧ Single I^2C serial I/F port
  - ✧ Up to 13 General Purpose I/O ports
  - ✧ One PWM signals for LED intensity control
- PLL with 9.6MHz to 40MHz external reference clock to generate internal clock.
- Power supply
  - ✧ Core: 1.2 V ± 0.1 V
  - ✧ DSI I/O: 1.2 V ± 0.1 V
  - ✧ I/O: 1.8 V ± 0.1 V to 3.0 V ± 0.3 V
- Package
  - ✧ 4.5mm×4.5mm body, 72 ball, 0.4mm ball pitch, 1.0mm height (max)

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REFERENCES

1. MIPI Alliance Specification for D-PHY, Version 0.90.00 (October 8, 2007)
2. MIPI Alliance Specification for Display Serial Interface, Version 1.01.00 (February 21, 2008)
3. MIPI Alliance Specification for Display Bus Interface, Version 2.00 (November 29, 2005)
4. MIPI Alliance Specification for Display Pixel Interface(DPI-2), Version 2.00 (September 15, 2005)

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1. Overview

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By using latest power saving technology, TC358763XBG can be controlled to minimize the power consumption in the target system.

Figure 1.1 shows the system overview and a block diagram of TC358763XBG.

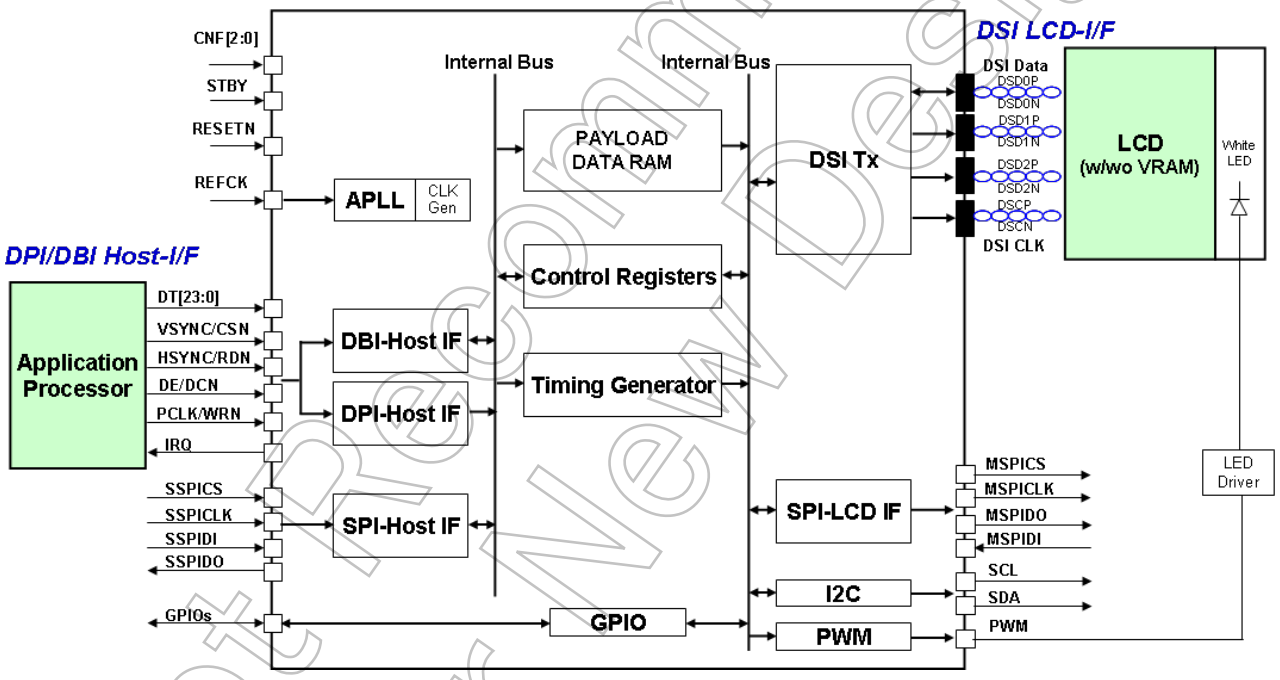

Figure 1.1 System Block Diagram of TC358763XBG

Pin Name Abbreviation:

GPIOs: GPIO0 to GPIO6

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2. Features

- LCD module interface
  - MIPI DSI-TX Data 3-lane, CLK 1-lane with data rates up to 500Mbps/lane
  - ✧ Support up to XGA size LCD panel. (When DPI is selected as host interface)
  - ✧ Output format: RGB888, RGB666 and RGB565.
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- Host interface
  - ✧ MIPI DPI 24-bit bus interface
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  - ✧ Serial input interface
    - 3 or 4-wire 8-bit SPI synchronous transfer
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- Peripheral control ports
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- PLL with 9.6MHz to 40MHz external reference clock to generate internal clock.

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  - ✧ Core: 1.2 V ± 0.1 V
  - ✧ DSI I/O: 1.2 V ± 0.1 V
  - ✧ I/O: 1.8 V ± 0.1 V to 3.0 V ± 0.3 V

- Package
  - ✧ 4.5mm×4.5mm body, 72 ball, 0.4mm ball pitch, 1.0mm height (max)

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3. External Pins

3.1. Pin layout

Top View

A1 VDDS	A2 DT10	A3 DT11	A4 AVSS	A5 AVSS	A6 AVSS	A7 AVSS	A8 VSSO	A9 VDDS
B1 VSSO	B2 DT9	B3 DE	B4 AVDD18	B5 AVSS	B6 AVDD12	B7 HSYNC	B8 DT12	B9 DT13
C1 PCLK	C2 STBY	C3 DT8	C4 GPIO1	C5 GPIO3	C6 VSYNC	C7 GPIO0	C8 DT14	C9 VDDC
D1 VDDC	D2 DT7	D3 CNF0	D4 No ball	D5 No ball	D6 No ball	D7 DT15	D8 DT16	D9 VSSC
E1 VSSC	E2 DT6	E3 GPIO4	E4 No ball	E5 No ball	E6 No ball	E7 GPIO2	E8 CNF2	E9 VSSO
F1 DT4	F2 DT3	F3 DT5	F4 No ball	F5 No ball	F6 No ball	F7 DT17	F8 DT20	F9 VDDS
G1 VSSO	G2 DT2	G3 GPIO5	G4 SCL	G5 DT21	G6 DT18	G7 DT19	G8 SDA	G9 REFCK
H1 VDDS	H2 DT1	H3 DSD0P	H4 DSCP	H5 VDDDS12	H6 DSD1P	H7 DSD2P	H8 RESETN	H9 DT22
J1 GPIO6	J2 DT0	J3 DSD0N	J4 DSCN	J5 VSSDS	J6 DSD1N	J7 DSD2N	J8 DT23	J9 CNF1

Figure 3.1 Ball layout (TC358763XBG)

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3.2. Signal Description

Table 3.1 shows the signal functionality of TC358763XBG.

Notation for Table 3.1;

1. “I/O” column shows direction of pin
   “I” means input pin. “O” means output pin. “I/O” means “Input / Output” pin.
   “NA” means “not applicable”.
2. “Type” column shows the type of IO pin
   “CMOS” means “CMOS” type input or inout pin. “CMOS” inout supports drive current value selection from 1mA, 2mA, 3mA, and 4mA by register settings. “SMT” means “Schmitt” type input or inout pin with pull-up/down control. “SMT” inout is 2mA drive current. “OD” means “Open Drain” type input or inout pin. “P” means Power supply. “G” means Ground.
3. “Initial” column shows the initial setting after reset with STBY=”H”.
   “In” means “Input pin, without pull-up nor pull-up resistor”. “PD” means “Input with internal pull-down”. “PU” means “Input internal pull-up”.
   “L” means “Low level output”. “H” means “High level output”, “Hi-Z” means “Hi-Impedance”. “NA” means “not applicable”. “NC” means “no connection”. No connection pin should be open.

   When STBY=”L”, all pin except for GPIO6, is Hi-Impedance state.

   GPIO6 is “PD” state even if STBY=”L”.

Note: Pull-up and Pull-down register is implemented by MOS Tr. They work as register only when IO power (VDDS) is supplied.

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Table 3.1 Signal Functionality of TC358763XBG

Group	Pin Name	Ball	I/O	Typ.	Initial	Function	Note
LSI Mode	CNF2	E8	I/O	SMT	In	LSI mode control pin, Configure Host Interface types	*1
	CNF1	J9	I/O	SMT	In		
	CNF0	D3	I/O	SMT	In		
Reset & Clock	RESETN	H8	I/O	SMT	In	System Reset Input L: Reset H: Operation	–
	REFCK	G9	I/O	CMOS	In	System Clock Input	–
	STBY	C2	I	CMOS	In	Sleep Enable L: Standby H: Operation	–
DBI/DPI	VSYNC	C6	I/O	CMOS	*4	This pin has multiple functions. DPI: VSYNC (Vertical synchronization signal) DBI Type B: CSN	–
	HSYNC	B7	I/O	CMOS	*4	This pin has multiple functions. DPI: HSYNC (Horizontal synchronization signal) DBI Type B: RDN	–
	DE	B3	I/O	CMOS	*5	This pin has multiple functions. DPI: DE (valid Data Enable) DBI Type B: DCN	–
	PCLK	C1	I/O	CMOS	*4	This pin has multiple functions. DPI: PCLK (Pixel Clock) DBI Type B: WRN	–
	DT[17:0]	-	I/O	CMOS	*5	Video Data. Bus width is selectable among 8, 16, 18 or 24 bits.	*2
GPIO	DT18	G6	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[18] DBI/DPI bus width select = 0: GPIO[7]	–
	DT19	G7	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[19] DBI/DPI bus width select = 0: GPIO[8]	–
	DT20	F8	I/O	CMOS	*5	This pin has multiple functions. DBI/DPI bus width select = 1: DT[20] DBI/DPI bus width select = 0: GPIO[9]	–
	DT21	G5	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO10 Function Select} = {1, x}: DT[21] {0, 1}: IRQ {0, 0}: GPIO[10]	–
	DT22	H9	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO11 Function Select} = {1, x}: DT[22] {0, 1}: PWM {0, 0}: GPIO[11]	–
	DT23	J8	I/O	CMOS	*5	This pin has multiple functions. { DBI/DPI bus width select, GPIO10 Function Select} = {1, x}: DT[23] {0, 1}: CLKOUT {0, 0}: GPIO[12]	–

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	GPIO0	C7	I/O	SMT	*7	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPICS else if GPIO0 Function Select [1:0] = [00]: GPIO0 [01]: IRQ [10]: PWM [11]: Reserved	
	GPIO1	C4	I/O	CMOS	*6	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPICLK else if GPIO1 Function Select [1:0] = [00]: GPIO1 [01]: IRQ [10]: CLKOUT [11]: Reserved	
	GPIO2	E7	I/O	SMT	*7	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100]:SSPIDI else if GPIO2 Function Select [1:0] = [00]: GPIO2 [01]: IRQ [10]: TE [11]: Reserved	
	GPIO3	C5	I/O	CMOS	H	This pin has multiple functions. If CNF[2:0]=[001 or 010 or 011 or 100] & Slave SPI CS bypass output enable = [1] :SSPICS bypass output else if {Master SPI Enable} = [1]: MSPICS (Master SPI Chip Select) else GPIO3 Function Select} = [00]: GPIO3 [01]: CLKOUT [10]: Host image write line end pulse output [11]: Reserved	–
	GPIO4	E3	I/O	CMOS	L	This pin has multiple functions. {Master SPI Enable, GPIO4 Function Select} = [0,00]: GPIO4 [0,01]: PWM [0,10]: HDE output [0,11]: Reserved [1,xx]: MSPICLK (Master SPI Clock)	
	GPIO5	G3	I/O	CMOS	L	This pin has multiple functions. {Master SPI Enable, GPIO5 Function Select} = [0,0]: GPIO5 [0,1]: IIRQ [1,x]: MSPIDOI (Master SPI Data Out/In)	

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	GPIO6	J1	I/O	SMT	PD	This pin has multiple functions.
						If CNF[2:0]=[001 or 010 or 011 or 100] {
						If {Slave SPI 4-wire Enable,
						Slave SPI CS bypass output enable} =
						[0, 1]: SSPICS bypass output
						[1, x]: SSPIDO (Slave SPI Data Out)
						}
						}
						else if {Master SPI Enable,
						Master SPI CS pin select,
						GPIO6 Function Select [2:0]} =
						[1, 1, xx]: MSPICS2 (Master SPI CS2)
						[1, 0, xx]: MSPIDI (Master SPI Data In)
						[0, x, 11]: IRQ
						[0, x, 10]: PWM
						[0, x, 01]: TE
						[0, x, 00]: GPIO6	

I2C (master)	SCL	G4	O	OD	Hi-Z	I^2C Clock signal (Master)	–
	SDA	G8	I/O	OD	Hi-Z	I^2C Data signal (Master)	
DSI special I/O	DSD0P	H3	I/O	NA	NA	DSI Data Lane 0 Positive Input/Output	*1
	DSD0N	J3	I/O	NA	NA	DSI Data Lane 0 Negative Input/Output	
	DSD1P	H6	O	NA	NA	DSI Data Lane 1 Positive Output	
	DSD1N	J6	O	NA	NA	DSI Data Lane 1 Negative Output	
	DSD2P	H7	O	NA	NA	DSI Data Lane 2 Positive Output	
	DSD2N	J7	O	NA	NA	DSI Data Lane 2 Negative Output	
	DSCP	H4	O	NA	NA	DSI Clock Positive Output	
	DSCN	J4	O	NA	NA	DSI Clock Negative Output	
Power & Ground	VDDC	-	-	P	NA	VDD for Internal Core(1.2 V)	*3
	VDDS	-	-	P	NA	VDD for I/O	
	VDDDS12	H5	-	P	NA	VDD for DSI Analog (1.2 V)	
	VSSDS	J5	-	G	NA	VSS for DSI	
	AVDD12	B6	-	P	NA	Internal Analog core Power Please connect to AVSS	
	AVDD18	B4	-	P	NA	Internal Analog core Power Please connect to AVSS	
	AVSS	-	-	G	NA	VSS for Internal Analog Core	
	VSSC	-	-	G	NA	Ground for Internal Core	
	VSSO	-	-	G	NA	Ground for I/O	

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*1: CNF[2:0] pin is used for Operation mode configuration of TC358763XBG. LCD Interface Configuration is specified by register settings. Initial State will change by the CNF[2:0] setting.

Table 3.2 CNF[2:0] Host I/F Configuration (LSI Mode)

CNF[2:0]	LSI Mode	Host I/F Configuration	Initial State				Note
			*4	*5	*6	*7	
000	-	Reserved	-	-	-	-	LSI Test mode
001	-	Reserved	-	-	-	-	LSI Test mode
010	-	Reserved	-	-	-	-	LSI Test mode
011	Mode 2-1	DPI + SPI slave	In	In	In	In	-
100	Mode 2-2	DPI + SSI slave	In	In	In	In	-
101	Mode 3	DBI Type-B	In	In	L	PD	-
110	-	Reserved	-	-	-	-	LSI Test mode
111	-	Reserved	-	-	-	-	LSI Test mode

*2: DT[23:0] pin assignment

Table 3.3 DT[23:0] pin assignment

DT	Loc	DT	Loc	DT	Loc	DT	Loc	DT	Loc	DT	Loc
[23]	J8	[19]	G7	[15]	D7	[11]	A3	[7]	D2	[3]	F2
[22]	H9	[18]	G6	[14]	C8	[10]	A2	[6]	E2	[2]	G2
[21]	G5	[17]	F7	[13]	B9	[9]	B2	[5]	F3	[1]	H2
[20]	F8	[16]	D8	[12]	B8	[8]	C3	[4]	F1	[0]	J2

*3: VDD/VSS pin assignment

All VSS pins (VSSDS, VSSC,VSSO and AVSS) have to be connected to Ground. DSI analog power supply pin have to connect 1.2 V power supply for both with/without DSI use case.

Table 3.4 VDD/VSS pin assign

Name	Pin					Function
VDDC	C9	D1	-	-	-	VDD for Internal Core
VDDS	A1	A9	F9	H1	J5	VDD for I/O
VSSC	D9	E1	-	-	-	VSS for Internal Core
VSSO	A8	B1	E9	G1	-	VSS for I/O
AVSS	B5	A4	A5	A6	A7	VSS for Internal Analog Core

*A4, A5, A6, A7 can be tied to GND or can be left open.

*4 to *7: Refer to Initial state field of Table 3.2.

*8: If signals are not used, please connect as follows.

DT16 to DT23: GND

SDA and SCL: GND

GPIO3 to GPIO6: Open

DSD1P, DSD1N, DSD2P, DSD2N: Open

GPIO0 to GPIO2: Open (Mode3 (CNF[2:0]=101) only)

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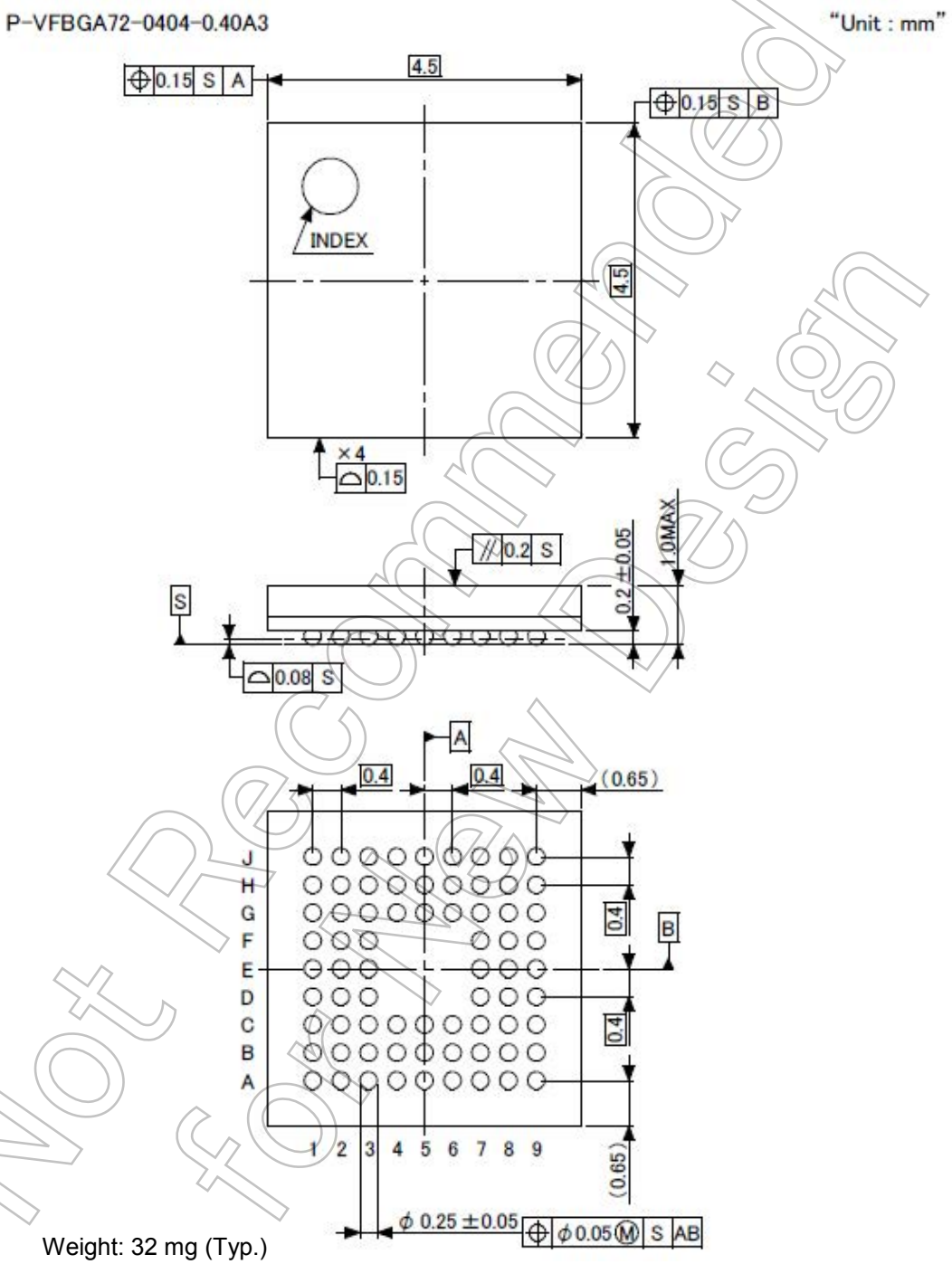
4. Package

4.1. Package Dimensions (P-VFBGA72-0404-0.40A3)



Weight: 32 mg (Typ.)

Figure 4.1 Package Dimensions of TC358763XBG

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5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS= 0V reference

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply voltage	VDDS	-0.3 to +3.9	V
	VDDDS12	-0.3 to +1.8	V
	VDDC	-0.3 to +1.8	V
Input voltage	VIN	-0.3 to VDDS+0.3	V
Output voltage	VOUT	-0.3 to VDDS+0.3	V
Input Current	IIN	-10 to +10	mA
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS= 0V reference

Table 5.2 Operation Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply voltage	VDDS	1.7	-	3.3	V
	VDDDS12	1.1	1.2	1.3	
	VDDC	1.1	1.2	1.3	
Operating frequency (internal system clock)	Fopr	-	-	125	MHz
Operating temperature	Ta	-20	-	+85	°C

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6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.60g	2014-04-10	Newly released
1.61	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.71	2017-11-09	Corrected *2 in section 3.2. Changed header, footer and the last page. Changed corporate name.

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