APPLICATION NOTE (Summary)
TC90106FG

1. Overview

TC90106FG is video decoder which has three ADCs. It supports input signal of CVBS, Y/C, and YCbCr up to 525p/625p. In addition, it has picture quality improver and vertical enhancer.

2. Feature

- ITU-R BT.656 format output for CVBS, Y/C, 525i and 625i input signal
- 8 bit 54MHz clock mode embedded SAV and EAV for 525p, 625p input signal
- Built-in picture quality improver and vertical enhancer
- Operated by I^2C Bus control
- Power supply **:** 3.3V, 2.5V, 1.5V
- Package **:** LQFP 64pin 10 x 10 mm (LQFP64-P-1010-0.50E)

3. An example of application circuit

Figure 3-1 is an example of Application circuit.
It requires device for displaying the ITU-R BT.656 signal and I^2C control device.

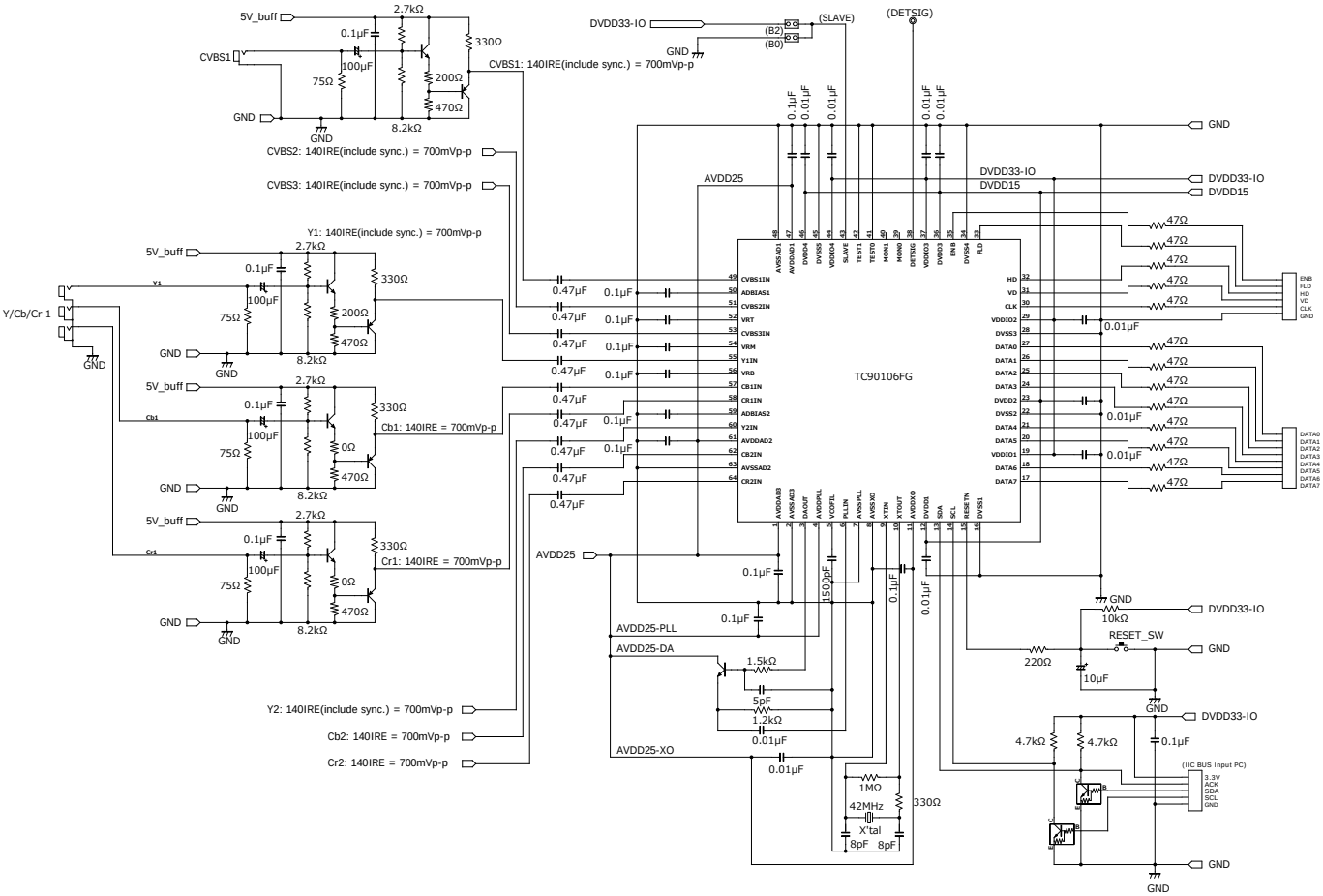


Figure 3-1 An example of Application circuit

4. Terminal Function

(1) PLL Block for generating system clock

TC90106FG has a PLL circuit which generates system clock. In addition, system clock synchronizes with horizontal synchronization signal of input signal. Please refer to another document about an example of PLL circuit.

・Terminal 3**:** It outputs signal of an internal DAC.

DAC output is HPLL phase comparator signal. It outputs 6.75MHz and inputs the emitter follower output signal to terminal 6 via 0.01μF after connecting R and C.

・Terminal 5**:** It is a terminal for VCO control.

This is a terminal of control signal for oscillated internal VCO. It connects 1500pF between terminal and GND.

・Terminal 6**:** It inputs signal of HPLL.

It inputs 6.75MHz output signal from terminal 3. It is connected internal phase comparator. It makes the phase comparison with the divided signal from VCO output signal to 6.75MHz rate, and it controls VCO.

(2) The block for the crystal oscillator

It uses the crystal oscillator of the 42MHz fundamental type. Please refer to the “<Supplementary explanation related to the peripheral circuit>”.

(3) I^2C terminal

・Terminal 13: It is input signal for SDA of I^2C control.

・Terminal 14: It is input signal for SCL of I^2C control.

Withstand voltage of terminal for SDA and SCL are 5V.

・Terminal 43: It is for slave address setting.

When terminal voltage is 3.3V, slave address is B2. When terminal voltage is GND, it is B0.

(4) Reset control

・Terminal 15: It is for RESET control. It is usually 3.3V(High). Please set to GND (LOW) level when It makes a reset.

Period of the reset(Low), the video output are set to high impedance.

(5) Digital output

・Terminal 17 (MSB), 18, 20, 21, 24, 25, 26, 27 (LSB): They are for output video signal. They connect to the next stage via a damping resistor.

・Terminal 30: It is for digital clock output. It outputs 27MHz at ITU-R BT.656 mode. In addition, it outputs 54MHz when input signal is component input (525p/625p) mode. It connects to the next stage via a damping resistor. Clock Polarity is set by the INVCK of Sub address 29h.

(6) Synchronous signal output. It outputs ITU-R BT.656 signal and synchronous signal.

・Terminal 31: It outputs Vertical synchronous signal. It connects to the next stage via a damping resistor. Signal phase is set by HV601 of Sub address 25h and polarity is set by PVPOLE of sub address 29h.

・Terminal 32: It outputs Horizontal synchronous signal. It connects to the next stage via a damping resistor. Polarity is set by PHPOLE of Sub address 29h.

(7) Other signal output

・Terminal 33: It outputs Field signal. It connects to the next stage via a damping resistor. Polarity is set by PFPOLE of Sub address 29h.

・Terminal 35: It outputs Enable signal. It connects to the next stage via a damping resistor.

・Terminal 38: It outputs detection signal of presence for the signal condition or non-signal condition. It can set ON / OFF function of operating independently from the I^2C read. Setting of detection sensitivity is set by Sub address 26h at NOSIG_MODE[1:0], NOSIG_O,NOSIG_VE[1:0], NOSIG_VS[1:0].

ON / OFF function of the terminal 38 is set by the Sub address 00h NOSIG_EN. Setting of the detection sensitivity is only valid in the terminal 38.

(8) Input signal

Selection of the input signal format is set by INSEL[1:0] of Sub address 01h.
Selection of CVBS input terminal is set by YSWSEL[1:0] of Sub address 02h.
Selection of YCbCr1 and YCbCr2 input or Y/C1 and Y/C2 input are set by YCBCR_SEL [1:0] of Sub address 03h.
Selection of 525i/625i or 525p/625p in YCbCr input is set by PROGSEL of Sub address 02h. (525i and 625i, or 525p and 625p are automatic detection)
In addition, it has a detection circuit of 525p/625p independently at NOSIGD2 of Read register.

Terminal 49, 51, 53**:** Input terminal of CVBS signal.
Input CVBS signal amplitude adjust 0.7Vpp between sync bottom and white 100%, and it inputs each terminals through 0.47µF capacitor.
The color decoder system corresponds to the world wide system.
It has a manual setting and automatic detection mode.(Sub address:02h)
Pedestal offset level of output can select at NTSCJM of Sub address 03h.

Color system detection method has four type. It can select detection mode at FSCAUTO of Sub address 02h.

Register(01h) FSCAUTO	Mode	fsc detection	Detail
00	Manual	—	Color system is set by manual control at register:TVM0-TVM3 (TVM0 - TVM3 ＝ Bank 00h Sub address:01h)
01	Europe	4.4336MHz 3.57954MHz	Priority of detection ： 4.43MHz PAL→ NTSC→ SECAM (It cannot detect PAL of 3.58MHz)
10	South America	3.57954MHz 3.5756MHz 3.5820MHz	Priority of detection ： 3.58MHz PAL→ 3.58MHz NTSC (It cannot detect fsc of 4.43MHz)
11	Full multi	4.4336MHz 3.57954MHz 3.5756MHz 3.5820MHz	Priority of detection ： PAL→ NTSC→ SECAM

There is no priority for vertical frequency (50/60Hz).
VD output is controlled by register VDSEL (Sub address 1Eh).
00 : It synchronizes with input signal continuously.
01 : When it detects no signal input, to use the most recent detection result.
1*: VD frequency is set by the value of register TVM[2], when FSCAUTO is [00].

・Terminal 55**:** It is a Y signal input terminal for YCbCr1 or Y/C1.
The Y signal amplitude adjust 0.7Vpp between sync bottom and white 100%, and it inputs the terminal through 0.47µF capacitor.

・Terminal 57**:** It is a Cb1 input terminal for YCbCr1 or C input terminal for Y/C1.
The Cb1 signal at 100% color is adjusted to 0.7Vpp, and it inputs the terminal through 0.47µF capacitor.

・Terminal 58**:** It is a Cr1 input terminal for YCbCr1 or C input terminal for Y/C1.
The Cr1 signal at 100% color is adjusted to 0.7Vpp, and it inputs the terminal through 0.47µF capacitor.

・Terminal 60 ： It is a Y signal input terminal for YCbCr2 or Y/C2.
The Y signal amplitude adjust 0.7Vpp between sync bottom and white 100%, and it inputs the terminal through 0.47µF capacitor.

・Terminal 62**:** It is a Cb2 input terminal for YCbCr2 or C input terminal for Y/C2.
The Cb2 signal at 100% color adjust 0.7Vpp, and it inputs the terminal through 0.47µF capacitor.

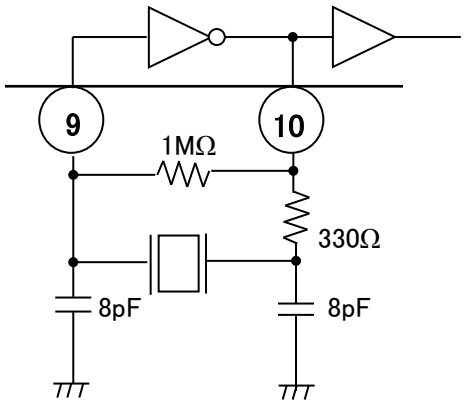
・Terminal 64**:** It is a Cr2 input terminal for YCbCr2 or C input terminal for Y/C2.
The Cr2 signal at 100% color adjust to 0.7Vpp, and it inputs the terminal through 0.47µF capacitor.

<Supplementary explanation related to the peripheral circuit>

Oscillation block by the crystal oscillator

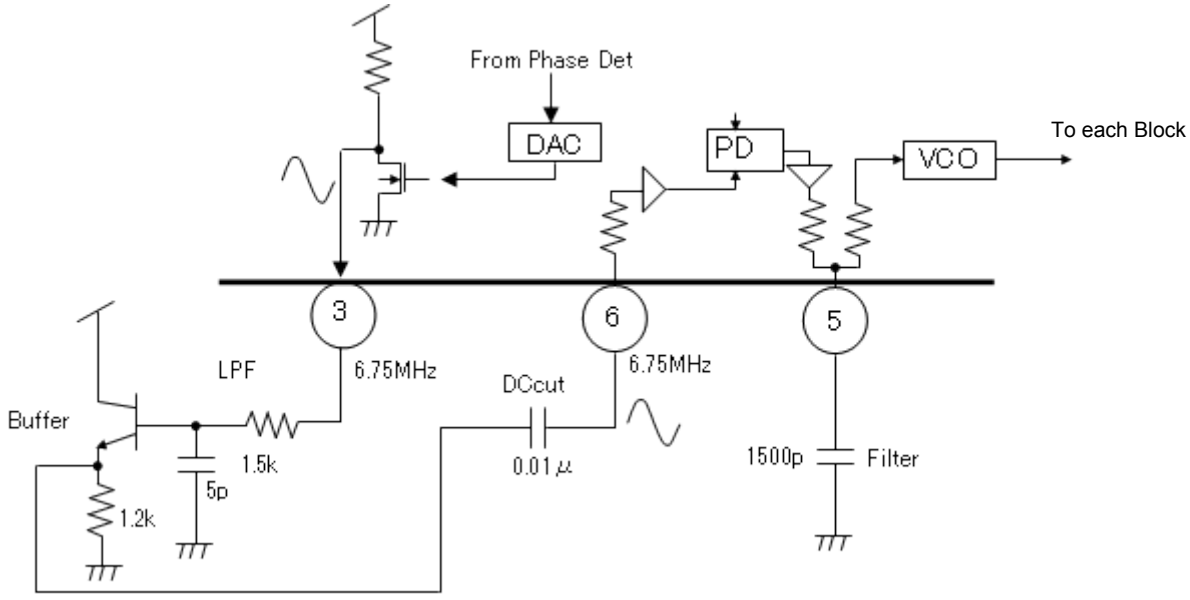
It shows an example of the fundamental oscillation circuit.
Please select a constant of parts from evaluating the oscillation characteristics in the board.
Please choose the crystal oscillator of the fundamental frequency 42MHz, and small frequency deviation.
The frequency deviation influences the pull-in range of fsc.
When deviation is + 50ppm, the center of the pull-in range of fsc is shifted to the + 179Hz at NTSC and 222Hz at PAL. e.g. 179Hz (50ppm of 3.579545MHz) at NTSC and 222Hz at PAL.
When pull-in range is -500Hz to +500Hz, the frequency range shifts to (-500+179)=-321Hz to (+500+179)=+679Hz at NTSC.
The pull-in range of fsc is possible to change by 16h_D6,

- Normal Mode 16h_D6=0 fsc±500Hz
- Wide Mode 16h_D6=1 fsc±800Hz



Peripheral circuit of PLL block

In this part, it gets the VCO output which is locked to the input horizontal synchronization signal by the PLL circuit.
The following circuit is an example circuit.



5. Picture quality adjustment

5.1. Y signal processing

5.1.1. Vertical enhancer

This function is detection of the non-correlation component in the vertical direction.
It is possible to set the vertical direction coring, gain and nonlinear-characteristics
Related registers, Sub address 04h:GVENH[2:0], VEN[1:0]
Sub address 03h:VEC[1:0]

5.1.2. LTI (Y edge correction)

The inclination correction of the horizontal edge of Y signal.
Related registers, Sub address 07h:FLTI
Sub address 06h:GLTI[1:0], LTILIM[1:0]

5.1.3. Sharpness

f0 is selectable from 4.2MHz or 3.3MHz. It is independent of LTI.

Related registers, Sub address 05h:FENH, GHENH[4:0]

5.1.4. Noise canceller

f0 is common setting to sharpness.

Related registers, Sub address 05h:FENH, NCLIM[1:0]
Sub address 04h:GNC[1:0]

5.1.5. Contrast control

Control range is 0.5 times to 2.4 times.

Related registers, Sub address 08h:YCONT[7:0]
Note. Output might be saturated when the input is large.

5.1.6. Brightness control

Adjustment for setup level in the effective picture period.
Related registers, Sub address 09h:YBRIT[7:0]

5.1.7. Mute control

This is mute function.

Y output is fixed to the pedestal level, and Cb/Cr output is fixed to the center level.
Related register, Sub address 0Dh:MUTE

5.2. Chroma signal processing

5.2.1. ACC (Auto Color Control)

It is available for CVBS and Y/C input.
Reference level is set by ACC register.
Related registers, Sub address 0Eh:ACC[3:0]

5.2.2. Killer control

It is available for CVBS input and Y/C input.
Sensitivity is set by CKILL register.
When it detects no color, CVBS signal is outputted to Y output.
Related registers, Sub address 0Eh:CKILL[2:0], 3LOFF

5.2.3. HUE control

It is available for CVBS input and Y/C input of NTSC signal.
It can control Demodulation phase adjustment and demodulation angle adjustment.
Related registers, Sub address 0Ch:HUE[6:0], 0Dh:HUE BIAS[5:0]

5.2.4. Sub color gain control

It can control Cb/Cr gain independently at an effective picture period.
Gain control range : 0.5 times to 1.4 times
Related registers, Sub address 0Ah:RGAIN[3:0], BGAIN[3:0]

5.2.5. Cb/Cr Offset adjustment

It can control Cb/Cr offset independently at an effective picture period.
Offset control range is -8LSB to +7LSB.
Related registers, Sub address 0Bh:ROFS[3:0], BOFS[3:0]

5.2.6. CTI (Color edge correction)

The inclination correction of the horizontal edge for Cb and Cr signal.
Related registers, Sub address 07h:FCTI, CTILIM[1:0], GCTI[1:0]

5.2.7. Filtering of Cb / Cr output stage

It can control a band-limited to the Cb / Cr signal output.
Related registers, Sub address 14h:FILON[1:0]

5.2.8. Muting of Cb / Cr

It can set mute control only color signal output.
Related registers, Sub address 0Dh:C MUTE

6. Other features

6.1. Blue back control

It automatically outputs the blue picture by detecting the non-signal.
Picture color is set at Sub address 33h, 34h and 35h.
Detection sensitivity is set by following register.
Related registers, Sub address 32h: BBACK_MODE[1:0], BBACKVE[1:0], BBACKVS[1:0], BBACK_AUTO, BBACK
Sub address 33h: BBACKY[7:0]
Sub address 34h: BBACKCB[7:0]
Sub address 33h: BBACKCR[7:0]

6.2. Power-down and power-saving of ADC

It has one 10bit ADC for CVBS/Y signal and two 8bit ADCs for color signal.
These ADC's operation status can be controlled by register.
Related registers, Sub address 38h: ADPWD10, ADPW8, ADPWS10, ADPWS8

6.3. NTSC-M mode

Input signal for NTSC is designed as NTSC-J. It has exclusive register for NTSC-M.
It can control pedestal level and gain for Y signal of NTSC-M.
Related registers, Sub address 03h: NTSCJM
Sub address 3Eh: BKOFST[7:0]
Sub address 3Fh: BKLVL[7:0]

6.4. Read register

It can read detected results for input signal format.

7. I²C BUS setting

(1) I²C Bus control

The TC90106FG can be controlled by the I²C bus. And supported up to 400kbit/s. Slave address can be selected at terminal 43. (Low : B0h / High : B2h)

It shows the basic of the bus control in Figure 7-1.
Basic transfer is order is : slave address - sub-address - data.

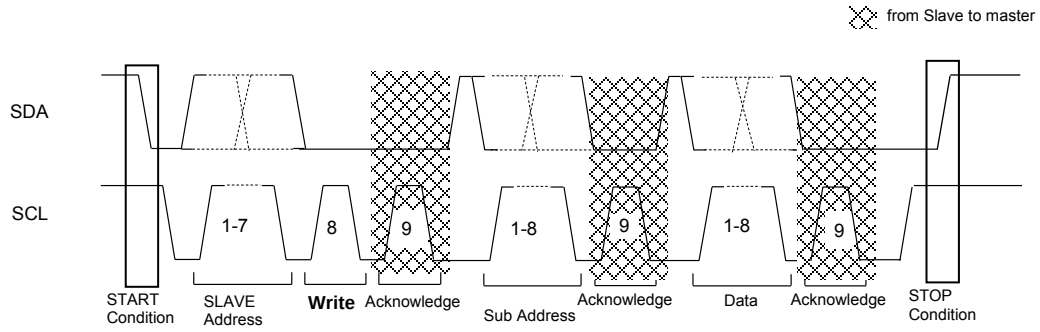


Figure 7-1 Bus control timing (Basic mode)

It shows the write mode and auto-increment mode is shown in Figure 7-2 and Figure 7-3.

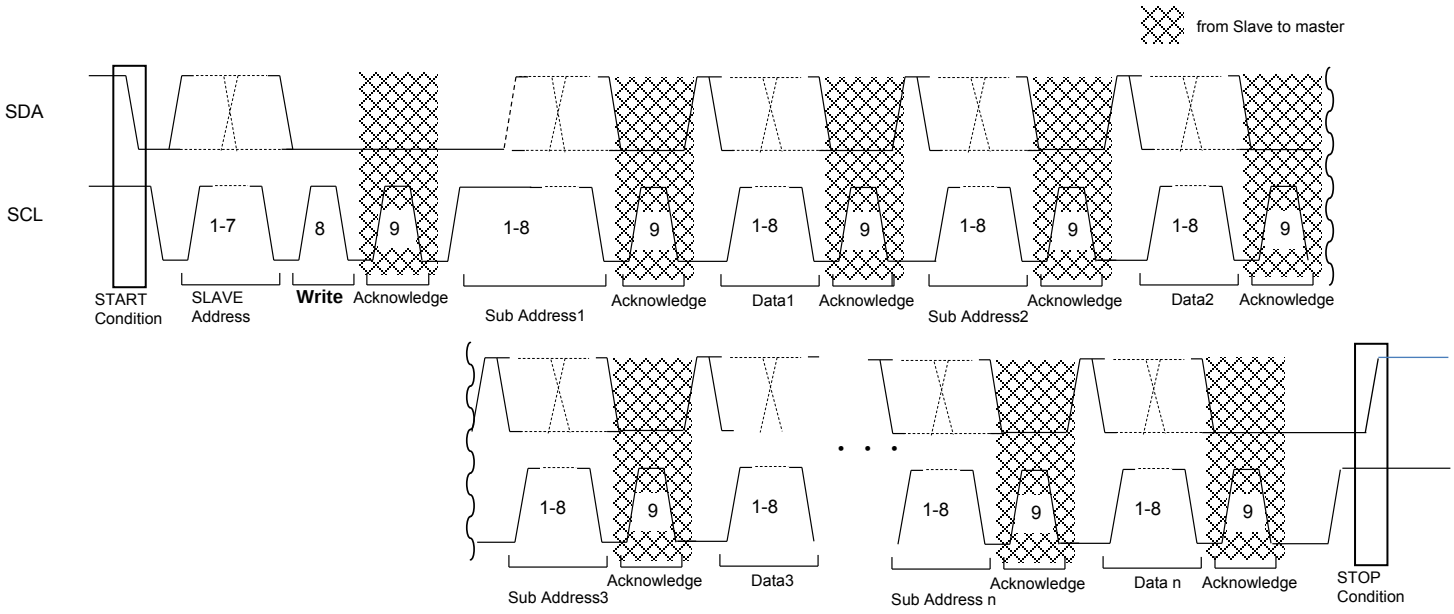


Figure 7-2 Bus control timing (Write mode)

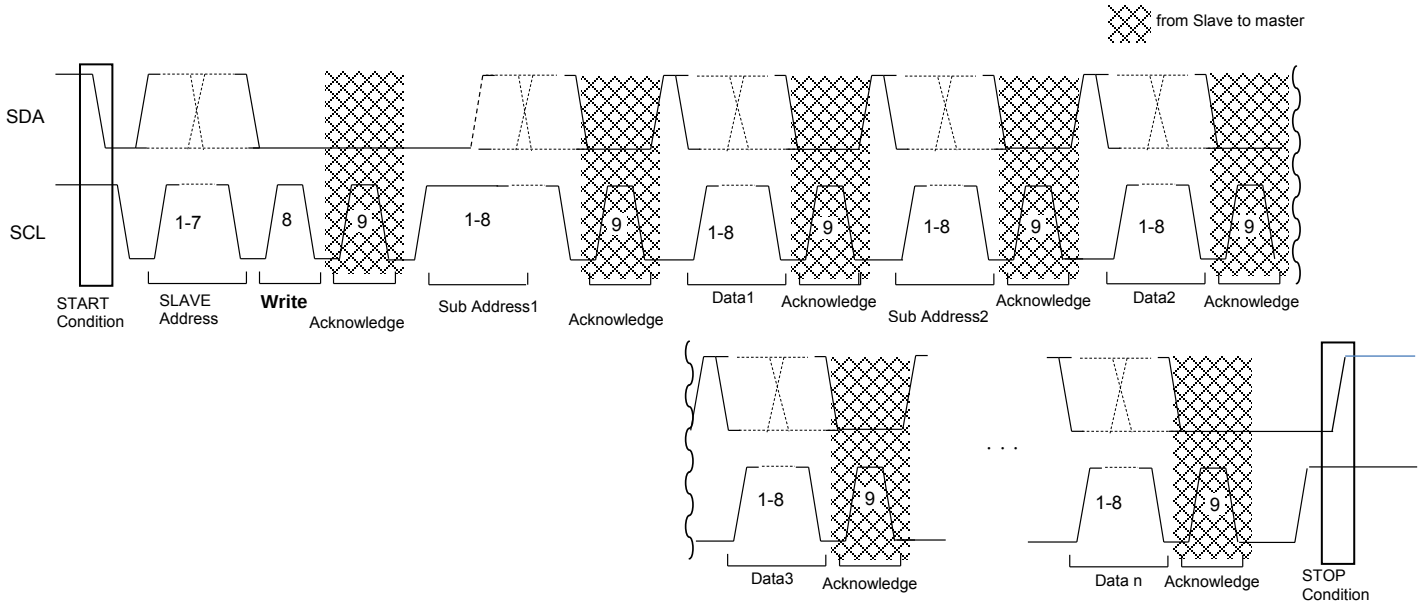


Figure 7-3 Bus control timing (auto increment mode)

It shows the reading format of the set value & status (50h to 54h) in Figure 7-4.

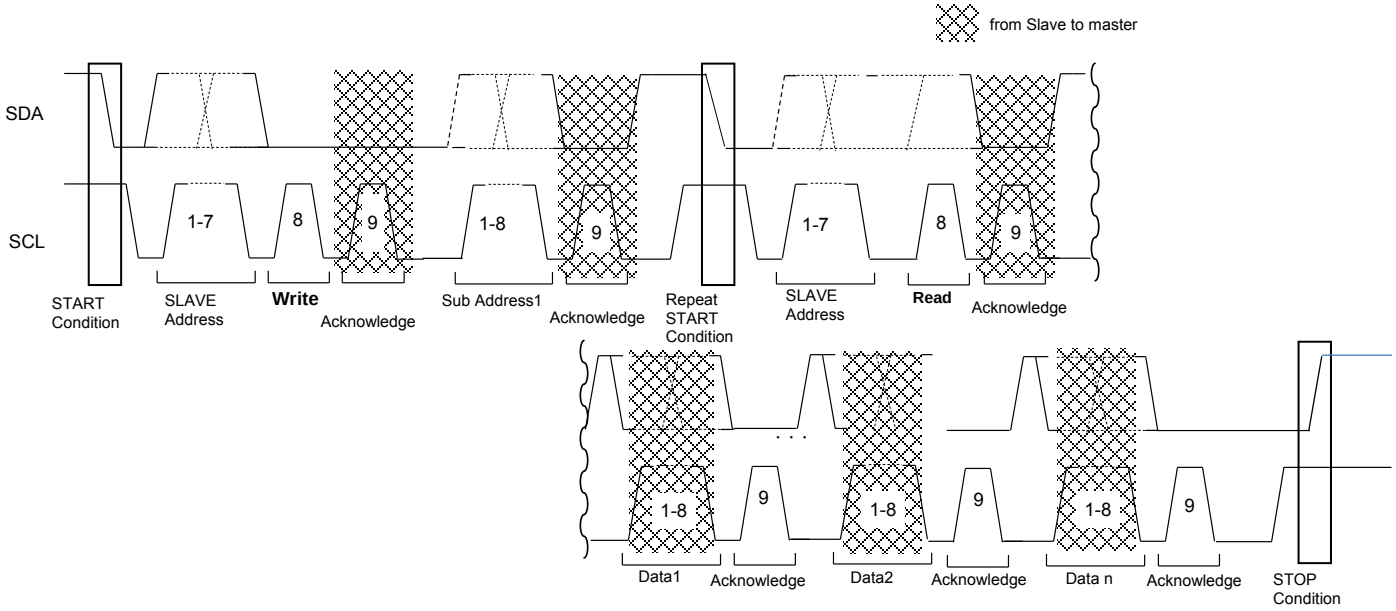
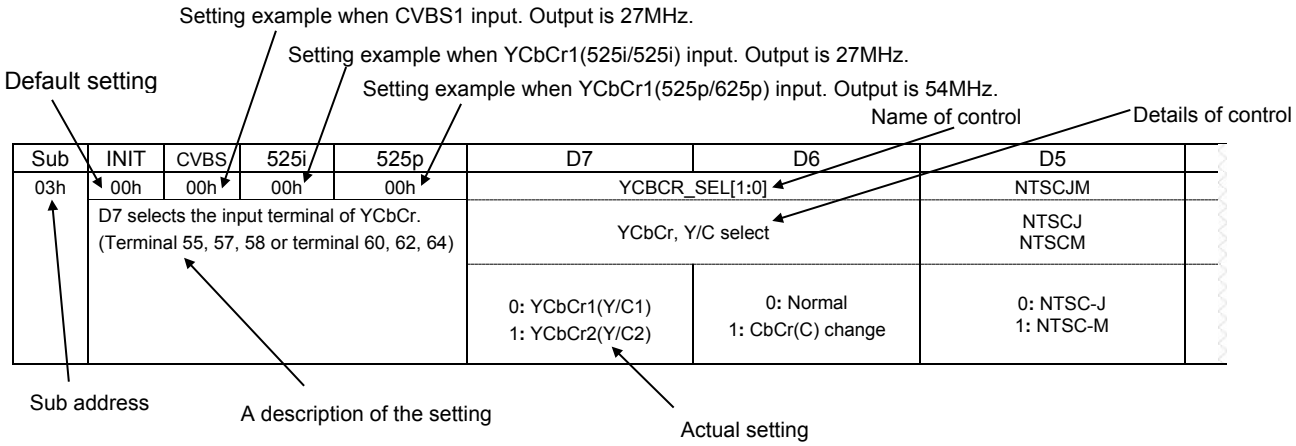


Figure 7-4 Bus control timing (Read mode)

(2) Points of view for register table

Introduction for register table and the bus set value for operating the TC90106FG.
Please refer to the example of setting, and try the settings for each register.



D4	D3	D2	D1	D0
VEC[1:0]				
V enhance coring				
00: OFF 01: 0.8IRE 10: 1.6IRE 11: 2.3IRE		–	–	–

Set the default value

Figure 7-5 How to use the register table

(3) Register table

(note) : Part of [–] set the initial value.

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
00h	24h	00h	00h	00h	MCDCKOFF	NOSIG_EN	OUTFIX[1:0]		OPINSEL	MUTE	Bank[1:0]	
	The D5 and D4 set to 00, IC becomes an output state.D2 set to 0. It is necessary to set Sub address:00h				Clock stop	DETSIG High-Z	Output Fixing		DATA MSB/LSB change	Video mute	Bank select	
					0: Active 1: Stop	0: High-Z 1: OUTPUT	00: OUTPUT 01: High-Z 10: L Fix 11: H Fix		0: Normal 1: swap	0: Normal 1: Mute ON	00: MCD (Multi Color Decoder) 01, 10, 11 : unusable	
01h	03h	03h	83h	83h	INSEL[1:0]		TVM3	TVM2	TVM1	TVM0	FSCAUTO[1:0]	
	It sets input format at D7 and D6.It selects CVBS or Y/C or YCbCr. D1 and D0 are for method of video system detection.				Input signal select		fsc	FV	PAL	SECAM	Video system detect mode select	
					00: CVBS (CVBS signal) 01: Y/C (Y/C signal) 10: YCbCr (Component signal) 11: unusable		0: 3.58MHz 1: 4.43MHz	0: 60Hz 1: 50Hz	0: Not PAL 1: PAL	0: Not SECAM 1: SECAM	00: Manual (00h-D5・・D2 enable) 01: Europe (Auto except 358-PAL) 10: South America (Detect except 443) 11: Full auto (All System)	
02h	02h	02h	02h	12h	YSWSEL[1:0]		PROGSEL[1:0]		DCOMBOFF	443NT	–	R656MODE
	D7 and D6 is the selection of the input terminal of CVBS (terminal 49, 51 and 53). When input the D2 of YCbCr, set the D4 to 1.				CVBS select		D1(525i/625i), D2(525p/625p) Setting		YC separation	443NT separation		Rec656 Version select
					00: CVBS1 01: CVBS2 10: CVBS3 11: unusable		00: D1 01: D2 1＊: unusable		0: 3Line separation 1: BPF separation	0: 2H comb 1: 4H comb		0: 656-3 1: 656-4 later
03h	00h	00h	00h	00h	YCBCR_SEL[1:0]		NTSCJM	VEC[1:0]				
	D7 is for selection of YCbCr input terminal . (terminal 55, 57, 58 or terminal 60, 62, 64)				Select the YCbCr or_Y/C		NTSCJ NTSCM	V Enhance coring		–	–	–
					0: YCbCr(Y/C)1 1: YCbCr(Y/C)2	0: Normal 1: CbCr(C) swap	0: NTSC-J 1: NTSC-M	00: OFF 01: 0.8IRE 10: 1.6IRE 11: 2.3IRE				
04h	00h	00h	00h	00h	GVENH[2:0]			VEN[1:0]		GNC[1:0]		PRENH
	D7 to D3, (03H_D4, D3) are for setting of the enhancer. Reference setting value is D8h				V Enhance gain			V Enhance turning point		Noise cancel gain		Pre Enhance
					000: OFF 001: Gain min to 111: Gain max			00: 6IRE 01: 9IRE 10: 13IRE 11: 16IRE		00: OFF 01: ×1/4 10: ×1/2 11: ×1		0: OFF 1: ON
05h	00h	00h	00h	00h	GHENH[4:0]					NCLIM[1:0]		FENH
	D7 to D3 are for setting of the sharpness. Reference setting value is 19h.				Sharpness gain					Noise cancel coring		Sharpness : fo
					00000: OFF⇒00001⇒01111: +gain 11111: -gain←10001←00000: OFF (D7: 0 is +gain, D7: 1 is -gain)					00: 0.8IRE 01: 1.6IRE 10: 3.2IRE 11: 6.4IRE		0: 3.3MHz 1: 4.2MHz
06h	08h	08h	08h	08h	GLTI[1:0]		LTILIM[1:0]		SET DELAY[3:0]			
	D7 to D4 are for setting of LTI. Reference setting value is 48h.				LTI gain		LTI coring level		Chrominance delay setting			
					00: OFF 01: ×1/8 10: ×1/4 11: ×1/2		00: 0.8IRE 01: 1.6IRE 10: 3.2IRE 11: 6.4IRE		0000: -296ns to 1000: Center to 1111: 259ns (37ns step)			
07h	00h	00h	00h	00h	GCTI[1:0]		CTILIM[1:0]		FLTI	FCTI	–	TRAPOFF
	D7 to D4 are for setting of CTI. Reference setting value is 80h.				CTI gain		CTI coring level		LTI fo	CTI fo		BSRCY 9MHz Trap OFF
					00: OFF 01: ×1/8 10: ×1/4 11: ×1/2		00: 0.4IRE 01: 0.8IRE 10: 1.6IRE 11: 3.2IRE		0: 3.3MHz 1: 2.2MHz	0: 1.7MHz 1: 3.4MHz		0: Trap ON 1: Trap OFF
08h	40h	40h	40h	40h	YCONT[7:0]							
	D7 to D0 are for setting of contrast.				Contrast control							
					00h: ×1/2 to 40h: ×1 to FFh: ×2.4							
09h	00h	00h	00h	00h	YBRIT[7:0]							
	D7 to D0 are for setting of brightness.				Brightness (Y output offset)							
					0000 0000: OFF to 0111 1111: +127LSB -127LSB: 1000 0000 to 1111 1111							
0Ah	00h	00h	00h	00h	RGAIN[3:0]				BGAIN[3:0]			
	D7 to D0 are for setting of Cb and Cr Gain.				Cr output gain				Cb output gain			
					1000: ×1/2 to 0000: ×1 to 0111: ×1.4				1000: ×1/2 to 0000: ×1 to 0111: ×1.4			
0Bh	00h	00h	00h	00h	ROFS[3:0]				BOFS[3:0]			
	D7 to D0 are for setting of Cb and Cr offset.				Cr output offset				Cb output offset			
					1000: -LSB to 0000: 0 to 0111: +LSB				1000: -LSB to 0000: 0 to 0111: +LSB			

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	00h	00h	00h	00h	HUE[6:0]							RDDLY
	D7 to D1 are for setting of HUE phase adjustment.				HUE phase adjustment							-
					1000000: -44.3° to 0000000: 0° to 0111111: +43.6°							0: Cb front 1: Cr Delay
0Dh	00h	00h	00h	00h	HUE BIAS[5:0]						MUTE	C MUTE
	D7 to D2 are for setting of HUE angle. D1and D0 are for setting of mute.				HUE angle						Video mute	Color mute
					000000: 0° to 111111: +45°						0: OFF 1: ON	0: OFF 1: ON
0Eh	08h	08h	08h	08h	3LOFF	CKILL[2:0]			ACC[3:0]			
	Usually, It uses INITIAL setting.				Color killer	Color killer level			ACC level			
					0: color killer on 1: color killer off	000: -40dB to 111: -30dB			0000: min to 1111: max			
0Fh	A0h	A0h	A0h	A0h	–	2BPFOFF	2BTR	OLDTR2	OLDTR3	TOFON[2:0]		
	Usually, It uses INITIAL setting.					2'ndBPF/TRAP	2'ndBPF/TRAP	TRAP1	TRAP2	Take off filter (Demodulation input bandwidth limit)		
						0: ON 1: OFF	0: Trap 1: BPF	0: OFF 1: ON	0: OFF 1: ON	000: OFF 001: BPF ON 010: Min to 111: Max		

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
10h	82h	82h	82h	82h	–	–	STCLMP[1:0]		FBCLP_ON[1:0]		–	–
	D5 to D2 are for setting of clamp function. Usually, It uses INITIAL setting.						Sync tip clamp for ADC		FB clamp ON/OFF control			
							00: AUTO 01: Forcing ON 1*: Forcing OFF		00: Auto 01: Forcing ON 1*: Forcing OFF			
11h	13h	13h	12h	12h	YCLPON	FSCTRAP	–		–	—	–	CADFILON
	These are for setting of digital clamp.				Y digital clamp	fsc trap ON for clamp						C input LPF
					0: OFF 1: ON	0: OFF 1: ON						0: OFF 1: ON
12h	00h	00h	00h	00h	–		–		–		–	
	Fixed to initial value.											
13h	D6h	D6h	D6h	D6h	–		–	–	NCOEV	CGAIN[2:0]		
	Usually, It uses INITIAL setting.								SECAM De-Emphasis	Y trap performance set up for SECAM		
									0: Normal 1: UP	000: ×0 to 111: ×0.4375 [110]		
14h	00h	00h	00h	00h	–	–	–	–	–	–	FILON[1:0]	
	Fixed to initial value.										Decoder output IIR filter	
											00: OFF 01: Wide band 10: Narrow band 11: Low PASS	
15h	00h	00h	00h	00h	–	–	VSRACH[1:0]		–	WIDEGATE	–	–
	Usually, It uses INITIAL setting.						fsc lock period			443 detection gate width select		
							00: 3V 01: 4V 10: 5V 11: 6V			0: Narrow 1: Wide		
16h	00h	00h	00h	00h	BFD2	FSCWIDE	DIZY	OUTPEAK	–	RBCHG	–	–
	Usually, It uses INITIAL setting.				BGP search for DET443	fsc lead-in expand	Dither correction	Out peak limit		Cb/Cr swap		
					0: OFF 1: ON	0: Normal 1: Wide	0: OFF 1: ON	0: OFF 1: ON		0: Normal 1: change		

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
17h	10h	10h	10h	10h	GCLPWIDTH[2:0]			SELGCLP	GCLPDLY[3:0]			
	Usually, It uses INITIAL setting.				Y clamp pulse width setup			Y clamp position	Y clamp pulse position setup			
					100: 1.78μs to 000: 2.37μs to 011: 2.81μs (D1: 6.75MHz D2: 13.5MHz step)			0: Sync Tip 1: Pedestal	1000: -1.18μs to 0000: ±0μs to 0111: +1.03μs (D1: 6.75MHz D2: 13.5MHz step)			
18h	10h	10h	10h	10h	RBCLPWIDTH[2:0]			SELRBCLP	RBCLPDLY[3:0]			
	Usually, It uses INITIAL setting.				Cr/Cb clamp pulse width setup			Cr/Cb clamp position	Cr/Cb clamp position setup			
					100: 1.78μs to 000: 2.37μs to 011: 2.81μs (D1: 6.75MHz D2: 13.5MHz step)			0: Sync Tip 1: Pedestal	1000: -1.18μs to 0000: ±0μs to 0111: +1.03μs (D1: 6.75MHz D2: 13.5MHz step)			
19h	3Bh	3Bh	3Bh	38h	–				–		HGAIN[1:0]	
	D1, D0 are for AFC gain. It needs to select regarding input signal.										AFC gain selection	
											00: Input signal is 525p format. 11: Input signal is CVBS or 525i format. 01 or 10: Unusable	
1Ah	87h	87h	87h	87h	–				–			
	Fixed to initial value.											
1Bh	25h	25h	25h	25h	–				–	–		
	Fixed to initial value.											
1Ch	1Fh	1Fh	1Fh	1Fh	–		–	–	–		–	
	Fixed to initial value.											
1Dh	00h	00h	00h	00h	SHCTRL[5:0]						SLSEL	–
	Usually, It uses INITIAL setting.				Horizontal reference phase adjustment						H separation level	
					100000: -4.74μs to 000000: ±0μs to 011111: +4.59μs (1/6.75MHz step)						0: 30% 1: 40%	
1Eh	00h	00h	00h	00h	VHPH[2:0]			–	–	–	VDSEL[1:0]	
	Usually, It uses INITIAL setting.				Vertical reference phase adjustment						VD output control	
					011: +3H to 000: center(typ.) to 100: -4H						00: Always synchronize input 01: keep DET50 frequency just before NOSIG 1*: TVM2 at FSCAUTO=00	
1Fh	81h	81h	81h	81h	–			–	–	–	FIELDET	–
	Usually, It uses INITIAL setting.										Field Identification for Nonstandard Signal	
											0: ODD/EVEN output reverse (every 1V) 1: Low	

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
20h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
21h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
22h	00h	00h	00h	00h	–		–		–		–	
	Fixed to initial value.											
23h	00h	00h	00h	00h	–		–		–		–	
	Fixed to initial value.											

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
24h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
25h	00h	00h	00h	00h	–	HV601 656VD Pulse Output switching 0: 656 VD 1: 601 VD	–	–	–	–	–	
	Usually, It uses INITIAL setting.											
26h	00h	00h	00h	00h	–	NOSIG_MODE[1:0] Detect condition 0:H detection (V latch) 1:H detection (No V latch)	 0: H detection only 1: H, V, fscLOCK detection	NOSIG_O DETSIG polarity 0:High when there is signal 1:Low when there is signal	NOSIG_VE[1:0] End V 00: same time NOSIG 01: after 3V 10: after 5V 11: after 7V		NOSIG_VS[1:0] Start V 00: same time NOSIG 01: after 3V 10: after 5V 11: after 7V	
	Usually, It uses INITIAL setting.											
27h	00h	00h	00h	00h	HDPH[3:0] Horizontal phase adjustment for digital output signal 1000: -1.185µs to 0000: 0µs to 1111: +1.04µs				VDPH[3:0] Vertical phase adjustment for digital output signal 0000: 0H to 1111: +15H			
	Usually, It uses INITIAL setting.											
28h	10h	10h	10h	10h	–			–	–		–	
	Fixed to initial value.											
29h	00h	00h	00h	00h	PHPOLE HD polarity select 0: Positive 1: Negative	PVPOLE VD polarity select 0: Positive 1: Negative	PFPOLE Field polarity 0: Positive 1: Negative	THRHV H,V-OUT select 0: ITU-R BT.656 mode 1: through	SEL_BLK Setup BLK Process 0: forced 1: through	–	CLP Pedestal clip 0: OFF 1: ON	INVCK Clock polarity 0: Positive 1: Negative
	D7, D6, D5, D0 are for polarity switching of VD, HD, Field, CLOCK.											
2Ah	00h	00h	00h	00h	EN_PIXH_S[3:0] Fine tune horizontal start phase of picture processing 1000: -1.185µs to 0000: ±0µs to 0111: +1.04µs				EN_PIXH_W[3:0] Fine tune horizontal picture processing period 1000: -1.185µs to 0000: ±0µs to 0111: +1.04µs			
	Usually, It uses INITIAL setting.											
2Bh	00h	00h	00h	00h	–	–	–	–	–	–		
	Fixed to initial value.											
2Ch	00h	00h	00h	00h	–				–			
	Fixed to initial value.											
2Dh	20h	20h	20h	20h	–				–	–	–	–
	Fixed to initial value.											
2Eh	00h	00h	00h	00h	–				–			
	Fixed to initial value.											
2Fh	00h	00h	00h	00h	–				–			
	Fixed to initial value.											

Sub	INIT	CVBS	525i	525p	D7	D6	D5	D4	D3	D2	D1	D0
30h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
31h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
32h	00h	00h	00h	00h	BBACK_MODE[1:0]		BBACKVE[1:0]		BBACKVS[1:0]		BBACK_AUTO	BBACK
	When there is no signal, it outputs a specified blue back (blue image) .				Blue Back switching condition		Blue Back END V		Blue Back start V		Forcing B_BACK ON/OFF	Change to Blue Back when no signal
					0: H detection (V latch) 1: H detection (No V latch)	0: H detection only 1: H, V, fscLOCK detection	00: same time NOSIG 01: after 3V 10: after 5V 11: after 7V (When 32h D6=1, it sets to 00)		00:same time NOSIG 01: after 3V 10: after 5V 11: after 7V		0: OFF(Normal) 1: ON(Forced)	0: OFF 1: ON
33h	00h	00h	00h	00h	BBACKY[7:0]							
	It sets the blue back data of the function 32h.				Blue Back Y							
					00h(16h): Black to FFh: white							
34h	00h	00h	00h	00h	BBACKCB[7:0]							
	It sets the blue back data of the function 32h.				Blue Back Cb							
					00h to 80h: center to FFh							
35h	00h	00h	00h	00h	BBACKCR[7:0]							
	It sets the blue back data of the function 32h.				Blue Back Cr							
					00h to 80h:center to FFh							
36h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
37h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
38h	F0h	F0h	F0h	F0h	ADPWD10	ADPWD8	ADPWS10	ADPWS8	–	–	–	–
	When CVBS inputs, it can save the current using 8bit ADC OFF function.				10bit ADC Power down	8bit ADC Power down	10bit ADC Power save	8bit ADC Power save				
					0: Power down 1: Normal	0: Power down 1: Normal	0: Power save 1: Normal	0: Power save 1: Normal				
39h	00h	00h	00h	00h	–	–	–	–	–	–	–	–
3Ah	00h	00h	00h	00h	–	–	–	–	–	–	–	–
3Bh	00h	00h	00h	00h	–	–	–	–	–	–	–	–
3Ch	00h	00h	00h	00h	–	–	–	–	–	–	–	–
3Dh	00h	00h	00h	00h	–	–	–	–	–	–	–	–
3Eh	00h	00h	00h	00h	BKOFST[7:0]							
	It controls NTSC-M.				NTSC-M offset control							
					80h: -128LSB to 7Fh: +127LSB (8bit) recommendation is 11110101							
3Fh	00h	00h	00h	00h	BKLVL[7:0]							
	It controls NTSC-M.				NTSC-M gain control							
					00h: ×1/2 to 40h: ×1 to FFh: ×2.4							

For read data

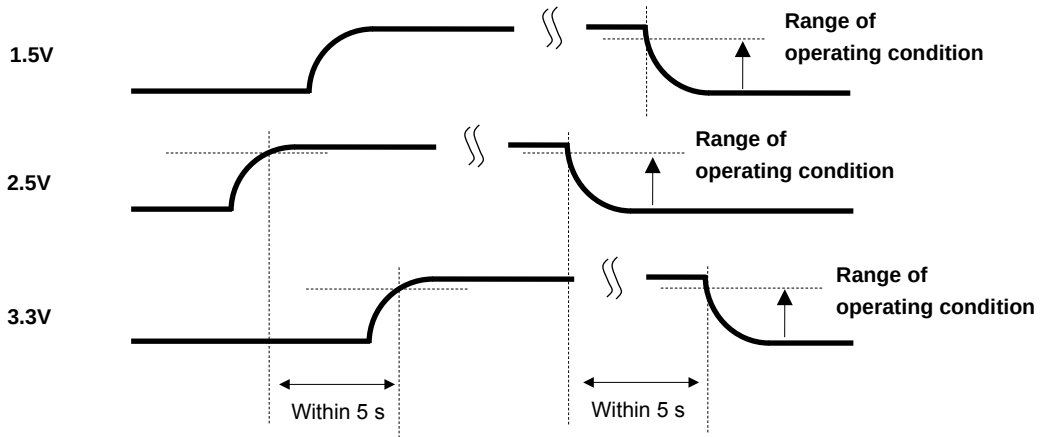
Sub		D7	D6	D5	D4	D3	D2	D1	D0
50h	Detected data for the input signal.	DET50	NOSIG	NOVP	FIELD	HLOCK	H/VSTD	Fixed to 0	NOSIGD2
		Field frequency	No-signal detection	V-Sync detection	Field detection	H LOCK	H-V standard		D2 judge
		0: 60Hz 1: 50Hz	0: signal 1: No signal	0: V detection 1: No V	0: ODD 1: EVEN	0: UNLOCK 1: LOCK	0: standard 1: Not standard		0: not D2 1: D2
51h	Detected data for the input signal.	DET443	PAL	SECAM	FSC_SEL[1:0]		CKILL	FSCSTD_N	FSCLOCK
		4.43MHz detection	Internal PAL operation	Internal SECAM operation	fsc detection		Killer detection	fsc standard	fsc lock detection
		0: No detection 1: detection	0: except PAL 1: PAL	0: except SECAM 1: SECAM	00: 3.579545MHz 01: 3.575611MHz 10: 3.582056MHz 11: 4.433MHz		0: killer off Color exists 1: killer on No color	0: standard 1: No standard	0: unlock 1: lock
52h	Detected data for the input signal.	NOISE_OUT[7:0]							
		S/N detection							
		0000_0000:S/N good → 1111_1111:S/N weak							
53h	Detected data for the input signal.	QVCD[7:0]							
		H counter number for 1V period							
		0000_0000 or 0000_0001:standard							
54h	Detected data for the input signal.	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	PALDET	SECAMDET
								PAL detection	SECAM detection
								0:No detection 1:detection	0:No detection 1:detection

Table 7-6 Register table

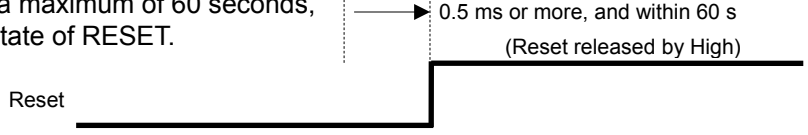
8. Control sequence for Power ON and OFF

This section is critical to the reliability assurance of the IC.
Read it carefully before setting power-on/off control,
reset control and I^2C-BUS control timing settings accordingly.
The signal input is not recommended in a state in which the power is not applied.

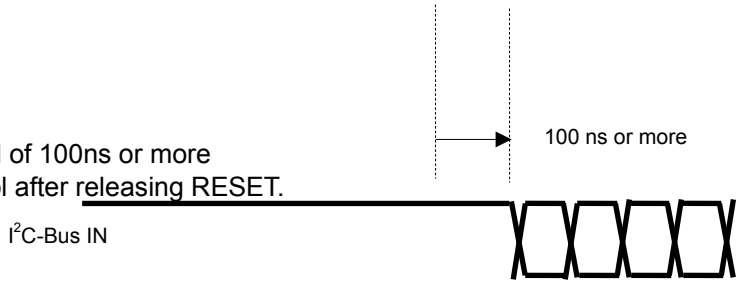
●Power ON/OFF
The power of this IC is three. It is 1.5V and 2.5V and 3.3V.
The order of power-on and power-off of 3-system VDD (1.5V, 2.5V, 3.3V) is good with random order.
However, please complete power-on and power-off of 3-system VDD within 5 second.



●Reset
It hold the RESET state at least 0.5ms or more after all 3 power systems have reached the operation power voltage.
State of RESET is a maximum of 60 seconds, and not leave the state of RESET.



●I^2C-Bus
It needs the period of 100ns or more for I^2C-BUS control after releasing RESET.



9. Revision History

Date	Revision	Contents
2016/03/24	1.0	First edition
2016/06/30	2.0	2nd edition
2017/04/05	2.1	Page 1 : Application circuit example Replacement figure of application circuit Page 2 : Terminal function (3) I^2C terminal In 5th line, change to “When terminal voltage is 3.3V, slave address is B2. When terminal voltage is GND, it is B0.” Page 3 : Terminal function (8) Input signal In 7th line, correction from NTSCLM to NTSCJM Page 11 : Sub address 00h D1 and D0 in Register table. Change to “unusable” when Bank select setting value is 11. Page 11 : Sub address 01h CVBS recommendation value in Register table. Correction from 00h to 03h. Page 13 : Sub address 19h D1 and D0 in Register table. Addition to a part of HGAIN AFC gain selection. Page 13 : Default setting value of sub address 1Bh in Register table. Correction from 00h to 25h. (4 places) Page 15 : Sub address 50h, 51h, 52h, 53h, 54h in Register table. Deletion of INIT item Page 15 : Sub address 50h, 54h in Register table. Change to “Fix to 0” for part of (-) Page 11 to 15 : Register table It colors part of initial value in tables. Full page : Reconsidering expressive style of English sentences.

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