

MOSFETs Silicon N-channel MOS (U-MOS<sup>Ⅷ</sup>-H)

# SSM3K341R

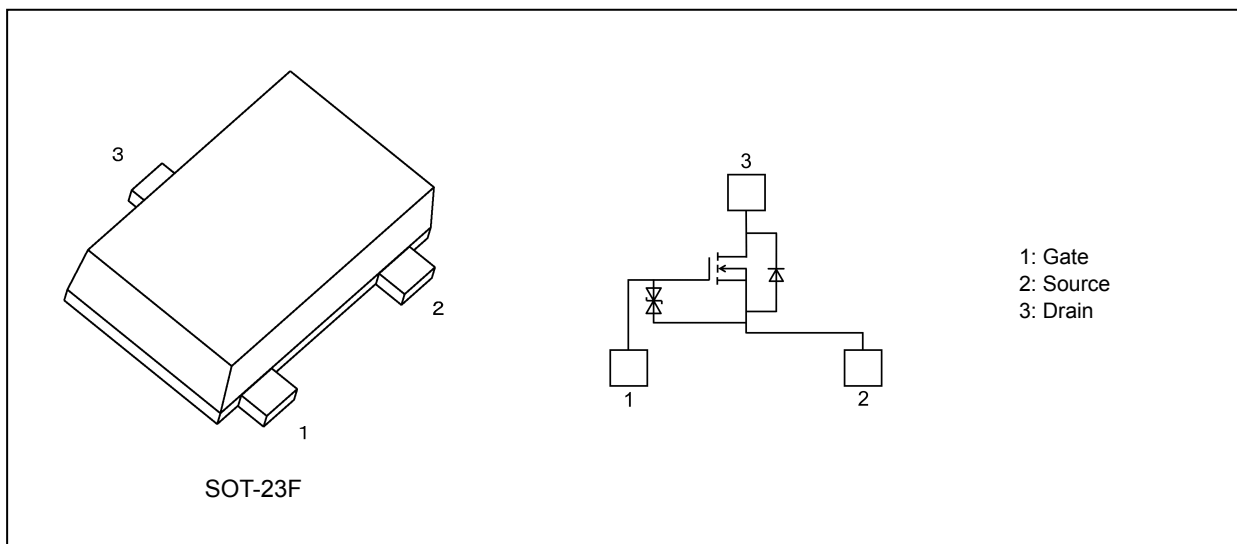
### 1. Applications

- Power Management Switches
- DC-DC Converters

### 2. Features

- (1) AEC-Q101 qualified (Please see the orderable part number list)
- (2) 175 °C MOSFET
- (3) 4.0 V drive
- (4) Low drain-source on-resistance  
 :  $R_{DS(ON)} = 28 \text{ m}\Omega$  (typ.) (@ $V_{GS} = 10 \text{ V}$ )  
 $R_{DS(ON)} = 36 \text{ m}\Omega$  (typ.) (@ $V_{GS} = 4.5 \text{ V}$ )  
 $R_{DS(ON)} = 43 \text{ m}\Omega$  (typ.) (@ $V_{GS} = 4 \text{ V}$ )

### 3. Packaging and Pin Assignment



### 4. Orderable part number

| Orderable part number | AEC-Q101     | Note                    |
|-----------------------|--------------|-------------------------|
| SSM3K341R,LF          | —            | General Use             |
| SSM3K341R,LXGF        | YES (Note 1) | Unintended Use (Note 1) |
| SSM3K341R,LXHF        | YES          | Automotive Use          |

Note 1: For more information, please contact our sales or use the inquiry form on our website.

Start of commercial production  
2016-01

### 5. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

| Characteristics                                     | Symbol    | Rating     | Unit             |
|---|-----------|------------|------------------|
| Drain-source voltage                                | $V_{DSS}$ | 60         | V                |
| Gate-source voltage                                 | $V_{GSS}$ | $\pm 20$   |                  |
| Drain current (DC) (Note 1)                         | $I_D$     | 6          | A                |
| Drain current (pulsed) (Note 1), (Note 2)           | $I_{DP}$  | 24         |                  |
| Power dissipation (Note 3)                          | $P_D$     | 1.2        | W                |
| Power dissipation ( $t \leq 10\text{ s}$ ) (Note 3) | $P_D$     | 2.4        |                  |
| Single-pulse avalanche energy (Note 4)              | $E_{AS}$  | 28.9       | mJ               |
| Single-pulse avalanche current (Note 4)             | $I_{AS}$  | 6          | A                |
| Channel temperature (Note 5)                        | $T_{ch}$  | 175        | $^\circ\text{C}$ |
| Storage temperature (Note 5)                        | $T_{stg}$ | -55 to 175 |                  |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 2: pulse width  $\leq 1\text{ ms}$ , Duty  $\leq 1\%$

Note 3: Device mounted on an FR4 board.(25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu pad: 645 mm<sup>2</sup>)

Note 4:  $V_{DD} = 25\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (Initial state),  $L = 1\text{ mH}$ ,  $R_G = 25\ \Omega$

Note 5: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 6. Thermal Characteristics

| Characteristics                                | Symbol         | Max | Unit                      |
|--|----------------|-----|---------------------------|
| Channel-to-ambient thermal resistance (Note 1) | $R_{th(ch-a)}$ | 125 | $^\circ\text{C}/\text{W}$ |

Note 1: Device mounted on an FR4 board.(25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu pad: 645 mm<sup>2</sup>)

### 7. Electrical Characteristics

#### 7.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

| Characteristics                         | Symbol        | Test Condition                              | Min | Typ. | Max      | Unit             |
|---|---------------|---|-----|------|----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 16\text{ V}$                  | —   | —    | $\pm 10$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 60\text{ V}$                      | —   | —    | 1        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$   | 60  | —    | —        | V                |
| Drain-source breakdown voltage (Note 1) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$ | 40  | —    | —        |                  |
| Gate threshold voltage (Note 2)         | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$ | 1.5 | —    | 2.5      |                  |
| Drain-source on-resistance (Note 3)     | $R_{DS(ON)}$  | $I_D = 2\text{ A}, V_{GS} = 4\text{ V}$     | —   | 43   | 69       | $\text{m}\Omega$ |
|   |               | $I_D = 3\text{ A}, V_{GS} = 4.5\text{ V}$   | —   | 36   | 51       |                  |
|   |               | $I_D = 5\text{ A}, V_{GS} = 10\text{ V}$    | —   | 28   | 36       |                  |

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (0.1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 7.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

| Characteristics                | Symbol    | Test Condition   | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|--|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1\text{ MHz}$   | —   | 550  | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |  | —   | 35   | —   |             |
| Output capacitance             | $C_{oss}$ |  | —   | 300  | —   |             |
| Switching time (rise time)     | $t_r$     | $V_{DD} = 30\text{ V}, I_D = 3\text{ A},$<br>$V_{GS} = 0\text{ to }4.5\text{ V}, R_{GS} = 50\ \Omega$<br>Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ ,<br>Common source,<br>See Chapter 7.3. | —   | 48   | —   | $\text{ns}$ |
| Switching time (turn-on time)  | $t_{on}$  |  | —   | 63   | —   |             |
| Switching time (fall time)     | $t_f$     |  | —   | 6    | —   |             |
| Switching time (turn-off time) | $t_{off}$ |  | —   | 18   | —   |             |

#### 7.3. Switching Time Test Circuit

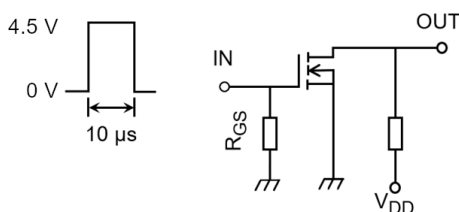


Fig. 7.3.1 Switching Time Test Circuit

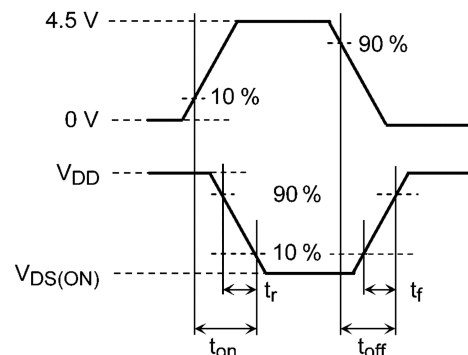


Fig. 7.3.2 Input Waveform/Output Waveform

#### 7.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

| Characteristics                                 | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|---|-----------|---|-----|------|-----|-------------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} = 48\text{ V}, I_D = 2\text{ A},$<br>$V_{GS} = 10\text{ V}$ | —   | 9.3  | —   | $\text{nC}$ |
| Gate-source charge 1                            | $Q_{gs1}$ |   | —   | 1.8  | —   |             |
| Gate-drain charge                               | $Q_{gd}$  |   | —   | 2.0  | —   |             |

## 7.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

| Characteristics                | Symbol    | Test Condition                                | Min | Typ. | Max | Unit |
|--------------------------------|-----------|---|-----|------|-----|------|
| Diode forward voltage (Note 1) | $V_{DSF}$ | $I_{DR} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$ | —   | 0.9  | 1.5 | V    |

Note 1: Pulse measurement.

## 8. Marking

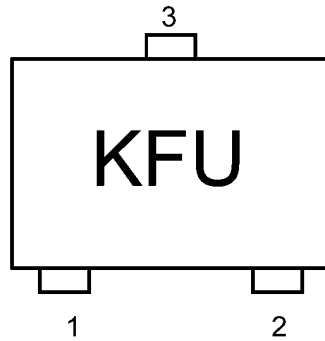
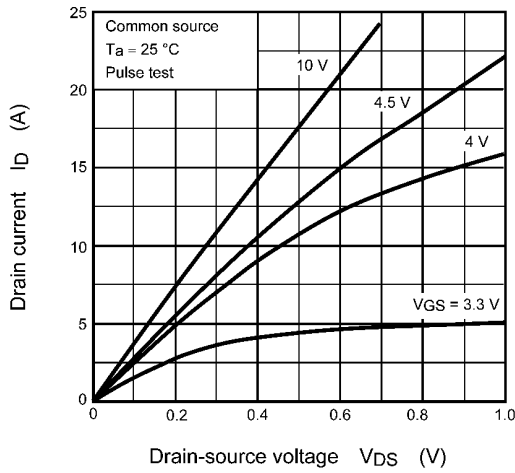
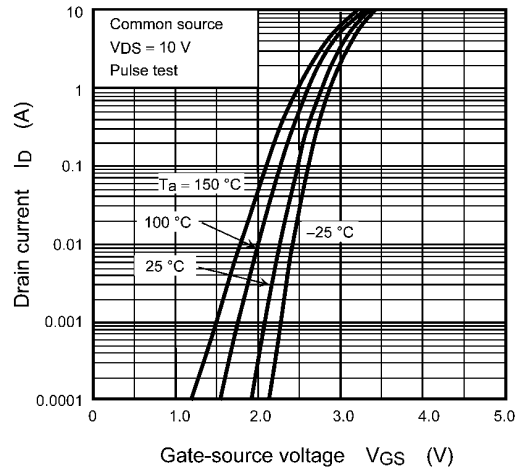


Fig. 8.1 Marking

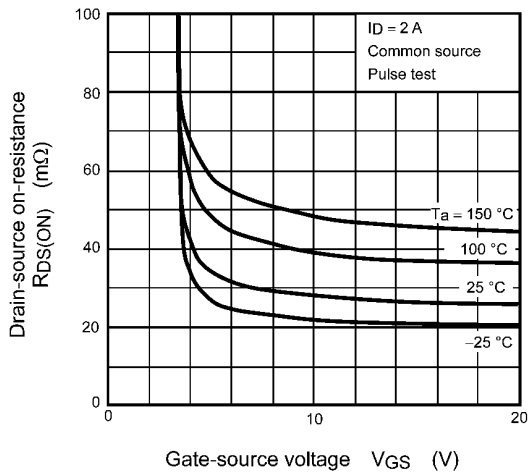
### 9. Characteristics Curves (Note)



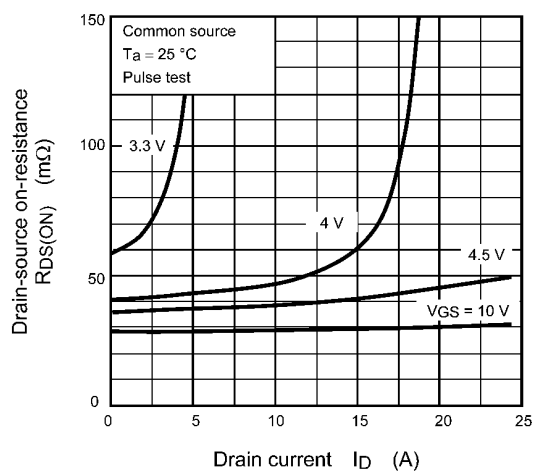
**Fig. 9.1  $I_D - V_{DS}$**



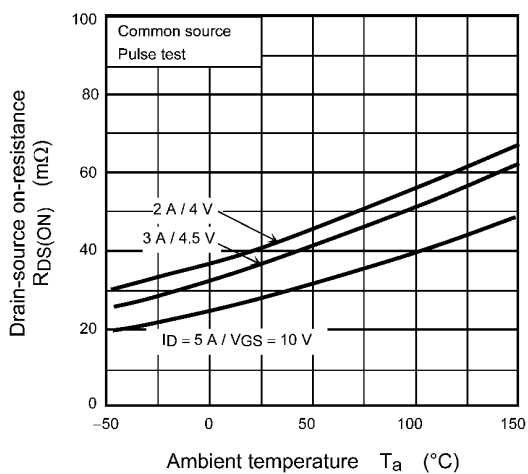
**Fig. 9.2  $I_D - V_{GS}$**



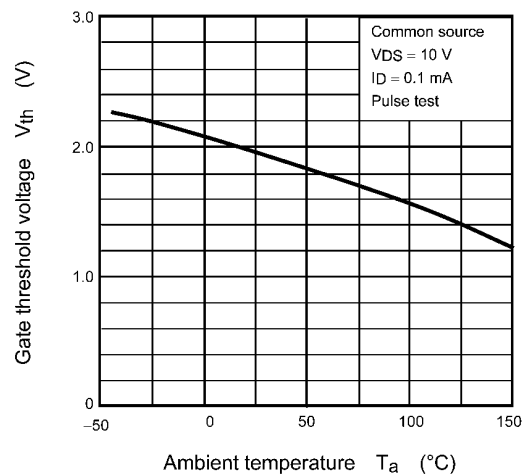
**Fig. 9.3  $R_{DS(ON)} - V_{GS}$**



**Fig. 9.4  $R_{DS(ON)} - I_D$**



**Fig. 9.5  $R_{DS(ON)} - T_a$**



**Fig. 9.6  $V_{th} - T_a$**

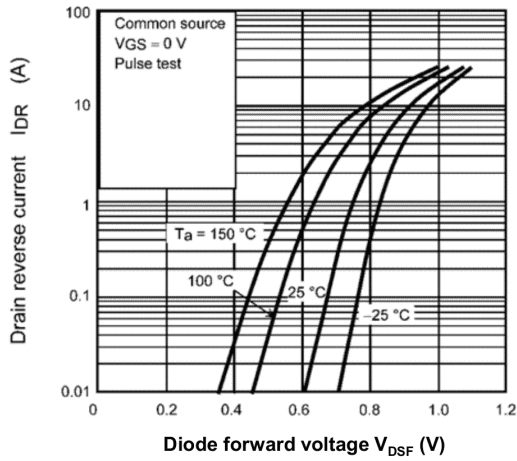


Fig. 9.7  $I_{DR} - V_{DSF}$

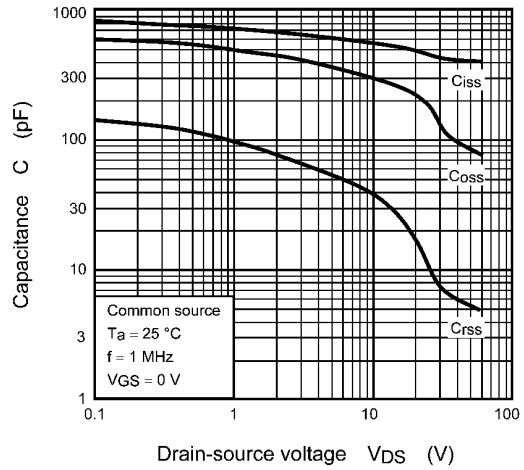


Fig. 9.8  $C - V_{DS}$

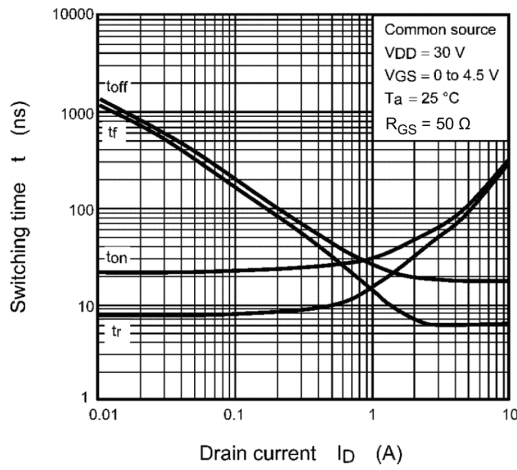


Fig. 9.9  $t - I_D$

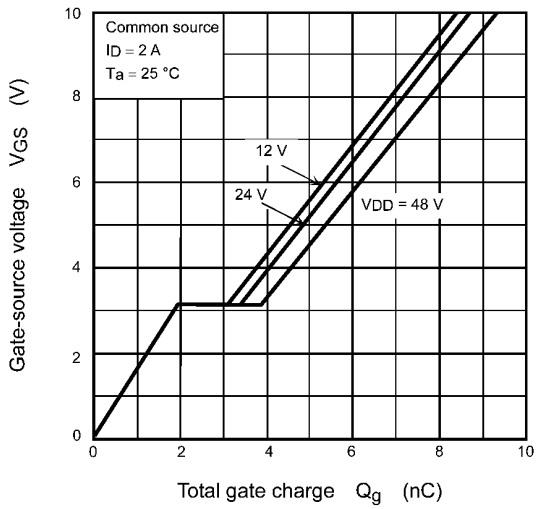


Fig. 9.10 Dynamic Input Characteristics

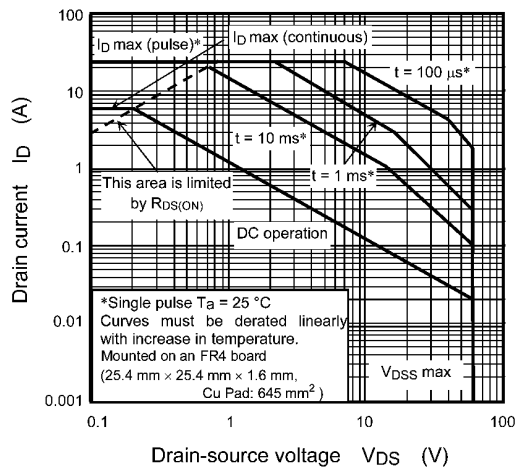


Fig. 9.11 Safe Operating Area

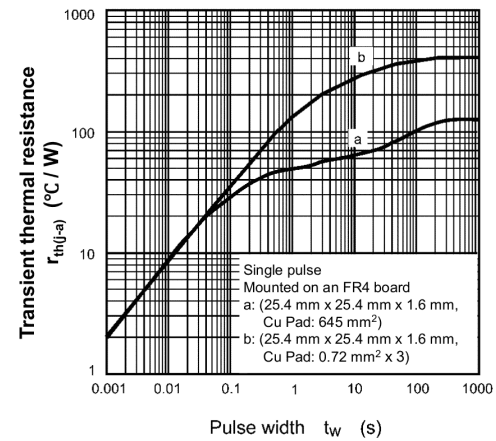


Fig. 9.12  $r_{th(j-a)} - t_w$

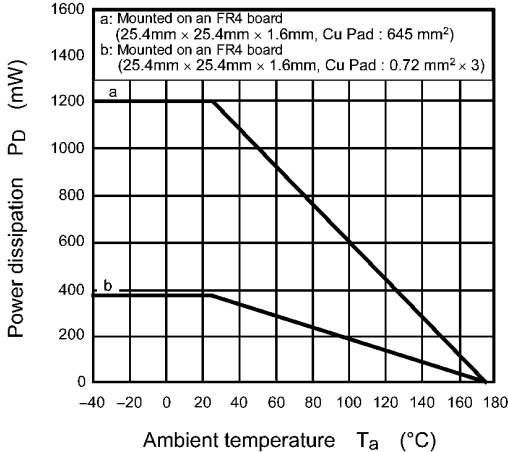


Fig. 9.13  $P_D - T_a$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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