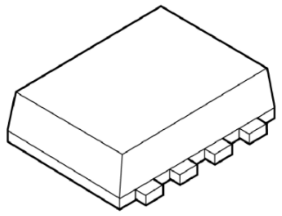
TOSHIBA Intelligent Power Device Silicon Monolithic MOS Integrated Circuit

TPD7104AF

1 channel High-Side N channel MOSFET Gate Driver

1. Description

TPD7104AF is a 1channel high-side N channel MOSFET gate driver. This IC contains a charge pump circuit, allowing easy configuration of a high-side switch for large-current applications.



weight: 0.017g (typ.)

2. Applications

- Junction Boxes for Automotive.
- Power distribution modules for Automotive.
- Semiconductor relays.

3. Features

- Charge pump circuit is built in.
- Built-in short circuit (overcurrent detection) and reverse battery protection.
- AEC-Q100 qualified.
- The package is a small surface mount type PS-8, and the packaging is embossed tape.

Note: Due to its MOS structure. This product is sensitive to static electricity.

Start of commercial production
2015-08

4. Block Diagram

4.1. Application example of load switch circuit (reverse power connection protection not supported)

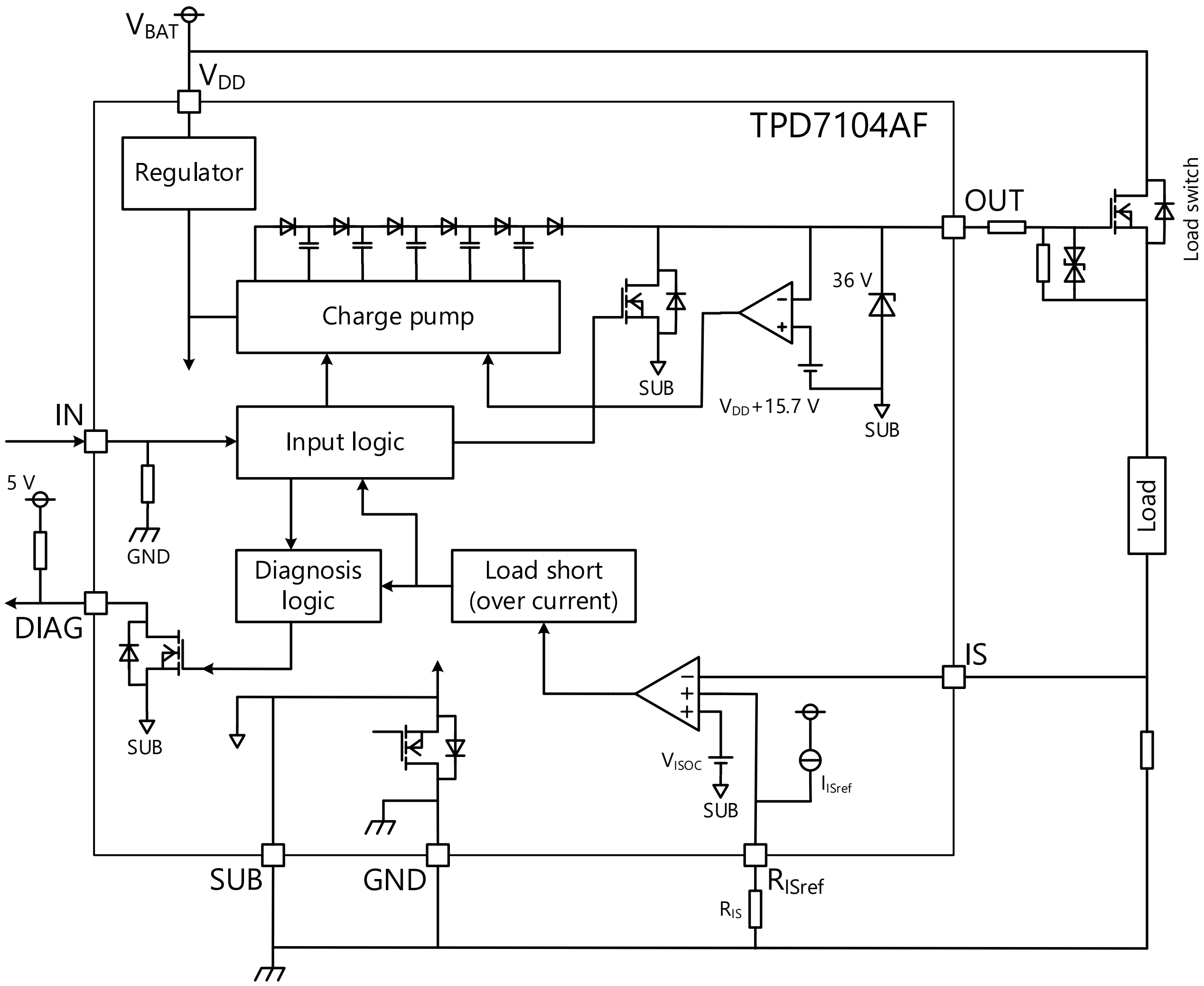


Figure 4.1 Block diagram (application example of load switch circuit)

4.2. Application example of power supply reverse connection protection circuit (keeps external FET off when power supply is reversely connected)

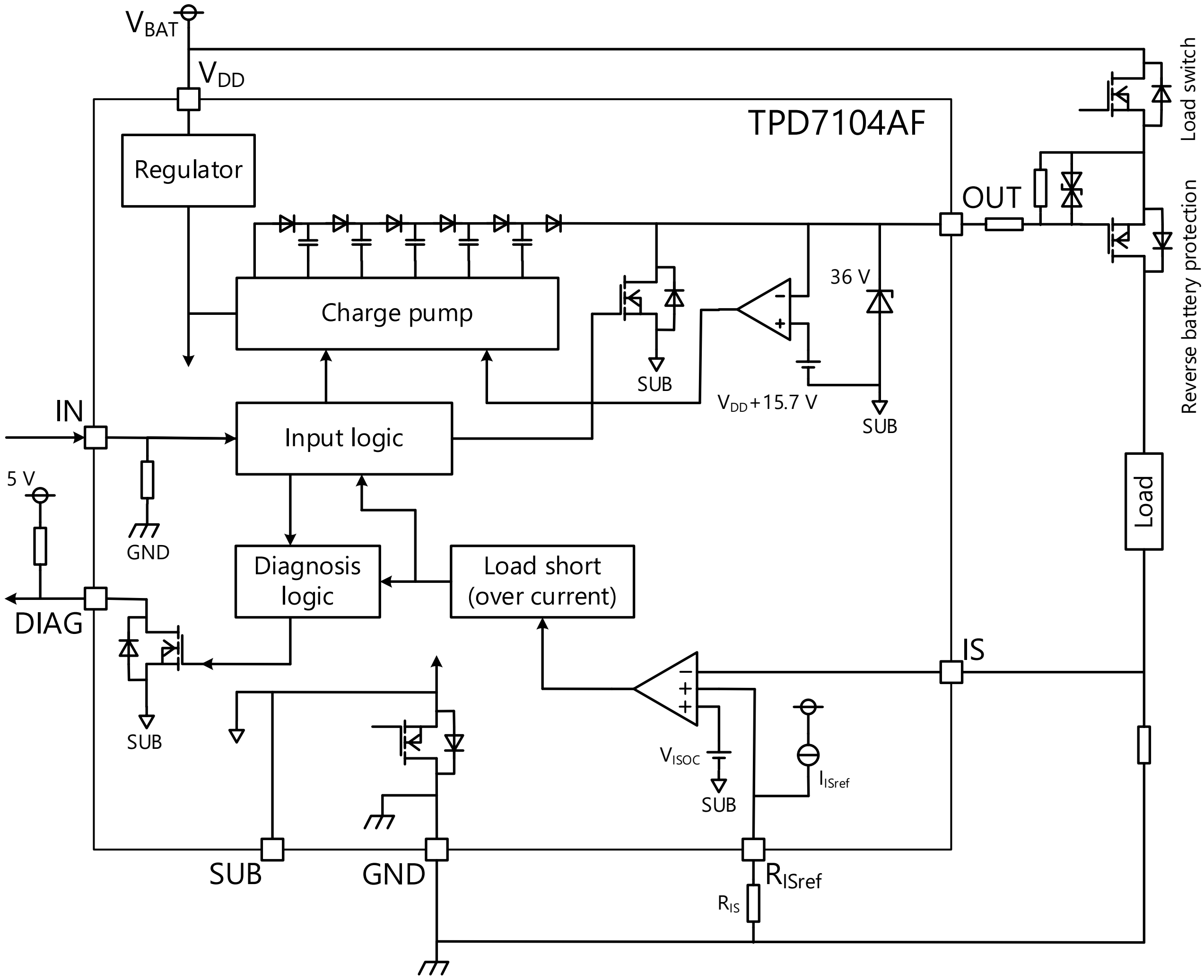


Figure 4.2 Block Diagram (application example of power supply reverse connection protection circuit)

5. Pin Assignments

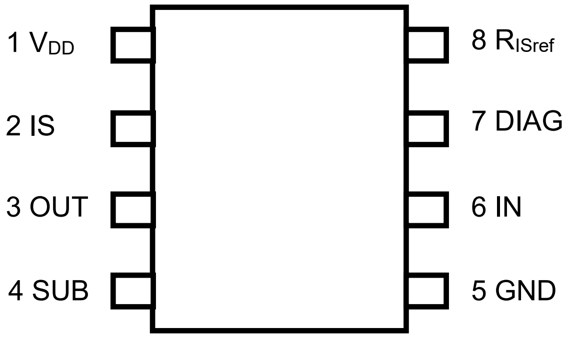


Figure 5.1 Pin Assignments (top view)

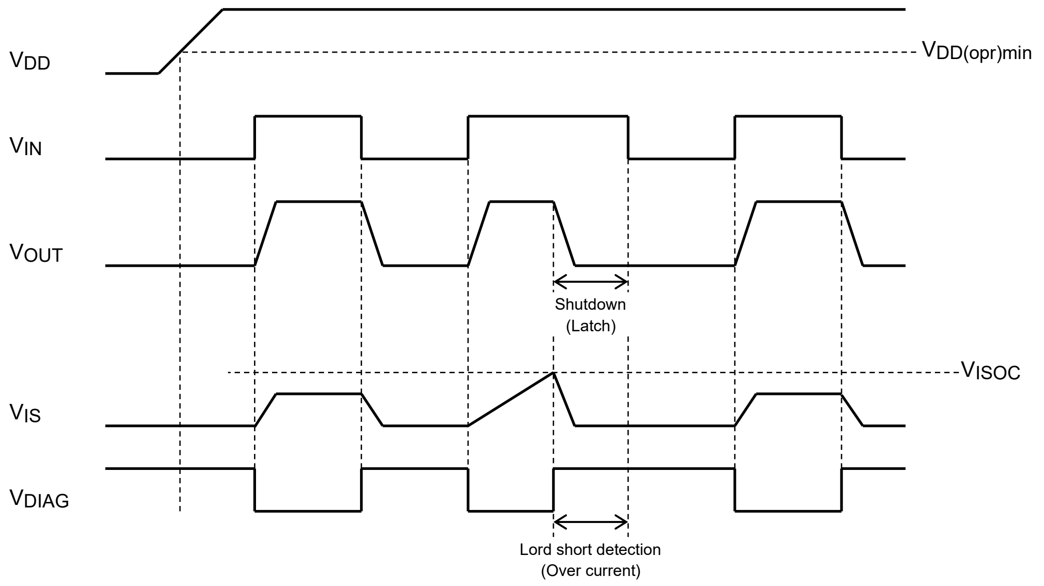
6. Pin Description

Table 6.1 Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD}	—	Power supply pin.
2	IS	IN	Detection pin for short circuit. If short circuit detection is not used, IS pin connect to GND.
3	OUT	OUT	Output pin for an external MOSFET drive. State is off (V_{OUT}="L") if detect short circuit.
4	SUB	—	Please use open if use protection for reverse connection of power supply. When not using the power supply reverse connection protection function, short the SUB terminal to GND (ground).
5	GND	—	Ground pin.
6	IN	IN	Input pin. IN has a pull-down resistor.
7	DIAG	OUT	Diagnosis detection pin. It is open drain composition. When a load short circuit is detected, V_{DIAG}="H" is output.
8	R_{ISref}	OUT	Adjust pin for sense level for short circuit detection. If you do not want to change the load short circuit detection level from V_{ISOC}=1.02V (typ.), leave R_{ISref} pin open.

7. Functional Description

7.1. Timing chart



Note: Output shut down when it detects short circuit and becomes latch state and protects outside MOSFET.
DIAG becomes H-state, and makes input L-state when reset the latch circuit.

Figure 7.1 Timing chart

7.2. Truth table

Table 7.1 Truth table

V_{IN}	V_{OUT}	Charge pump	V_{IS} (Note 1)	V_{DIAG}	Mode
L	L	Charge pump stop (oscillation is stopped)	L	H (Note 2)	Normal
H	H	Charge pump operation.	L	L	
L	L	Charge pump stop (oscillation is stopped)	H	H (Note 2)	Load short
H	L	Charge pump stop (oscillation is stopped)	H	H (Note 2)	
-	Hz (Note 3)	-	-	Hz (Note 3)	Reverse battery (SUB pin open)

Note 1: V_{IS} : Load short detection voltage.
Note 2: The DIAG output is a N channel open-drain and it is OFF state at the time of V_{DIAG} = “H”.
Note 3: Hz : High impedance.

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings (Note)

(T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit	Remarks
Power supply voltage	DC	$V_{DD(1)}$	-0.3 to 24.0	V	-
	Pulse	$V_{DD(2)}$	40.0	V	t=300ms single pulse
Power supply reverse connection		$-V_{DD(3)}$	18.0	V	SUB open
Input voltage		V_{IN}	-0.3 to 6.0	V	-
Output source current		$I_{OUT(-)}$	Internal capacity	mA	Source current
Output sink current		$I_{OUT(+)}$	5	mA	Sink current
IS pin voltage		V_{IS}	-0.3 to 6.0	V	-
Diagnosis output voltage		V_{DIAG}	-0.3 to 6.0	V	-
Diagnosis pin current		I_{DIAG}	5	mA	-
Power dissipation		$P_{D(1)}$	0.70	W	Refer to Figure 9.1
Power dissipation		$P_{D(2)}$	0.35	W	Refer to Figure 9.2
Operating temperature		T_{opr}	-40 to 125	°C	-
Junction temperature		T_j	150	°C	-
Storage temperature		T_{stg}	-55 to 150	°C	-

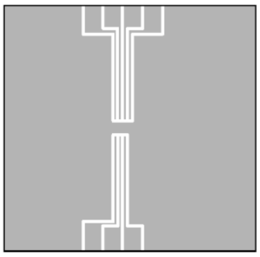
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/ "Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

9. Thermal Characteristics

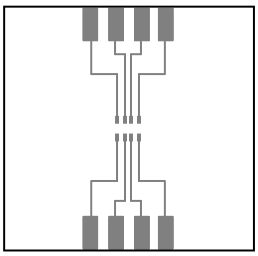
Table 9.1 Thermal characteristics

Characteristics	Symbol	Rating	Unit
Thermal resistance, channel to ambient	$R_{th\ (j\text{-}a)}$	178.6 (Figure 9.1)	°C/W
		357.2 (Figure 9.2)	

$P_D = (T_j - T_a) / R_{th\ (j\text{-}a)}$



Glass epoxy board (a)
Material: FR-4
25.4 mm × 25.4 mm × 0.8 mm



Glass epoxy board (b)
Material: FR-4
25.4 mm × 25.4 mm × 0.8 mm

Figure 9.1 Glass epoxy board (a)   **Figure 9.2 Glass epoxy board (b)**

10. Operating Ranges

Table 10.1 Operating Ranges

Characteristics	Symbol	Pin	Test condition	Min	Typ.	Max	Unit
Supply voltage	$V_{DD(opr)}$	V_{DD}	-	5	12	18	V

11. Electrical Characteristics

Table 11.1 Electrical Characteristics

(Unless otherwise specified, T_j = -40 to 125 °C, V_{DD} = 5 to 18 V)

Characteristics	Symbol	Pin	Test condition	Min	Typ. (Note1)	Max	Unit
Supply current	$I_{DD(off)}$	V_{DD}	V_{DD} = 12 V, V_{IN} = V_{IL}, T_j =25 °C	-	0.7	3.0	mA
	$I_{DD(on)}$	V_{DD}	V_{IN} = V_{IH}, output is open circuit	-	-	5.0	mA
High level input voltage	V_{IH}	IN	-	2.5	-	-	V
Low level input voltage	V_{IL}		-	-	-	1.5	
Input current	I_{IH}	IN	V_{IN} = 5 V	-	19	50	μA
	I_{IL}		V_{IN} = 0 V	-1	-	1	
High level output voltage (Note2)	V_{OUTH1}	OUT	V_{DD} = 5 V, V_{IN} = V_{IH}, I_{OUT} = -100 μA	V_{DD} +8.0	V_{DD} +13	V_{DD} +18.0	V
	V_{OUTH2}	OUT	V_{DD} = 8 to 18 V, V_{IN} = V_{IH}, I_{OUT} = -100 μA	V_{DD} +10.0	V_{DD} +15.7	V_{DD} +18.0	V
Output clamp voltage	V_{clamp}	OUT	V_{IN} = V_{IH}	31	36	40	V
Output resistance	R_{SINK}	OUT	V_{IN} = V_{IL}, I_{OUT} = 1 mA	-	510	800	Ω
Diagnosis output leakage current	I_{DIAGH}	DIAG	V_{IN} = V_{IL}, V_{DIAG} = 5 V	-	-	10	μA
Diagnosis output voltage	V_{DIAGL}	DIAG	V_{IN} = V_{IH}, I_{DIAG} = 500 μA	-	0.22	0.40	V
Short circuit detection voltage (Note3)	V_{ISOC}	R_{ISref}	V_{DD} = 12 V, R_{ISref} pin is open circuit	0.80	1.02	1.20	V
R_{ISref} pin output current	$I_{ISref(1)}$	R_{ISref}	V_{RISref} = 0.2 V	-60	-38	-20	μA
	$I_{ISref(2)}$	R_{ISref}	V_{RISref} = 0.4 V	-60	-38	-20	μA
	$I_{ISref(3)}$	R_{ISref}	V_{RISref} = 0.6 V	-60	-38	-20	μA
Switching time	t_{on}	OUT	Refer to Test circuit 1 (Figure 12.1) T_j = 25 °C	-	450	800	μs
	t_{off}			-	480	800	
Output current for reverse connection	$I_{REV(1)}$	OUT	Refer to Test circuit 2 (Figure 12.3) V_{DD}= -5 to -18 V, T_j = 25 °C	-1	-	-	μA
	$I_{REV(2)}$	OUT	Refer to Test circuit 2 (Figure 12.3) V_{DD}= -5 to -18 V, T_j = -40 to 125 °C	-10	-	-	

Note 1: Typical values are V_{DD}=12 V and T_j=25 °C. If measurement conditions are specified, follow those conditions.

Note 2: About the high level output voltage.
It has a built-in circuit that clamps V_{OUT}=V_{DD}+15.7 V (typ.) to drive the external MOSFET at the optimal voltage.
In addition, the output voltage is clamped at 36 V (typ.) to protect the internal circuit elements.

Note 3: The current detection voltage is controllable, when connecting resistance to R_{ISref} pin.
Please note that when V_{RISref} (R_{IS}×I_{ISref}) > V_{ISOC}, the V_{ISOC} voltage is the load short detection voltage.

12. Measurement circuit diagram

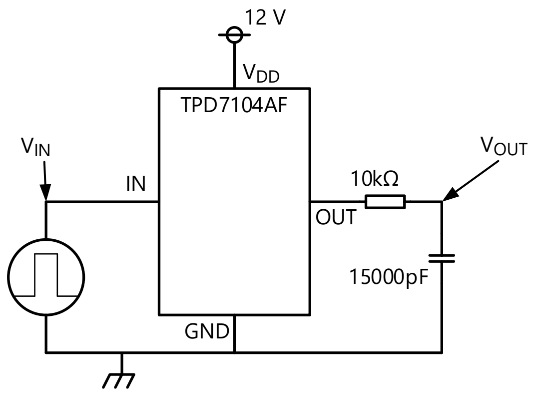


Figure 12.1 Measurement circuit diagram 1 (Switching time measurement circuit)

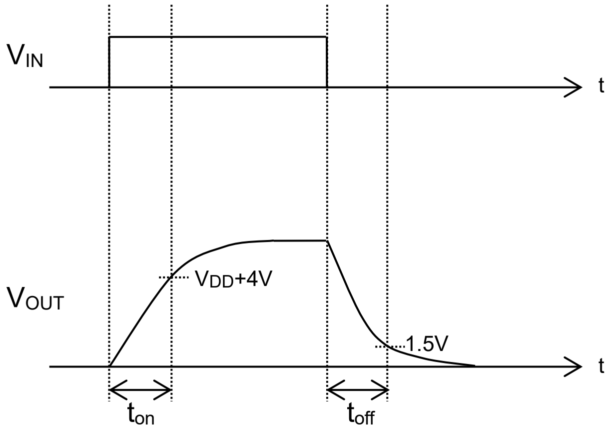


Figure 12.2 Switching time measurement waveform

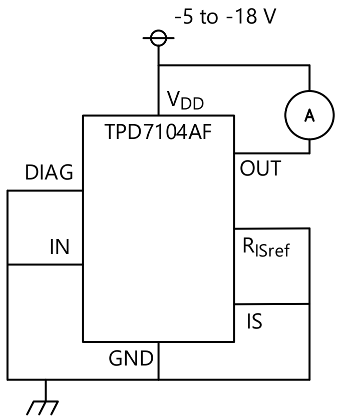


Figure 12.3 Measurement circuit diagram 2

(Output current measurement circuit when power supply is connected in reverse)

13. Characteristic curves

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

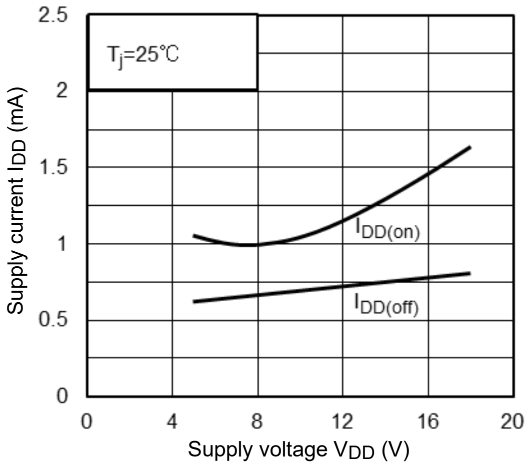


Figure 13.1 I_{DD} – V_{DD}

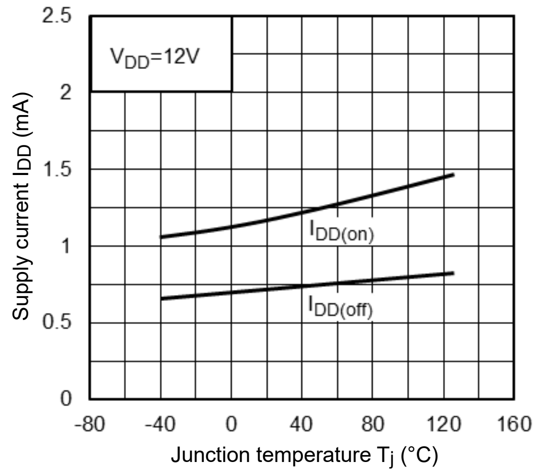


Figure 13.2 I_{DD} – T_j

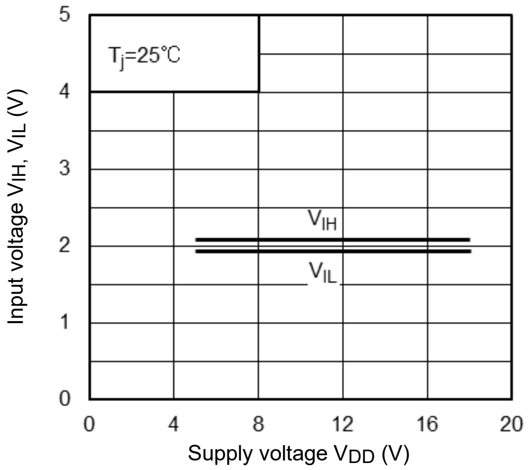


Figure 13.3 V_{IH}, V_{IL} – V_{DD}

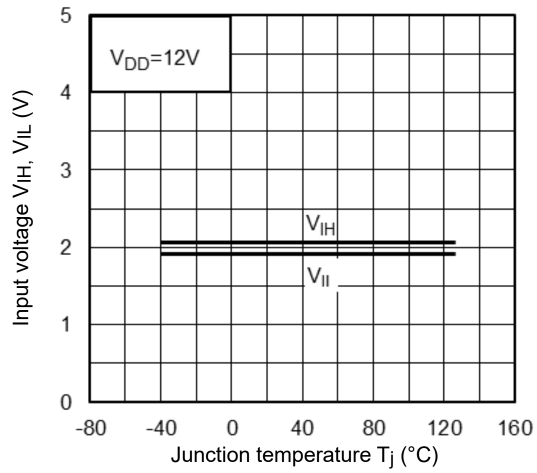


Figure 13.4 V_{IH}, V_{IL} – T_j

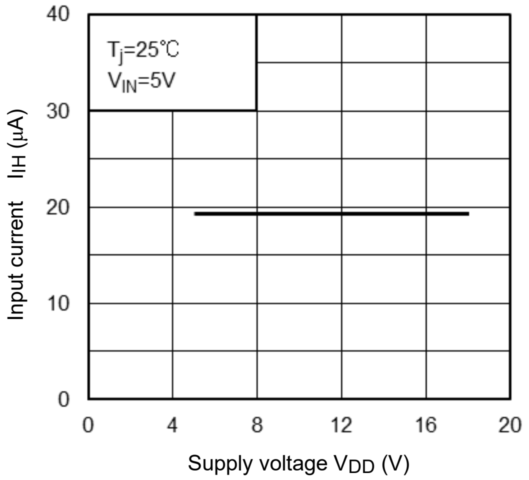


Figure 13.5 I_{IH} – V_{DD}

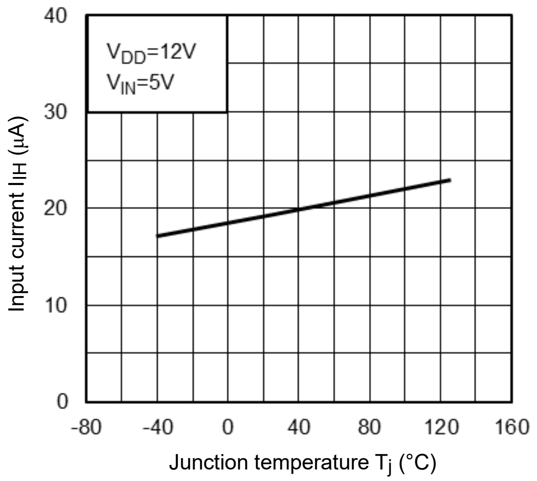


Figure 13.6 I_{IH} – T_j

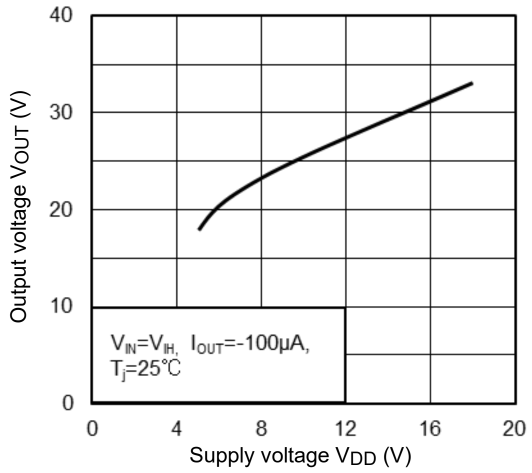


Figure 13.7 VOUT – VDD

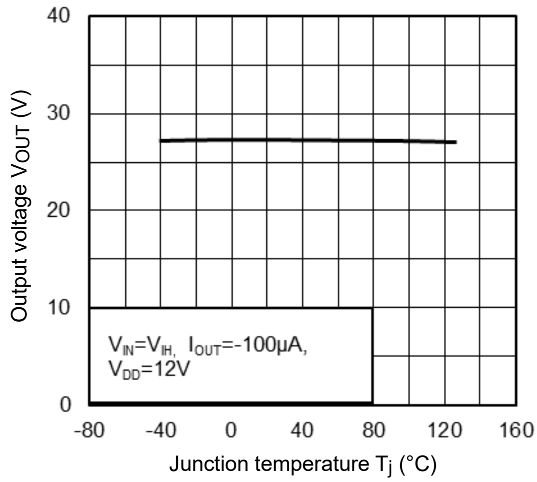


Figure 13.8 VOUT – Tj

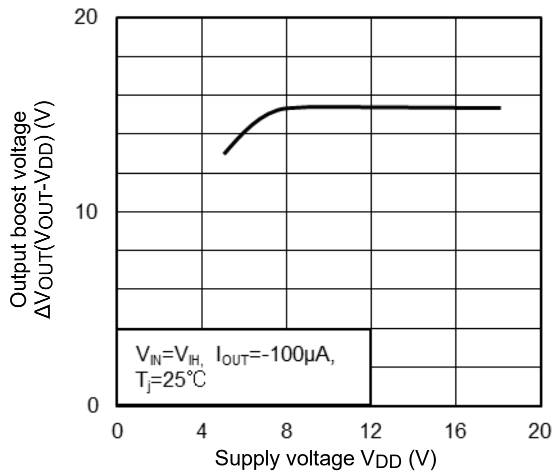


Figure 13.9 ΔVOUT (VOUT-VDD) – VDD

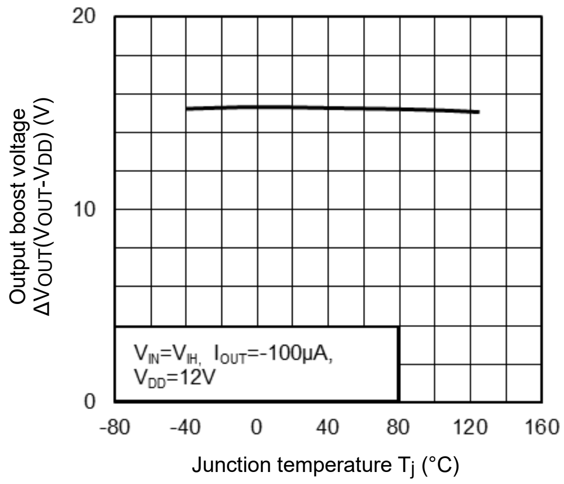


Figure 13.10 ΔVOUT (VOUT-VDD) – Tj

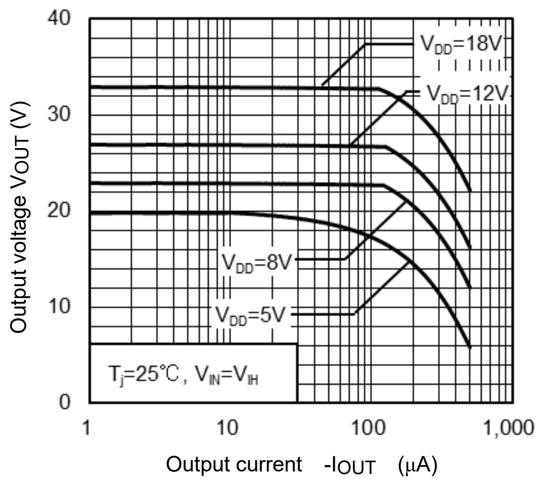


Figure 13.11 VOUT – -IOUT

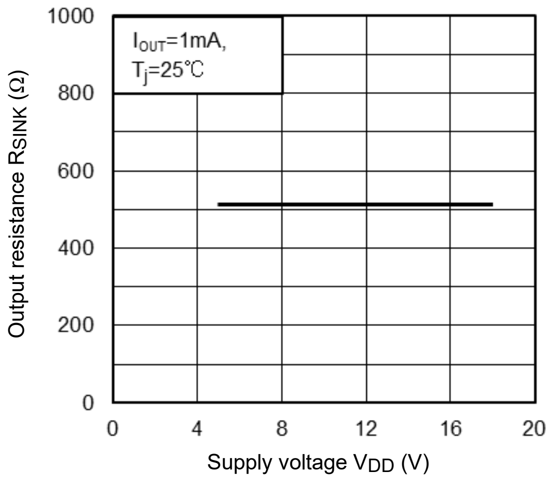


Figure 13.12 RSINK – VDD

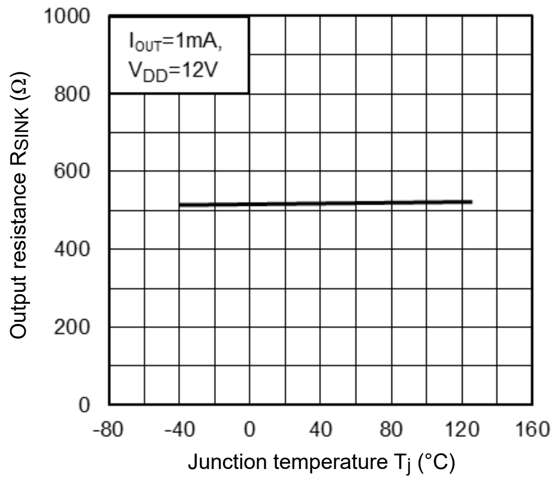


Figure 13.13 RSINK – Tj

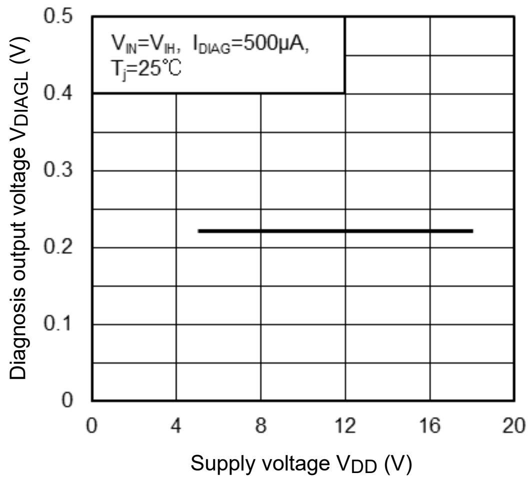


Figure 13.14 VDIAGL – VDD

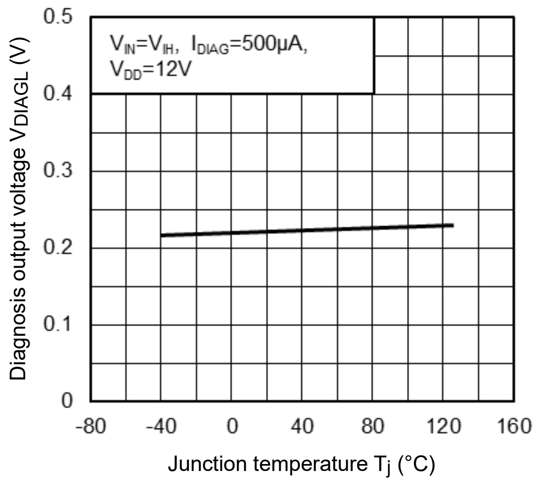


Figure 13.15 VDIAGL – Tj

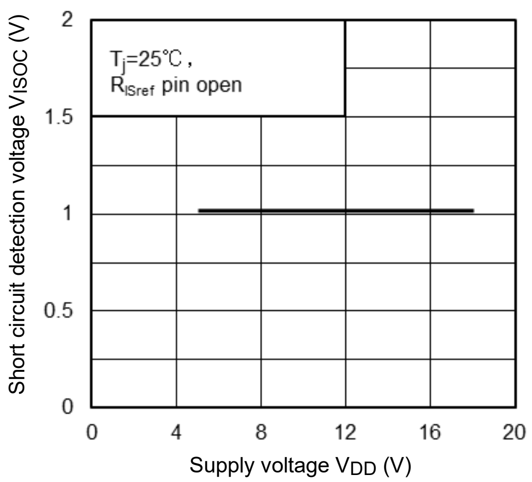


Figure 13.16 VISOC – VDD

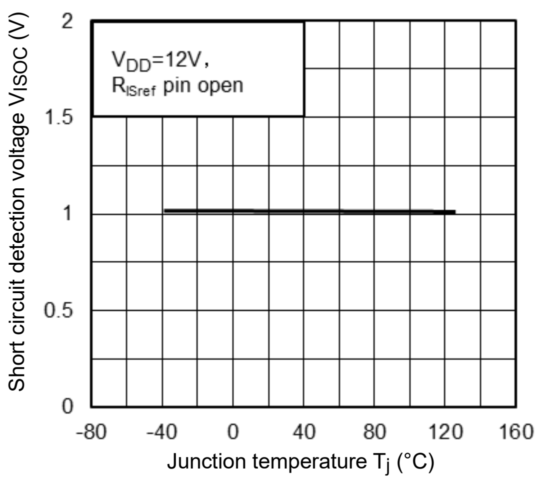


Figure 13.17 VISOC – Tj

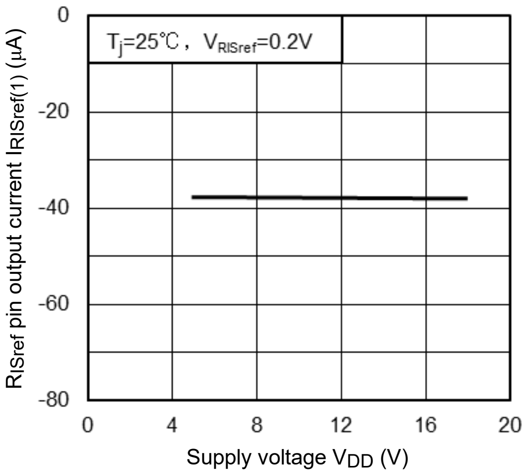


Figure 13.18 $I_{RISref(1)}$ – V_{DD}

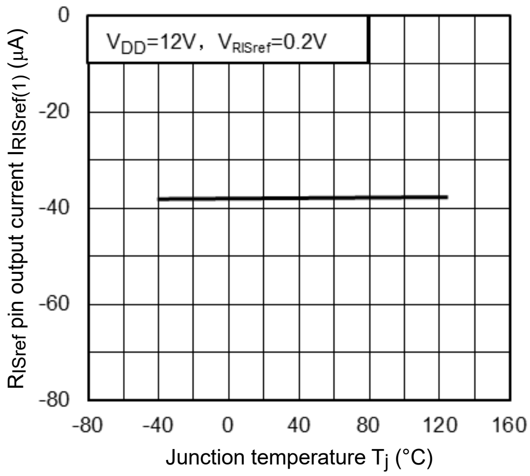


Figure 13.19 $I_{RISref(1)}$ – T_j

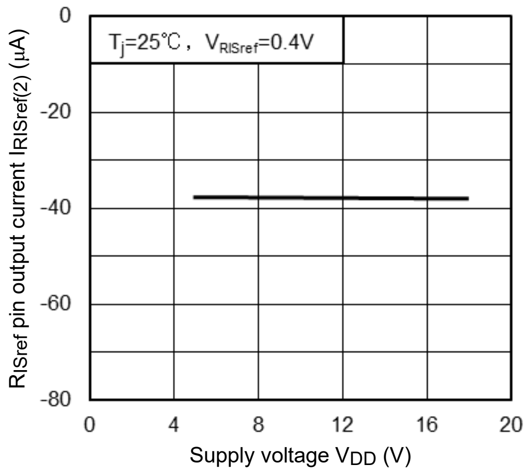


Figure 13.20 $I_{RISref(2)}$ – V_{DD}

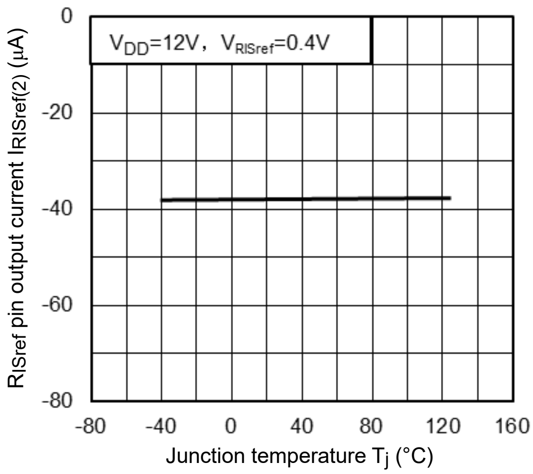


Figure 13.21 $I_{RISref(2)}$ – T_j

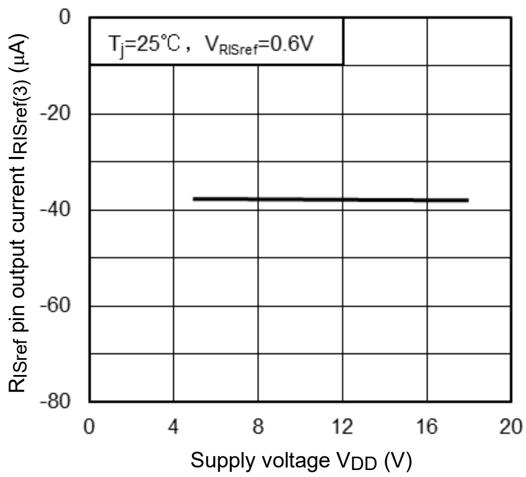


Figure 13.22 $I_{RISref(3)}$ – V_{DD}

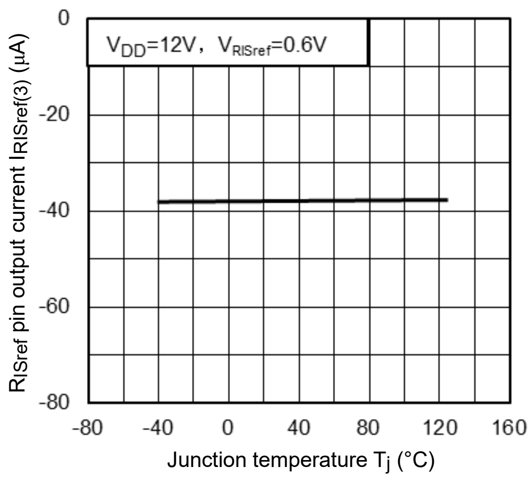


Figure 13.23 $I_{RISref(3)}$ – T_j

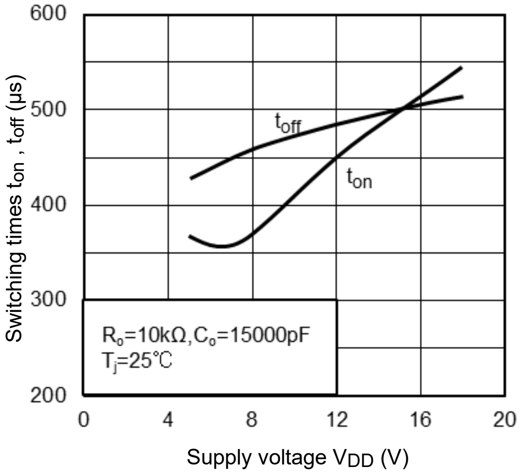


Figure 13.24 t_{on}, t_{off} – V_{DD}

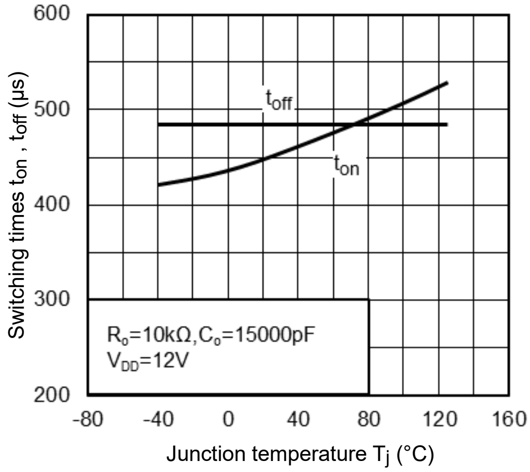


Figure 13.25 t_{on}, t_{off} – T_j

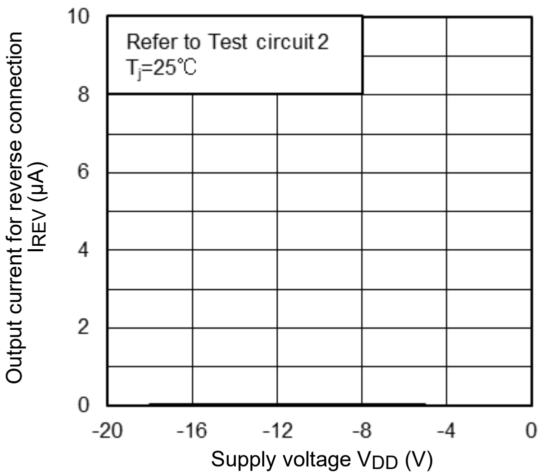


Figure 13.26 $I_{REV(1)}$ – V_{DD}

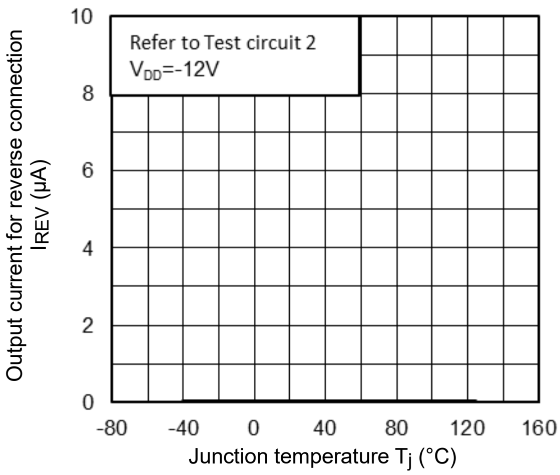


Figure 13.27 $I_{REV(2)}$ – T_j

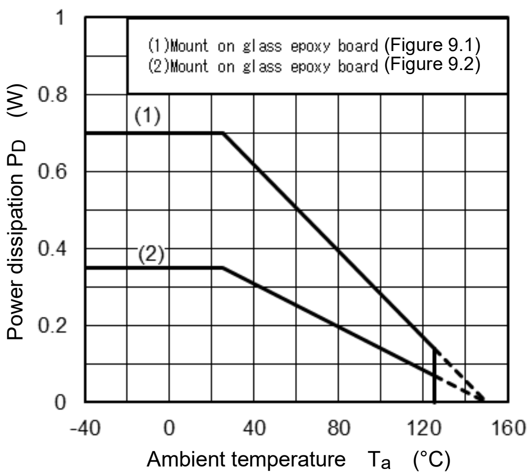


Figure 13.28 P_D – T_a

14. Package Information

14.1. Package Dimensions

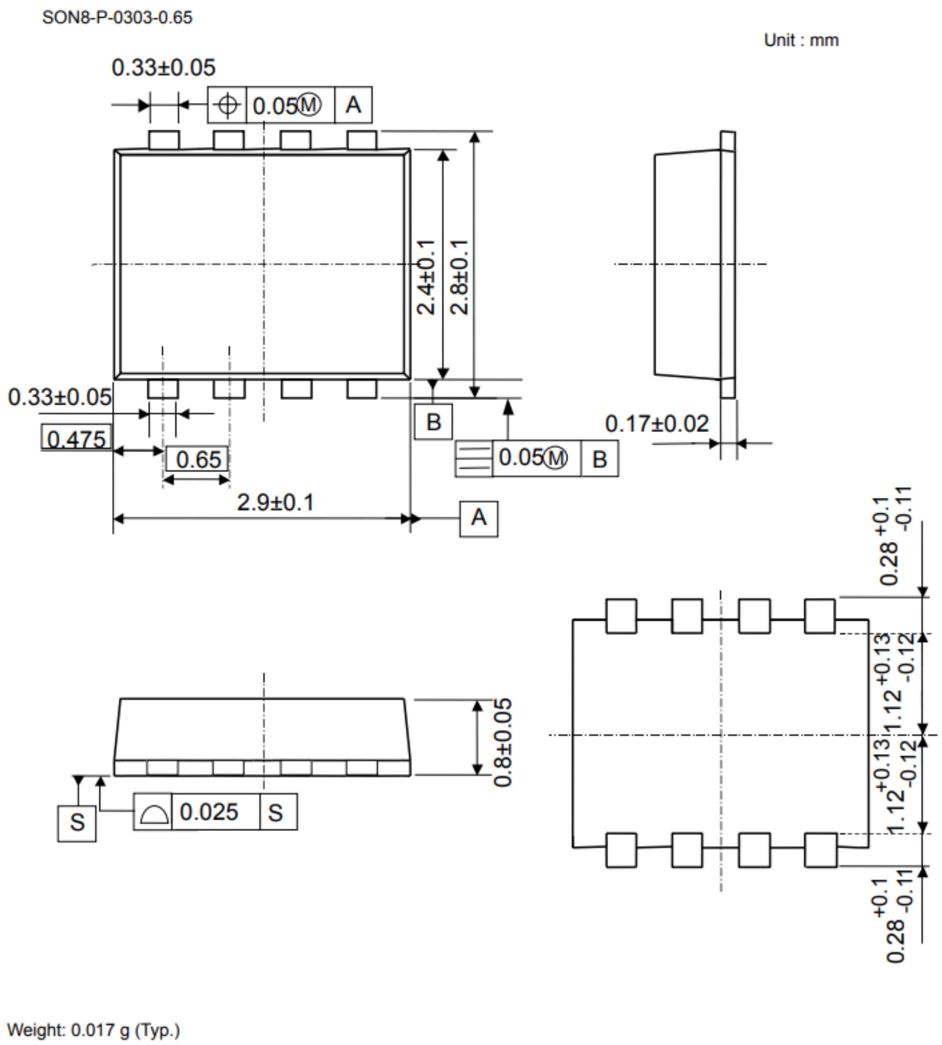


Figure 14.1 Package Dimensions

14.2. Marking

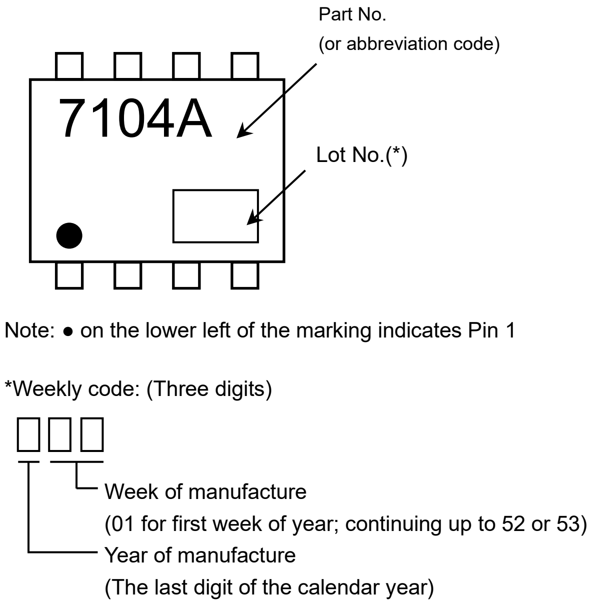


Figure 14.2 Marking

14.3. Land Pattern Dimensions for Reference only

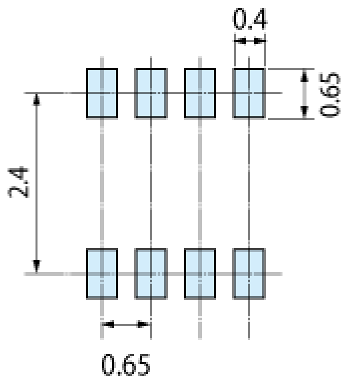


Figure 14.3 Land Pattern Dimensions for Reference only

15. IC Usage Considerations

15.1. Notes on Handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. None of the multiple ratings can be exceeded. Exceeding the absolute maximum ratings may cause destruction, damage and deterioration, and may result in injury due to explosion or burning.

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