

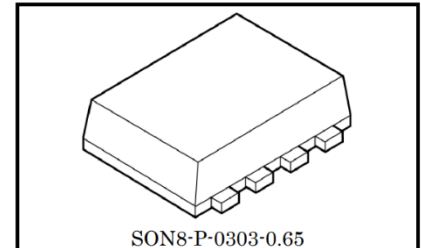
TOSHIBA Intelligent Power Device Silicon Monolithic MOS Integrated Circuit

TPD7104AF

1 channel High-Side N channel MOSFET Gate Driver

1. Description

TPD7104AF is a 1channel high-side N channel MOSFET gate driver. This IC contains a charge pump circuit, allowing easy configuration of a high-side switch for large-current applications.



weight: 0.017g (typ.)

2. Applications

- Junction Boxes for Automotive.
- Power distribution modules for Automotive.
- Semiconductor relays.

3. Features

- Charge pump circuit is built in.
- Built-in short circuit (overcurrent detection) and reverse battery protection.
- AEC-Q100 qualified.
- The package is a small surface mount type PS-8, and the packaging is embossed tape.

Note: Due to its MOS structure. This product is sensitive to static electricity.

Start of commercial production
2015-08

4. Block Diagram

4.1. Application example of load switch circuit. (disable reverse polarity protection)

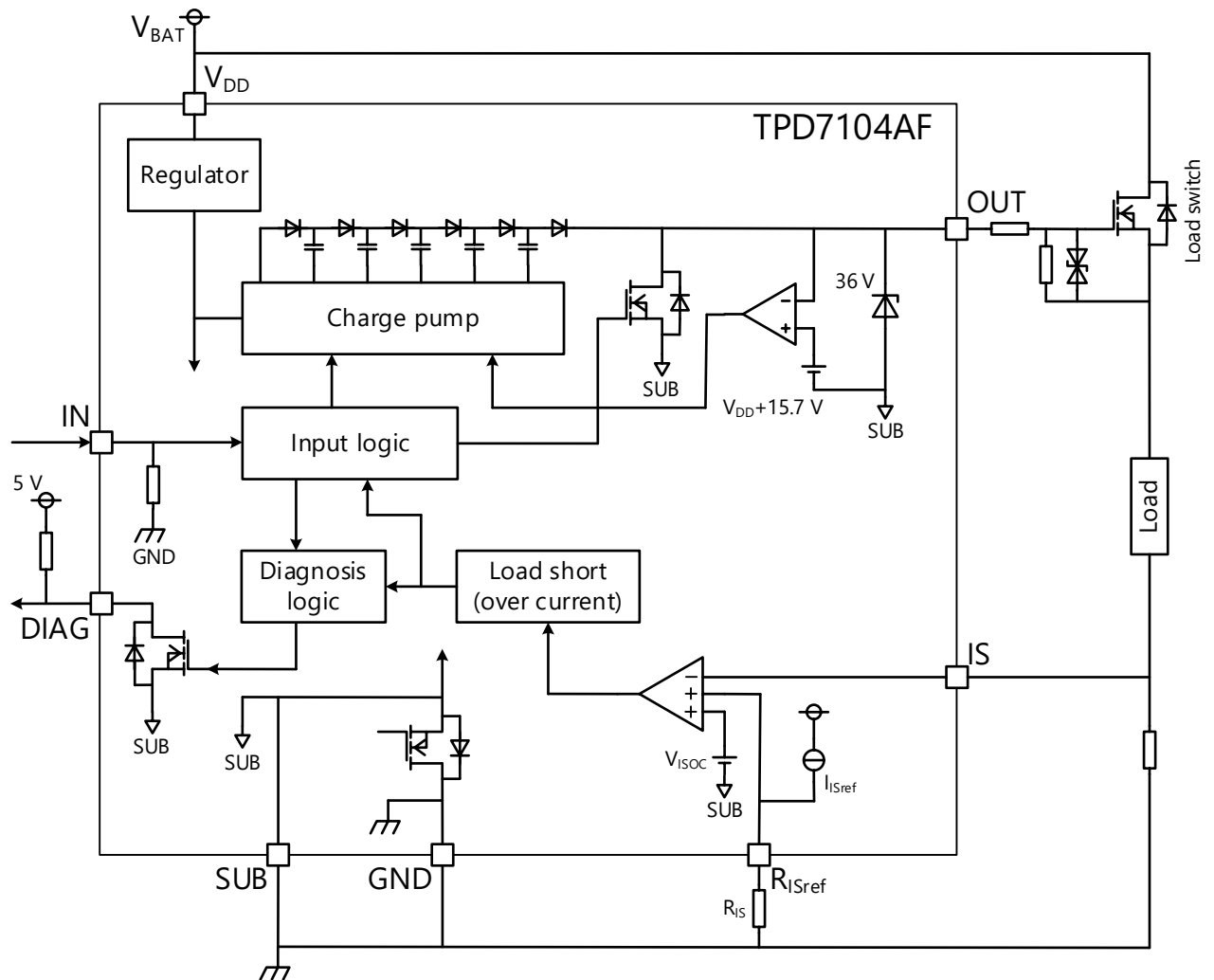


Figure 4.1 Block diagram (load switch circuit)

4.2. Application example of reverse polarity protection circuit. (enable reverse polarity protection)

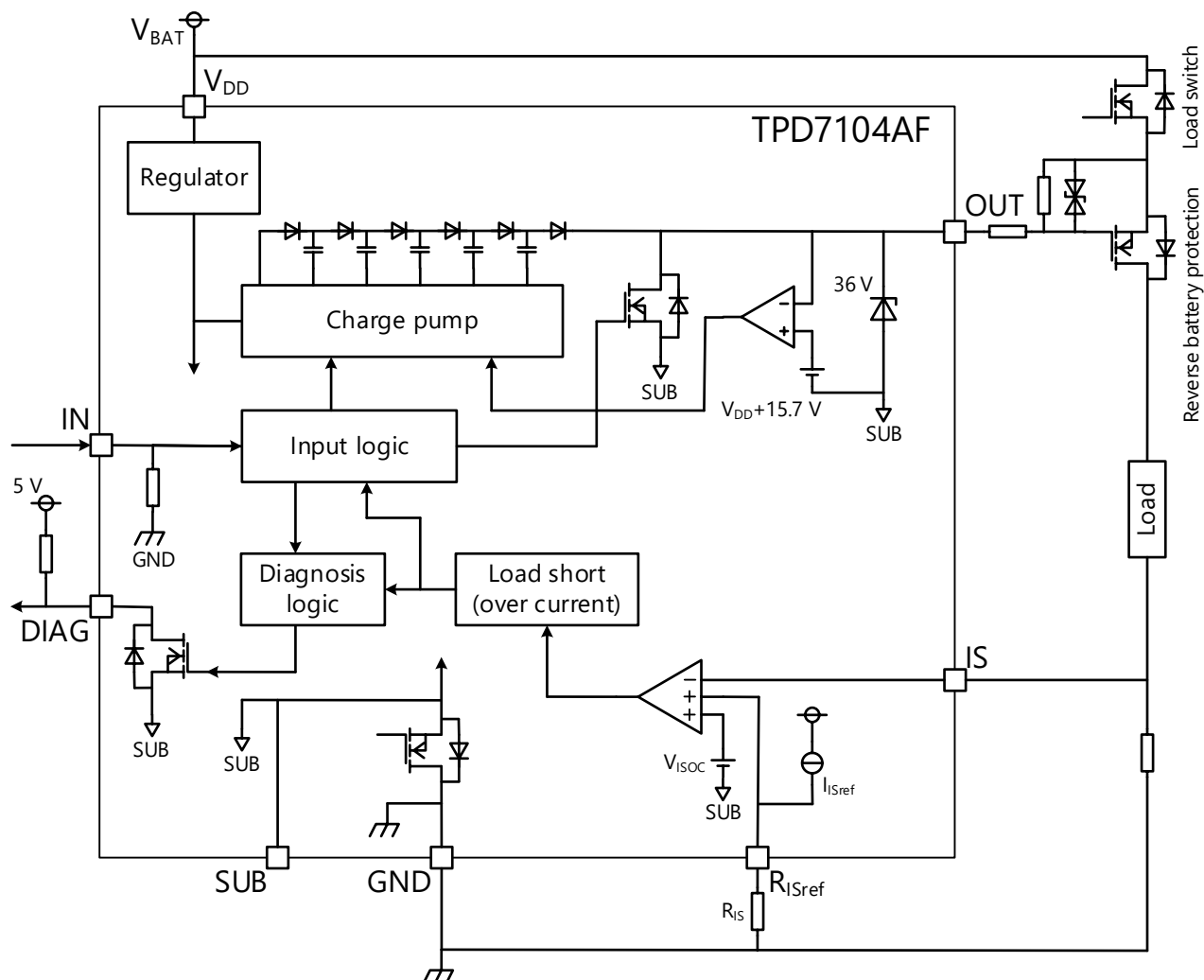


Figure 4.2 Block Diagram (reverse polarity protection)

5. Pin Assignments

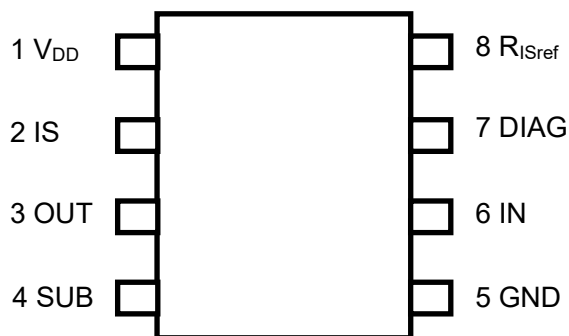


Figure 5.1 Pin Assignments (top view)

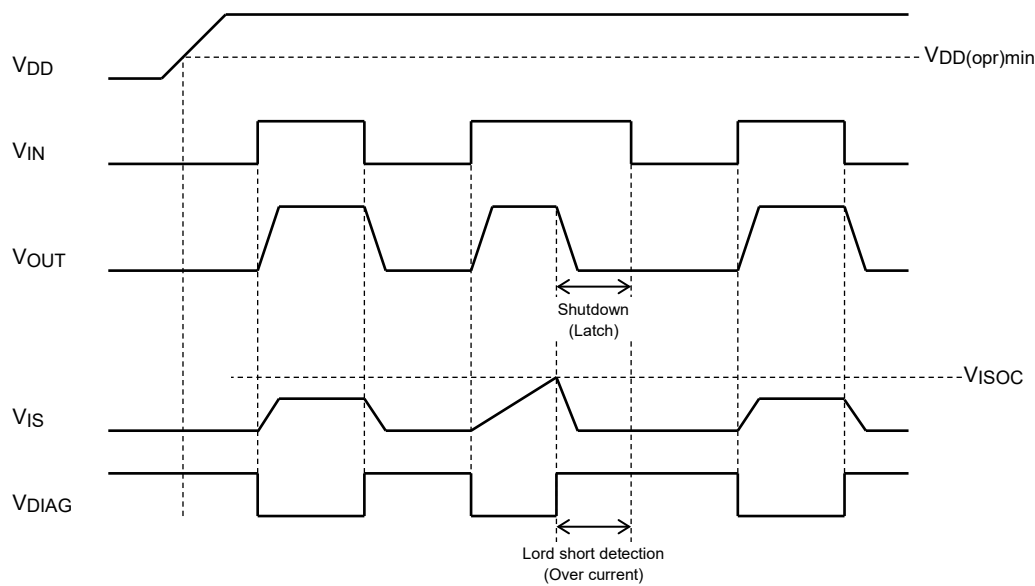
6. Pin Description

Table 6.1 Pin Description

Pin No.	Symbol	I/O	Description
1	V _{DD}	—	Power supply pin.
2	IS	IN	Detection pin for short circuit. If short circuit detection is disabled, IS pin should be connected to GND.
3	OUT	OUT	Output pin for driving an external MOSFET. V _{OUT} set to L when detect short circuit.
4	SUB	—	If reverse polarity protection is enabled, SUB pin should be open. If reverse polarity protection is disenabled, SUB pin should be connected to GND.
5	GND	—	Ground pin.
6	IN	IN	Input signal for external FET control. A pull-down resistor is built in.
7	DIAG	OUT	Diagnosis output pin. It is open drain composition. When a load short is detected, V _{DIAG} becomes H.
8	R _{ISref}	OUT	Adjust pin for sense level of load short detection. If load short detection level is not changed from V _{ISOC} =1.02V (typ.), R _{ISref} pin should be open.

7. Functional Description

7.1. Timing chart



Note: When a short-circuit condition is detected, the IC immediately shuts down the output and transitions to a latch state to protect the external MOSFET. During this latch state, V_{DIAG} is kept H. The latch state is cleared when the V_{IN} is set to L.

Figure 7.1 Timing chart

7.2. Truth table

Table 7.1 Truth table

V_{IN}	V_{OUT}	Charge pump	V_{IS} (Note 1)	V_{DIAG}	Mode
L	L	Charge pump stop (oscillation is stopped)	L	H (Note 2)	Normal
H	H	Charge pump operation.	L	L	
L	L	Charge pump stop (oscillation is stopped)	H	H (Note 2)	Load short
H	L	Charge pump stop (oscillation is stopped)	H	H (Note 2)	
-	Hz (Note 3)	-	-	Hz (Note 3)	Reverse battery (SUB pin open)

Note 1: H: $V_{IS} > V_{ISOC}$, L: $V_{IS} < V_{ISOC}$, V_{ISOC} : short circuit detection voltage.

Note 2: The DIAG output is configured as an N-channel open-drain MOSFET. When V_{DIAG} is 'H', the MOSFET is OFF.

Note 3: Hz: High impedance.

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings (Note)

(T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit	Remarks
Power supply voltage	DC	V _{DD(1)}	-0.3 to 24.0	V	-
	Pulse	V _{DD(2)}	40.0	V	t=300ms single pulse
Power supply reverse connection		-V _{DD(3)}	18.0	V	SUB open
Input voltage		V _{IN}	-0.3 to 6.0	V	-
Output source current		I _{OUT(-)}	Internal capacity	mA	Source current
Output sink current		I _{OUT(+)}	5	mA	Sink current
IS pin voltage		V _{IS}	-0.3 to 6.0	V	-
Diagnosis output voltage		V _{DIAG}	-0.3 to 6.0	V	-
Diagnosis pin current		I _{DIAG}	5	mA	-
Power dissipation		P _{D(1)}	0.70	W	Refer to Figure 9.1
Power dissipation		P _{D(2)}	0.35	W	Refer to Figure 9.2
Operating temperature		T _{opr}	-40 to 125	°C	-
Junction temperature		T _j	150	°C	-
Storage temperature		T _{stg}	-55 to 150	°C	-

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these ratings would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause breakdown, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

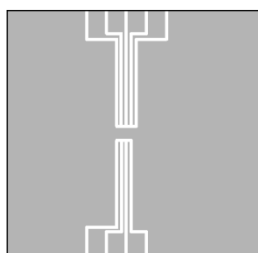
Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

9. Thermal Characteristics

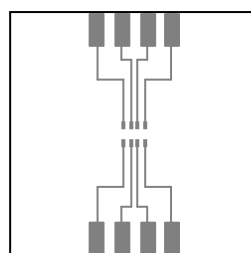
Table 9.1 Thermal characteristics

Characteristics	Symbol	Rating	Unit
Thermal resistance, channel to ambient	R _{th(j-a)}	178.6 (Figure 9.1)	°C/W
		357.2 (Figure 9.2)	

$$P_D = (T_j - T_a) / R_{th(j-a)}$$



Glass epoxy board (a)
Material: FR-4
25.4 mm × 25.4 mm × 0.8 mm



Glass epoxy board (b)
Material: FR-4
25.4 mm × 25.4 mm × 0.8 mm

Figure 9.1 Glass epoxy board (a)

Figure 9.2 Glass epoxy board (b)

10. Operating Ranges

Table 10.1 Operating Ranges

Characteristics	Symbol	Pin	Test condition	Min	Typ.	Max	Unit
Supply voltage	$V_{DD(opr)}$	V_{DD}	-	5	12	18	V

11. Electrical Characteristics

Table 11.1 Electrical Characteristics

(Unless otherwise specified, $T_j = -40$ to 125 °C, $V_{DD} = 5$ to 18 V)

Characteristics	Symbol	Pin	Test condition	Min	Typ. (Note1)	Max	Unit
Supply current	$I_{DD(off)}$	V_{DD}	$V_{DD} = 12$ V, $V_{IN} = V_{IL}$, $T_j = 25$ °C	-	0.7	3.0	mA
	$I_{DD(on)}$	V_{DD}	$V_{IN} = V_{IH}$, output is open	-	-	5.0	mA
High level input voltage	V_{IH}	IN	-	2.5	-	-	V
Low level input voltage	V_{IL}		-	-	-	1.5	
Input current	I_{IH}	IN	$V_{IN} = 5$ V	-	19	50	μ A
	I_{IL}		$V_{IN} = 0$ V	-1	-	1	
High level output voltage	V_{OUTH1}	OUT	$V_{DD} = 5$ V, $V_{IN} = V_{IH}$, $I_{OUT} = -100$ μ A	V_{DD} +8.0	V_{DD} +13	V_{DD} +18.0	V
	V_{OUTH2}	OUT	$V_{DD} = 8$ to 18 V, $V_{IN} = V_{IH}$, $I_{OUT} = -100$ μ A	V_{DD} +10.0	V_{DD} +15.7	V_{DD} +18.0	V
Output clamp voltage	V_{clamp}	OUT	$V_{IN} = V_{IH}$	31	36	40	V
Output resistance	R_{SINK}	OUT	$V_{IN} = V_{IL}$, $I_{OUT} = 1$ mA	-	510	800	Ω
Diagnosis output leakage current	I_{DIAGH}	DIAG	$V_{IN} = V_{IL}$, $V_{DIAG} = 5$ V	-	-	10	μ A
Diagnosis output voltage	V_{DIAGL}	DIAG	$V_{IN} = V_{IH}$, $I_{DIAG} = 500$ μ A	-	0.22	0.40	V
Short circuit detection voltage (Note2)	V_{ISOC}	IS	$V_{DD} = 12$ V, R_{ISref} pin is open	0.80	1.02	1.20	V
R_{ISref} pin output current	$I_{ISref(1)}$	R_{ISref}	$V_{RISref} = 0.2$ V	-60	-38	-20	μ A
	$I_{ISref(2)}$	R_{ISref}	$V_{RISref} = 0.4$ V	-60	-38	-20	μ A
	$I_{ISref(3)}$	R_{ISref}	$V_{RISref} = 0.6$ V	-60	-38	-20	μ A
Switching time	t_{on}	OUT	Refer to Measurement circuit 1 (Figure 12.1) $T_j = 25$ °C	-	450	800	μ s
	t_{off}			-	480	800	
Output current for reverse connection	$I_{REV(1)}$	OUT	Refer to Measurement circuit 2 (Figure 12.3) $V_{DD} = -5$ to -18 V, $T_j = 25$ °C	-1	-	-	μ A
	$I_{REV(2)}$	OUT	Refer to Measurement circuit 2 (Figure 12.3) $V_{DD} = -5$ to -18 V, $T_j = -40$ to 125 °C	-10	-	-	

Note 1: Assumptions for standard values: $V_{DD}=12$ V and $T_j=25$ °C. If measurement conditions are specified, follow those conditions.

Note 2: By connecting a resistor to the R_{ISref} pin, the voltage at the R_{ISref} pin is equal to $R_{IS} * I_{ISref}$.

When V_{RISref} ($R_{IS} * I_{ISref}$) is higher than V_{ISOC} , the short-circuit detection voltage is V_{ISOC} .

When V_{RISref} ($R_{IS} * I_{ISref}$) is less than V_{ISOC} , the short-circuit detection voltage is V_{RISref} .

12. Measurement circuit diagram

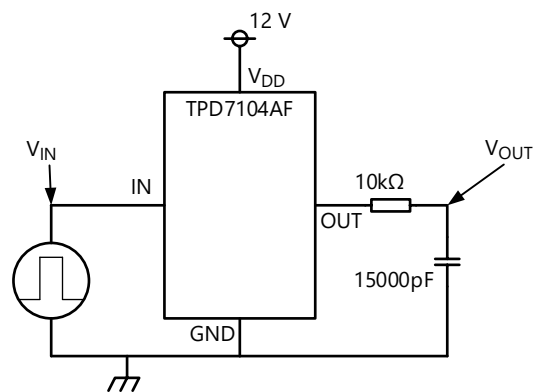


Figure 12.1 Measurement circuit diagram 1
(Switching time measurement circuit)

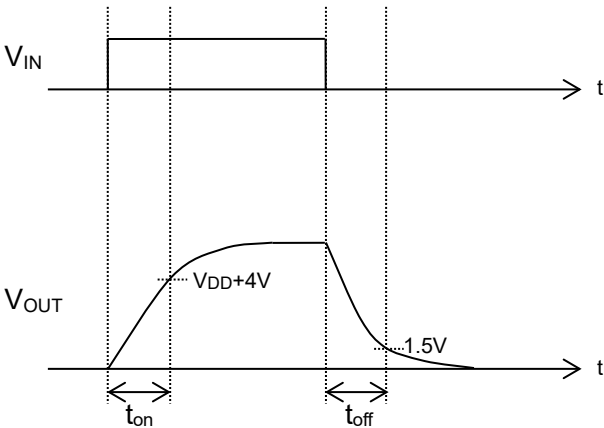


Figure 12.2 Switching time measurement waveform

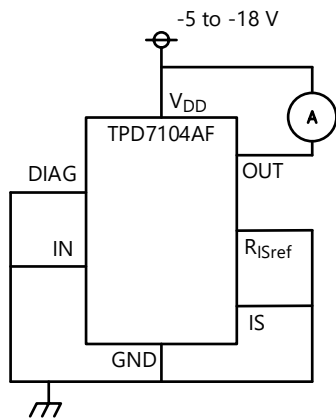


Figure 12.3 Measurement circuit diagram 2
(Output current measurement circuit under reverse polarity connection)

13. Characteristic curves

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

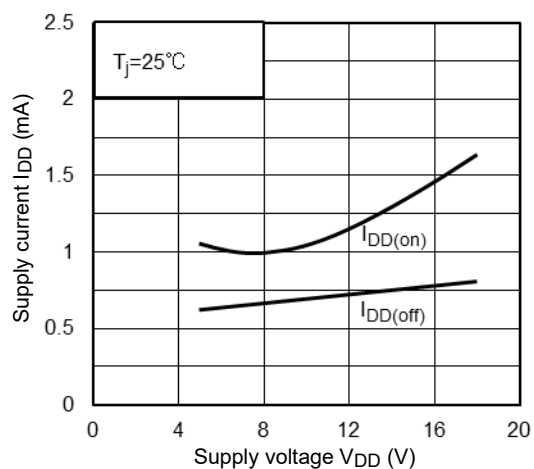


Figure 13.1 $I_{DD} - V_{DD}$

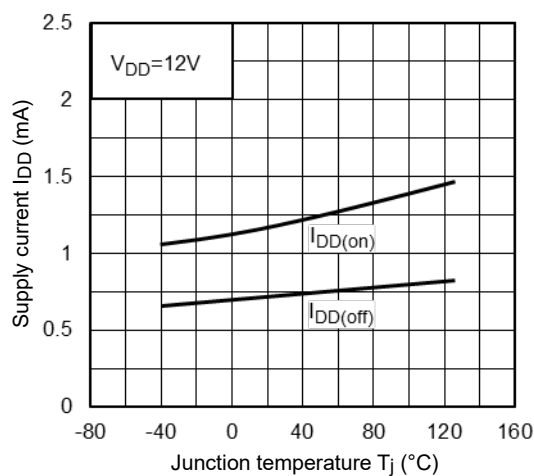


Figure 13.2 $I_{DD} - T_J$

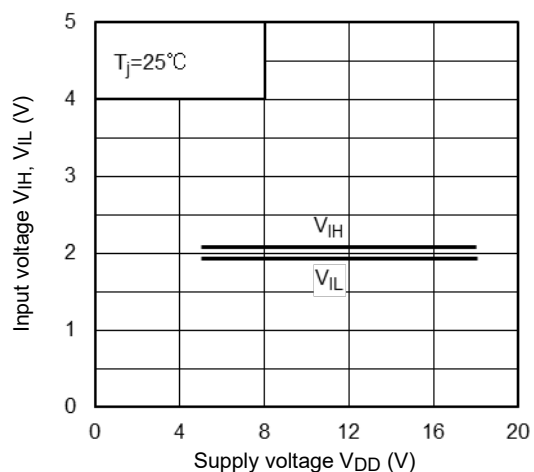


Figure 13.3 $V_{IH}, V_{IL} - V_{DD}$

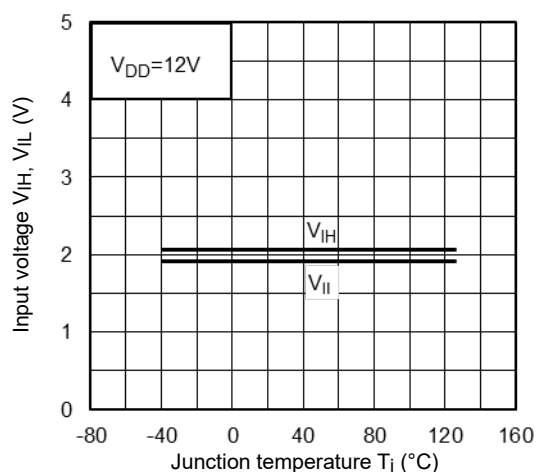


Figure 13.4 $V_{IH}, V_{IL} - T_J$

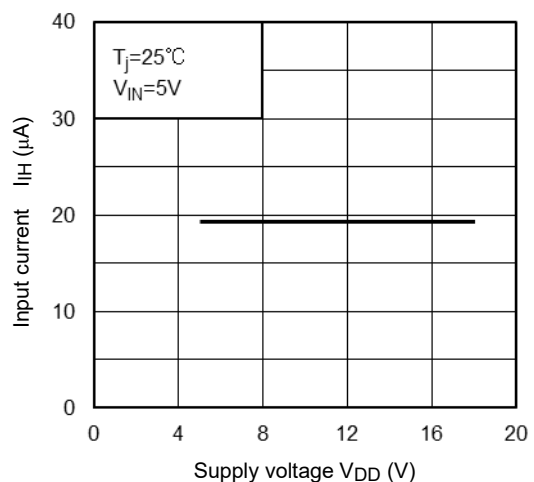


Figure 13.5 $I_{IH} - V_{DD}$

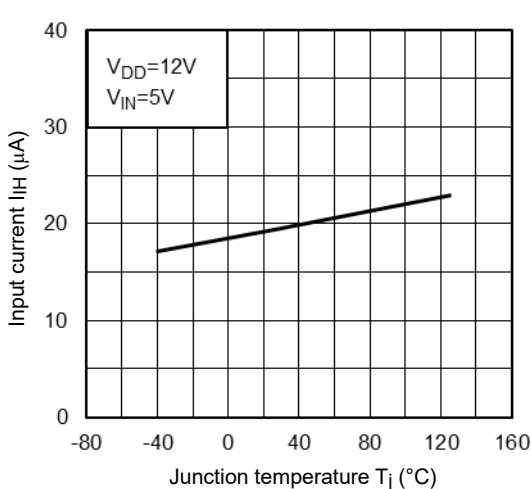


Figure 13.6 $I_{IH} - T_J$

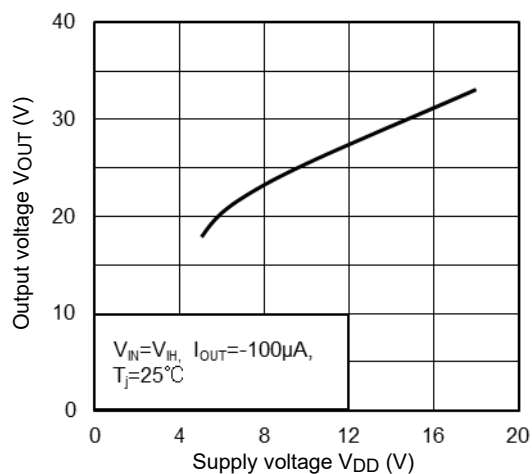


Figure 13.7 $V_{OUT} - V_{DD}$

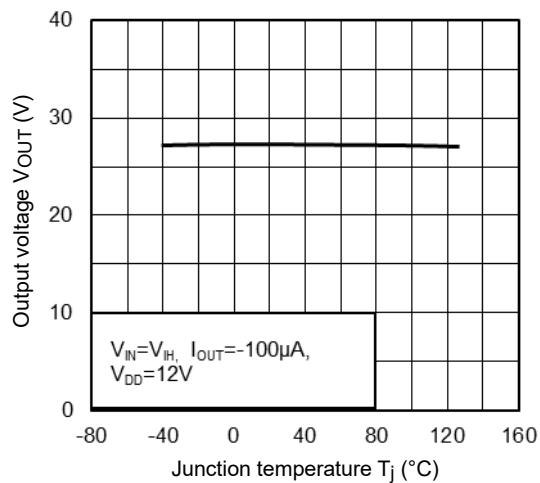


Figure 13.8 $V_{OUT} - T_J$

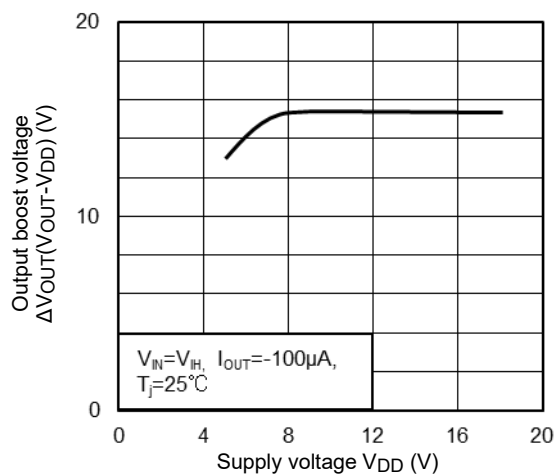


Figure 13.9 $\Delta V_{OUT}(V_{OUT}-V_{DD}) - V_{DD}$

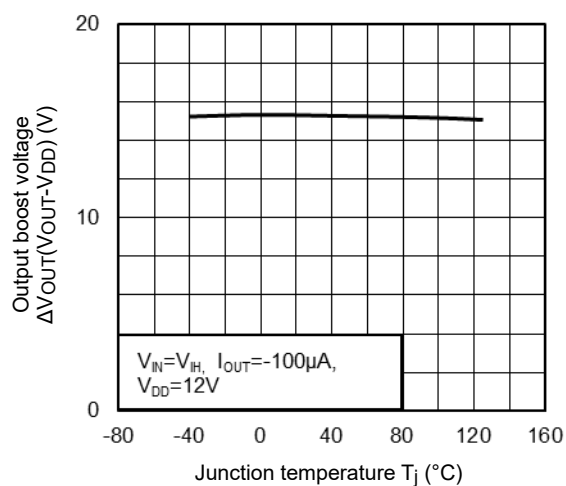


Figure 13.10 $\Delta V_{OUT}(V_{OUT}-V_{DD}) - T_J$

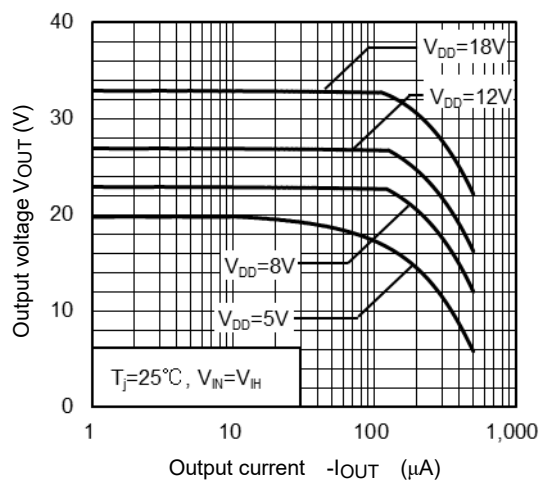


Figure 13.11 $V_{OUT} - I_{OUT}$

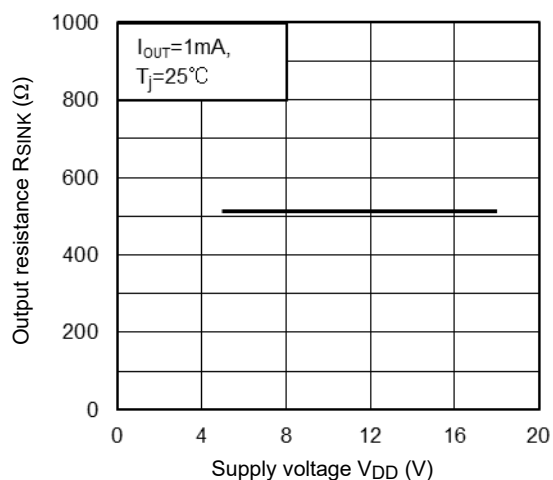


Figure 13.12 $R_{SINK} - V_{DD}$

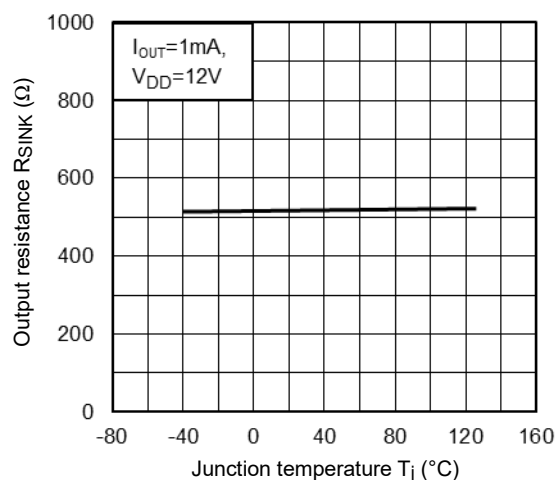


Figure 13.13 $R_{SINK} - T_j$

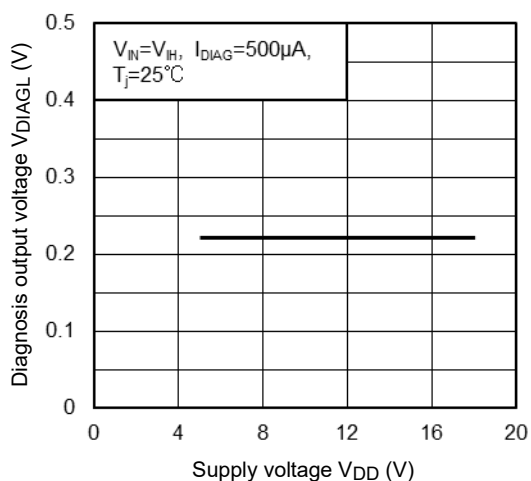


Figure 13.14 $V_{DIAGL} - V_{DD}$

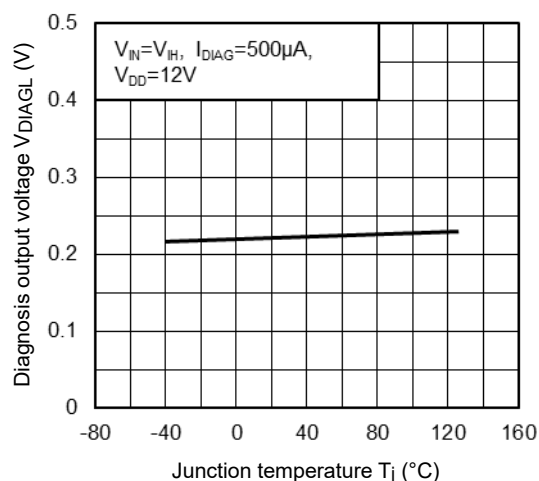


Figure 13.15 $V_{DIAGL} - T_j$

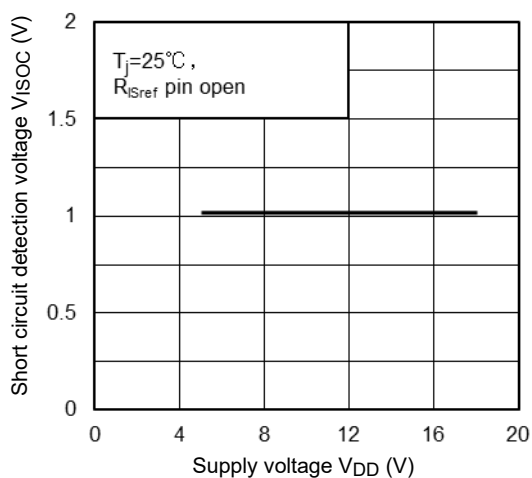


Figure 13.16 $V_{ISOC} - V_{DD}$

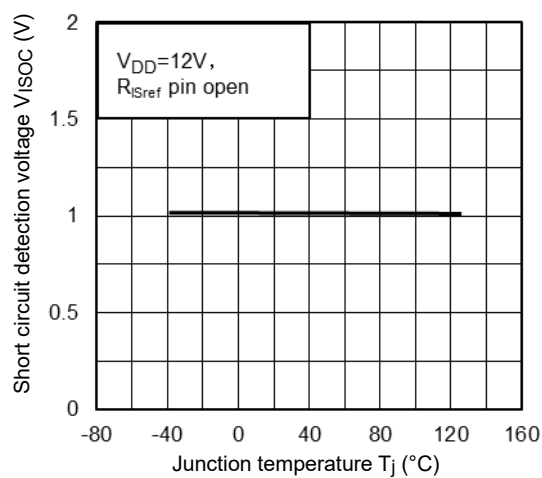


Figure 13.17 $V_{ISOC} - T_j$

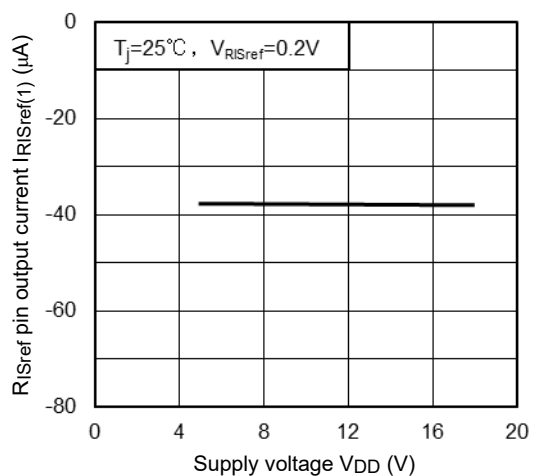


Figure 13.18 $I_{RISref(1)} - V_{DD}$

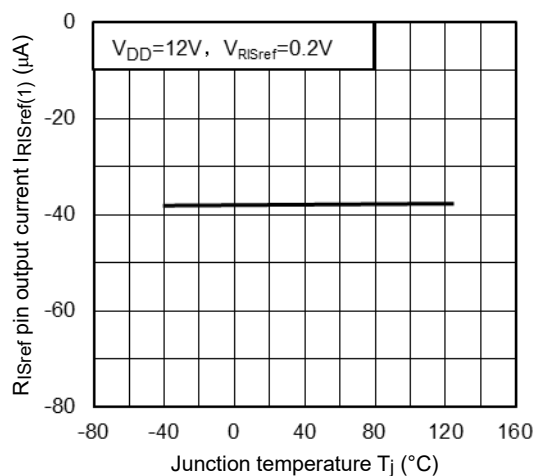


Figure 13.19 $I_{RISref(1)} - T_j$

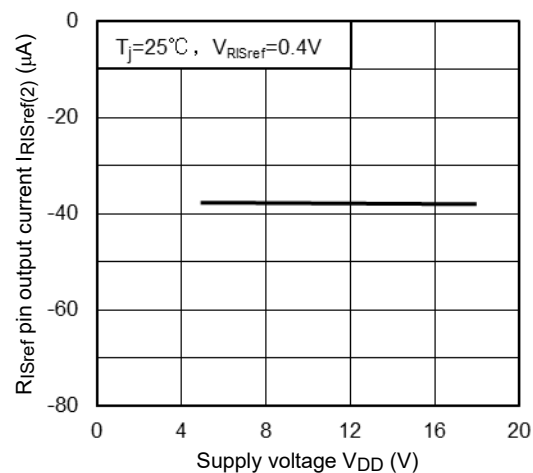


Figure 13.20 $I_{RISref(2)} - V_{DD}$

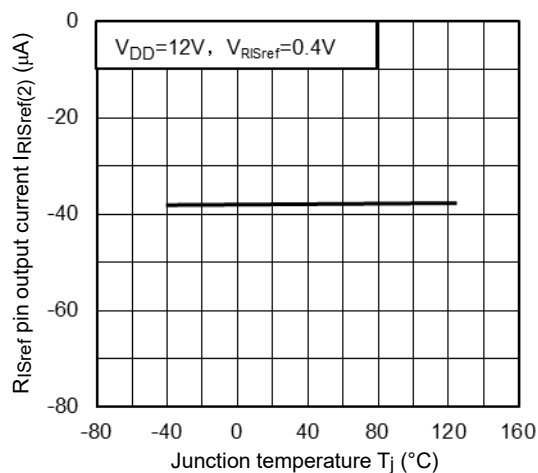


Figure 13.21 $I_{RISref(2)} - T_j$

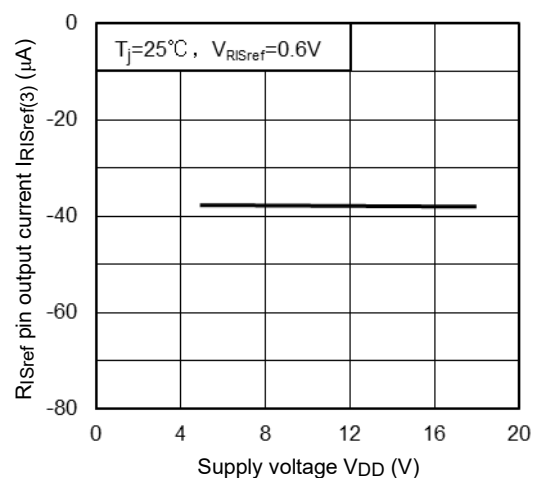


Figure 13.22 $I_{RISref(3)} - V_{DD}$

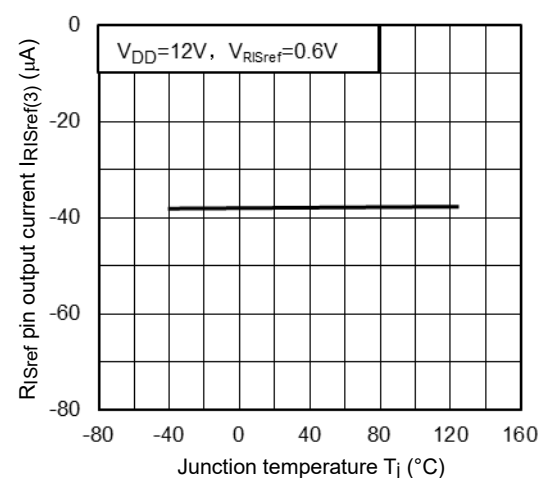


Figure 13.23 $I_{RISref(3)} - T_j$

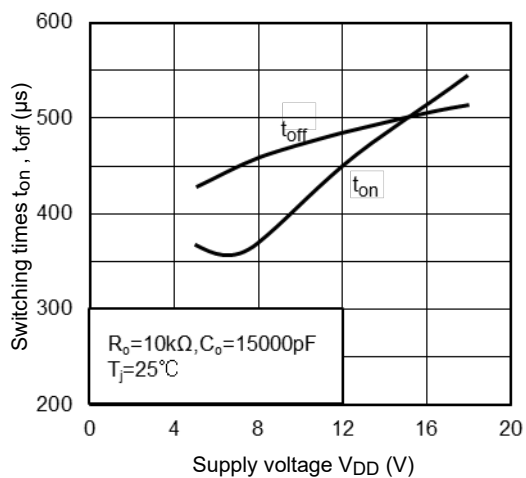


Figure 13.24 t_{on} , $t_{off} - V_{DD}$

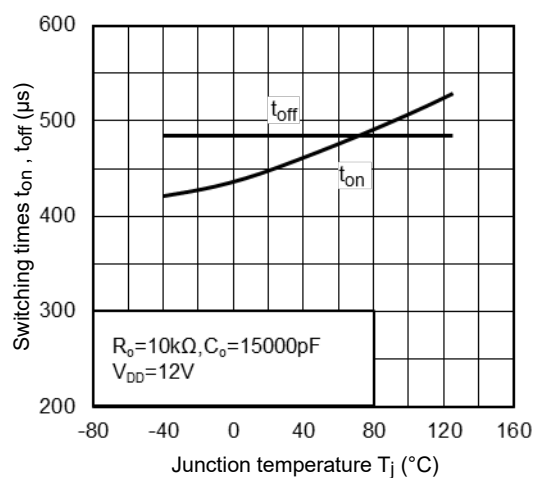


Figure 13.25 t_{on} , $t_{off} - T_j$

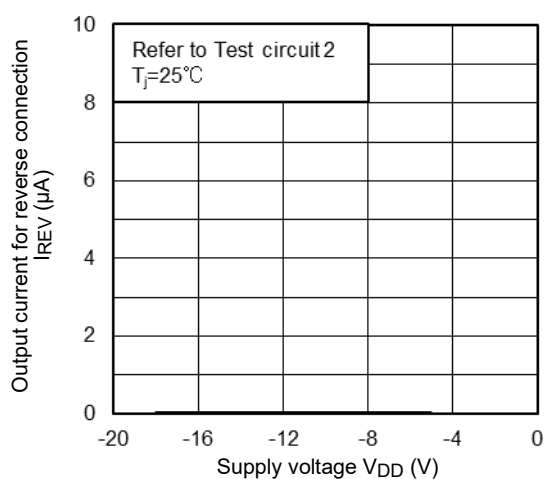


Figure 13.26 $I_{REV(1)} - V_{DD}$

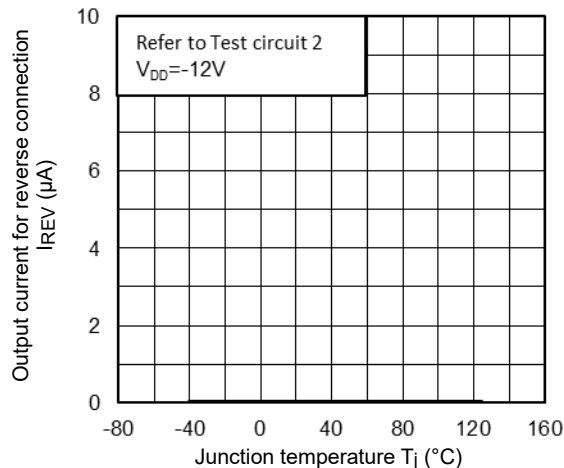


Figure 13.27 $I_{REV(2)} - T_j$

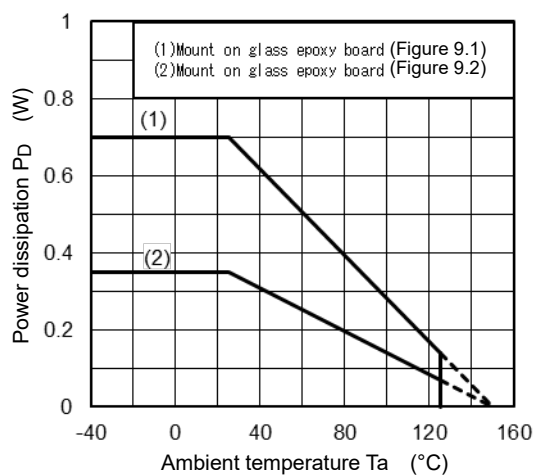
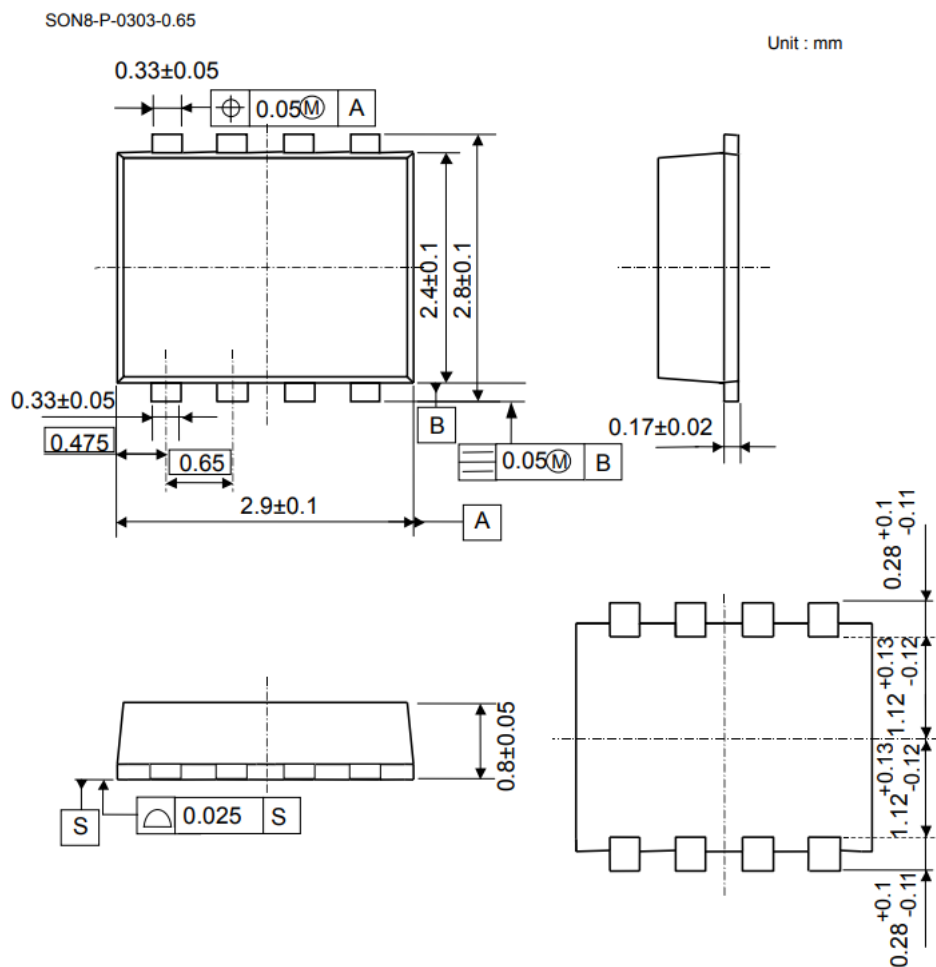


Figure 13.28 $P_D - T_a$

14. Package Information

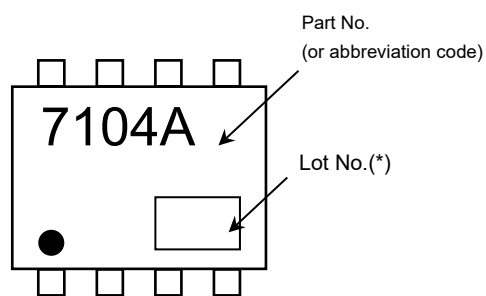
14.1. Package Dimensions



Weight: 0.017 g (Typ.)

Figure 14.1 Package Dimensions

14.2. Marking



Note: • on the lower left of the marking indicates Pin 1

*Weekly code: (Three digits)



Week of manufacture

(01 for first week of year; continuing up to 52 or 53)

Year of manufacture

(The last digit of the calendar year)

Figure 14.2 Marking

14.3. Land Pattern Dimensions for Reference only

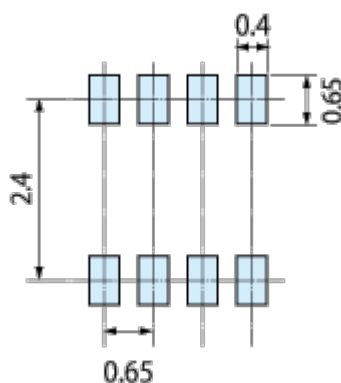


Figure 14.3 Land Pattern Dimensions for Reference only

15. IC Usage Considerations

15.1. Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
- (2) Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/ "Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.)

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