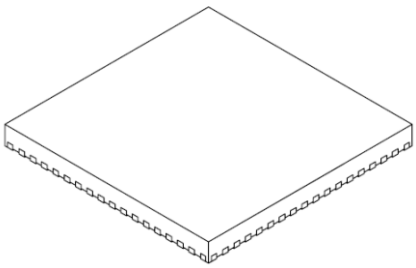
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC7734FTG

Power Management System IC

1. DESCRIPTION

TC7734FTG is a complete power supply solution for portable devices that include 4 DCDC Buck Converters, 3 LDOs, 2-ch LED Driver and built-in Switching Charger function. Most of the outputs can be controlled by I^2C bus for various programmable settings.



P-VQFN64-0909-0.50-001

Weight: 0.192 g (typ.)

2. FEATURES

- Operating voltage: 3.4 V to 5.5 V
- 4 ch DCDC converter (DCDC1 to DCDC4)
  - Synchronous Current Mode Buck Converters
  - DCDC1-4 Optional 2-Phase Switching Reduces Input Peak Current
  - Built-in compensation circuit: DCDC1 to DCDC4
- 3 ch LDO(LDO1 to LDO3)
- LED Driver
  - Built-in Current Mode DCDC Boost Converter
  - 2-Ch Constant Current LED Driver
  - Sink Current: up to 80 mA/ch with LED voltage up to 20 V
  - Output Current Accuracy: +/- 5% (ILED = 20 mA)
  - LED1 and LED2 Regulation Voltage: 0.4 V
  - PWM dimming, I^2C Controlled 32 steps with 195Hz fixed dimming frequency
  - LED Driver Protection Circuit
    - ➢ Over Voltage Detection (OVD)
    - ➢ Output Open Detection (OOD)
    - ➢ Output Short Detection (OSD)
- Battery Charger Function
  - USB Host and USB Charger Adaptor Detections for Optimum Charge Current for SDP, CDP, DCP and Other)
  - DCIN Input Over Voltage Protection (OVP): 5.8 V (typ.) * Maximum voltage of DCIN terminal is defined by 6 V.
  - Power Path Function
  - 1.5 A Switching Charger with Built-in Power MOSFETs

Output Descriptions:

Output	Adj Vout (V)	Step (V)	Default (V)	Default Options (V) [1]	Iout (A)	Control
DCDC1	0.9 - 1.4	50m	1.0	0.9 - 1.4 V@50 mV	1500 mA	I^2C
DCDC2	1.05 - 1.95	150m	1.35	1.05 - 1.95 V@150 mV	1000 mA	I^2C
DCDC3	2.7 - 3.4	100m	3.3	2.7 – 3.4 V@100 mV	800 mA	I^2C
DCDC4	1.5 - 3.3	-	(1.8)	R_ext	500 mA	R_ext
LDO1	1.2 – 1.9	-	1.8	1.2,1.3,1.4,1.5, 1.6, 1.7, 1.8, 1.9	300 mA	I^2C
LDO2	1.5 – 2.8	100m	2.8	1.5, 1.6, 1.7, 1.8, 2.3, 2.5, 2.8	350 mA	I^2C
LDO3	1.5 - 3.3	-	(1.8)	R_ext	120 mA	R_ext
Output	**Adj PWM**	**Iout**	**Vout (V)**	**Default Iout**	**fPWM (Hz)**	**Control**
LEDD	32 steps	80 mA x2	20	20 mA x 2	195	I^2C

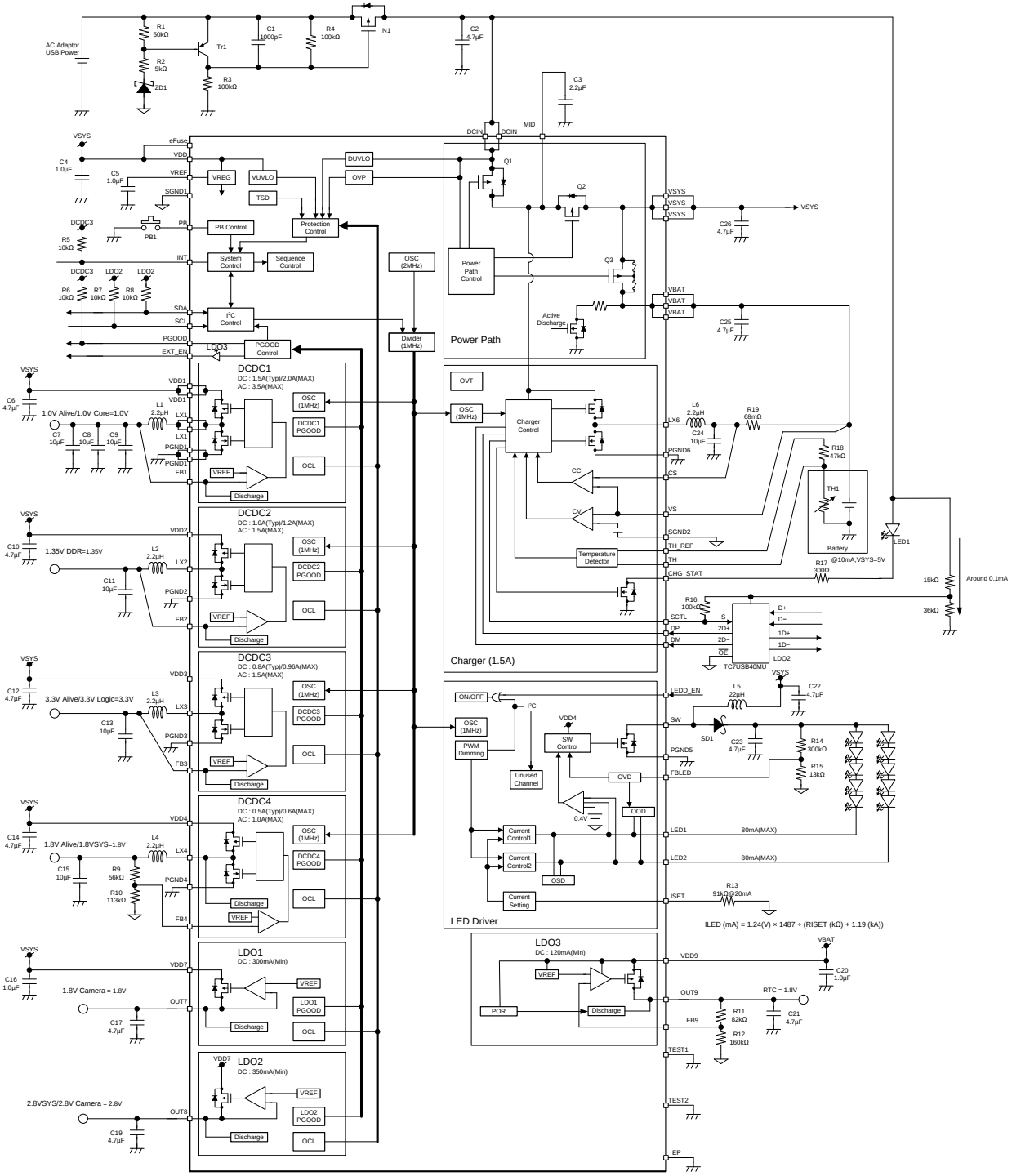
- I^2C Control for Various Parameters
- 1MHz Switching Frequencies DCDC1 to DCDC4
- 1MHz Switching Frequencies LED Driver, and Switching Charger
- PFM/PWM Operation for Wide Range of Load Current
- Built-in Soft start Circuit
- Programmable Power Sequence
- Interrupt for Event Notifications
- Power-good (PG) Notification
- DCDC and LDO Over Current Limit Circuits (OCL)
- Global Protection: Thermal Shutdown (TSD), VDD Under Voltage Lock Out (VUVLO), DCIN Under Voltage Lock Out (DUVLO)
- Register Password Protection
- Package: P-VQFN64-0909-0.50-001 9 mm × 9 mm × 0.7 mm (0.5 mm pin pitch)
- Application: Tablet PC, Portable Devices

Note 1: PFM does not apply to DCDC3

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3. Block Diagram, Application circuit

Figure: 1 Block Diagram and Application Circuit

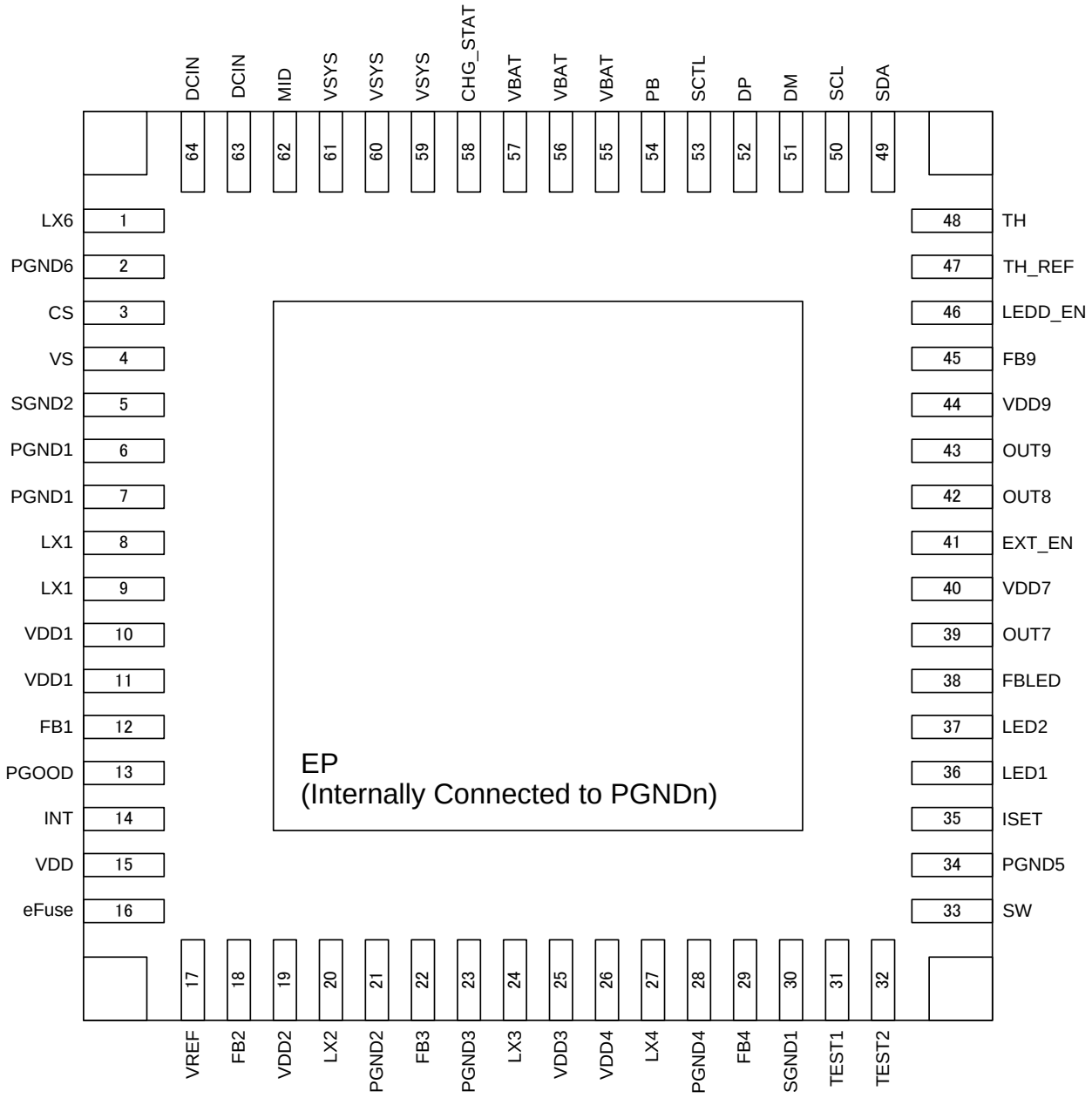


(Note)

- Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes. The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass-production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.
- GND wiring**:** We recommend that a heat sink be grounded at any parts, and the board and output pins be grounded at only one contact point. Take the heat dissipation into consideration when designing the board.
- Utmost care is necessary in the design of the each output lines, each VDD lines and each GND lines since IC may be destroyed due to short-circuit between outputs, to supply, or to ground.
- Especially for those pins that are connected to power supply and get a large current flow (such as each VDDs, Each LXs, VBAT, VSYS, MID, and each GNDs), they should be properly wired; otherwise troubles including destruction may occur to this IC.
- If the logic input pins (such as eFuse, VREF, TEST1, TEST2) are not wired properly, malfunction that would destroy the IC may occur due to a large current exceeding the absolute maximum ratings. Care should be taken in the design of board layouts and implementation of the IC.

4. Pin Layout (Top View)

Figure: 2 Pin Layout



5. Pin Description

Table: 1 Pin Description

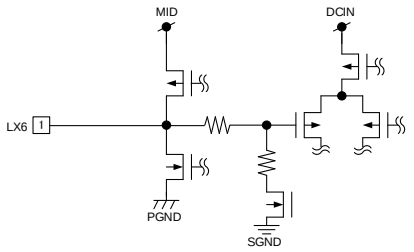
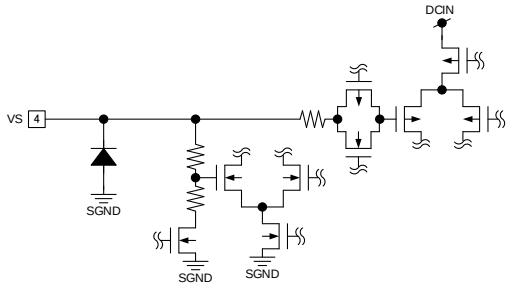
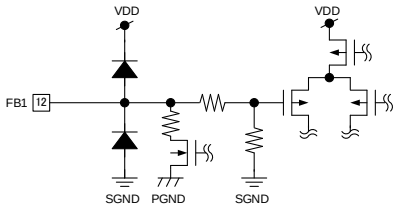
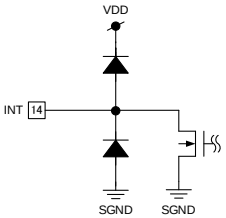
Pin No.	Name	I/O	Functions
1	LX6	O	Switching Output Terminal for Battery Charger
2	PGND6	P	Power GND Terminal for Battery charger
3	CS	I	Current sense(+) input Terminal
4	VS	I	Voltage sense input Terminal
5	SGND2	I	Signal GND Terminal for small signal
6	PGND1	P	Power GND Terminal for DCDC1
7	PGND1	P	Power GND Terminal for DCDC1
8	LX1	O	Switching Output Terminal for DCDC1
9	LX1	O	Switching Output Terminal for DCDC1
10	VDD1	P	VDD Terminal for DCDC1
11	VDD1	P	VDD Terminal for DCDC1
12	FB1	I	Feedback Terminal for DCDC1
13	PGOOD	O	Power-good signal output Terminal (Open-drain). Pulled low when any of the power rails are out of regulation. Behavior can be reset in register.
14	INT	O	Interrupt signal output Terminal, Open Drain, external R pull up needed.
15	VDD	P	VDD Terminal for IC internal bias
16	eFuse	I	TEST terminal for cutting eFuse This terminal should connect to VDD terminal.
17	VREF	O	Internal reference voltage output terminal
18	FB2	I	Feedback Terminal for DCDC2
19	VDD2	P	VDD Terminal for DCDC2
20	LX2	O	Switching Output Terminal for DCDC2
21	PGND2	P	Power GND Terminal for DCDC2
22	FB3	I	Feedback Terminal for DCDC3
23	PGND3	P	Power GND Terminal for DCDC3
24	LX3	O	Switching Output Terminal for DCDC3
25	VDD3	P	VDD Terminal for DCDC3
26	VDD4	P	VDD Terminal for DCDC4
27	LX4	O	Switching Output Terminal for DCDC4
28	PGND4	P	Power GND Terminal for DCDC4
29	FB4	I	Feedback Terminal for DCDC4
30	SGND1	S	Signal GND Terminal for small signal
31	TEST1	I	TEST terminal1. Cannot be used. Connect to SGND
32	TEST2	I/O	TEST terminal2. Cannot be used. No connect terminal
33	SW	O	LED Driver Switch terminal

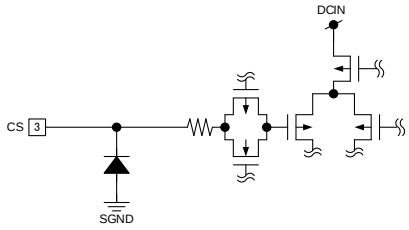
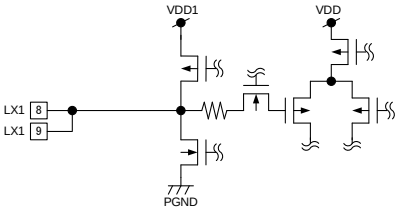
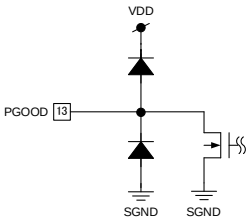
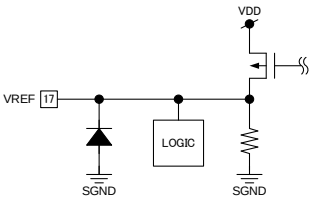
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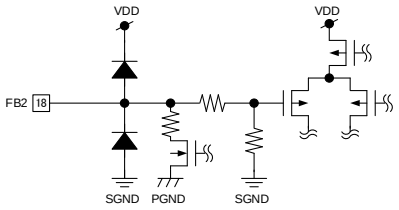
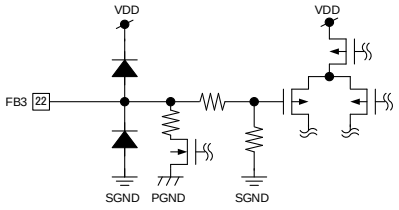
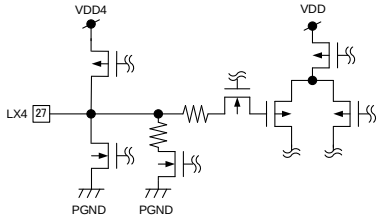
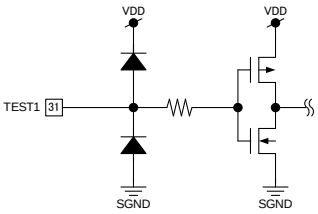
34	PGND5	P	Power GND Terminal for LED driver
35	ISET	O	LED current adjustment pin. Connect a resistor (RISET) to AGND
36	LED1	O	Channel 1 constant current sink terminal to drive LEDs
37	LED2	O	Channel 2 constant current sink terminal to drive LEDs
38	FBLED	I	Overvoltage threshold detect terminal for LED
39	OUT7	O	Output Terminal for LDO1
40	VDD7	P	VDD Terminal for LDO1 and LDO2
41	EXT_EN	O	Enable for external DCDC that power up sequence follows DCDC1 and turn off sequence follows DCDC2
42	OUT8	O	Output Terminal for LDO2
43	OUT9	O	Output Terminal for LDO3
44	VDD9	P	VDD Terminal for LDO3
45	FB9	I	Feedback Terminal for LDO3
46	LEDD_EN	I	LED Driver Enable Terminal
47	TH_REF	I	Battery thermistor sense input Terminal
48	TH	I	Battery thermistor input Terminal
49	SDA	I/O	I^2C-DATA Terminal
50	SCL	I	I^2C-CLK Terminal
51	DM	I/O	I/O pin(-) for USB power source detection
52	DP	I/O	I/O pin(+) for USB power source detection
53	SCTL	O	Open drain terminal for USB BUS control
54	PB	I	Push Button Switch Terminal with internal debounce circuit
55	VBAT	P	Battery+ Terminal
56	VBAT	P	Battery+ Terminal
57	VBAT	P	Battery+ Terminal
58	CHG_STAT	O	Open drain output terminal for charge status monitoring
59	VSYS	O	Output Terminal for System
60	VSYS	O	Output Terminal for System
61	VSYS	O	Output Terminal for System
62	MID	O	Power Path Charger Mid Point Connection. Place a 2.2 uF Cap. to PGND for proper operation Please take extra care while tracing the layout of the MID terminal to avoid shortage across GND. If such shortage occurs, IC may be permanently damaged.
63	DCIN	P	Power supply input Terminal. This terminal should connect power supply form AC adopter or USB power.
64	DCIN	P	Power supply input Terminal. This terminal should connect power supply form AC adopter or USB power.
EP	-	P	Power GND Terminal

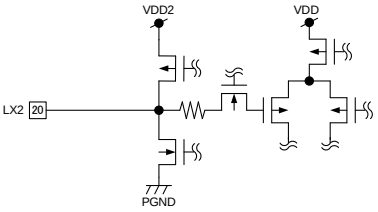
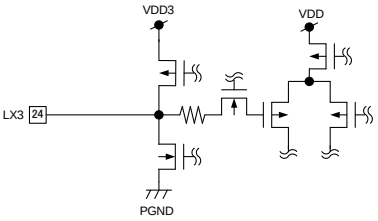
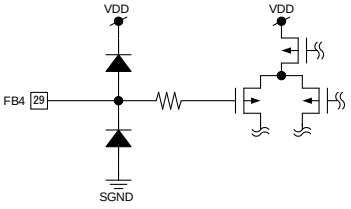
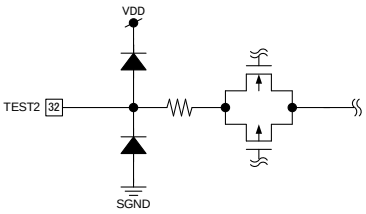
Notes: I=Input, O=Output, P=Power.

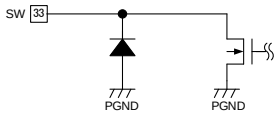
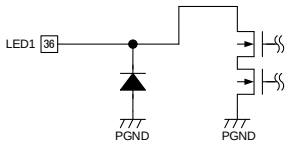
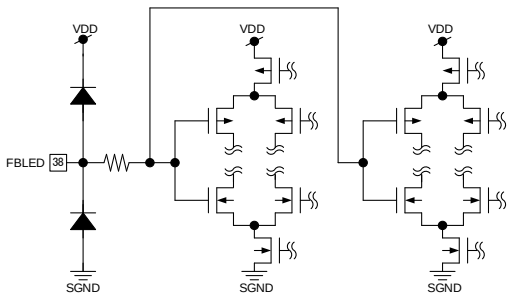
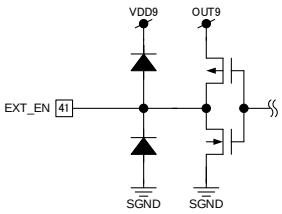
6. I/O Equivalent Pin Circuits

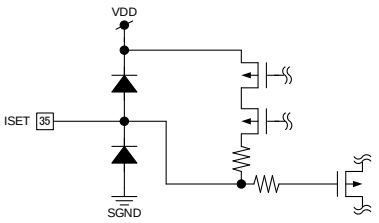
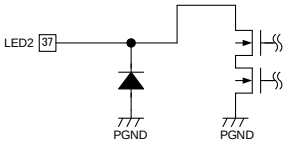
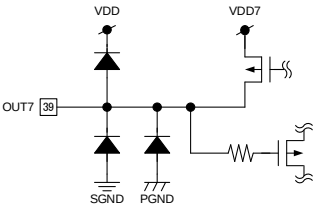
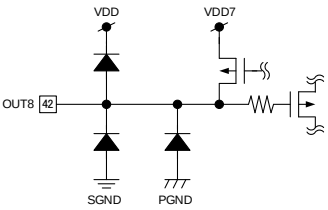
Terminal Name	Equivalent Circuit
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VS	
FB1	
INT	

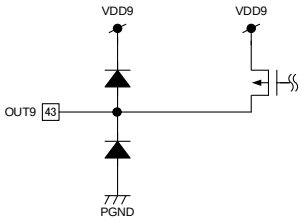
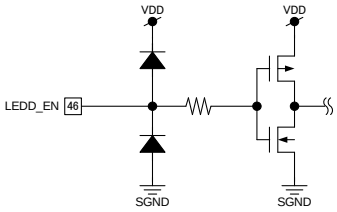
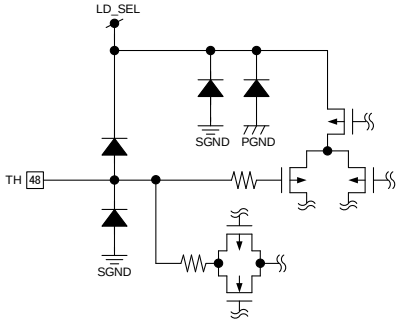
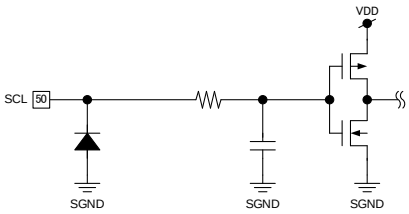
Terminal Name	Equivalent Circuit
CS	
LX1	
PGOOD	
VREF	

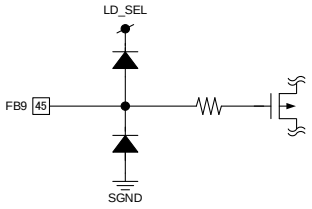
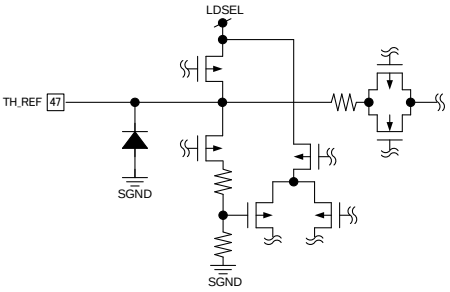
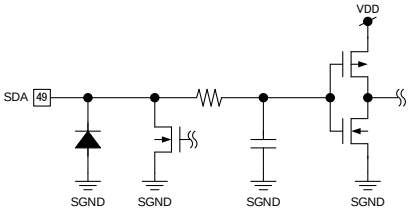
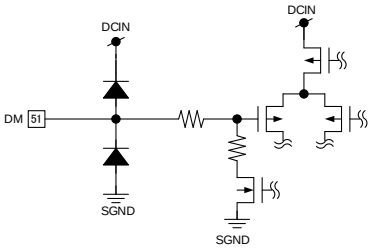
Terminal Name	Equivalent Circuit
FB2	
FB3	
LX4	
TEST1	

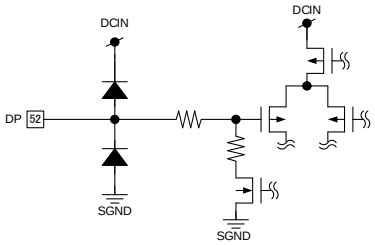
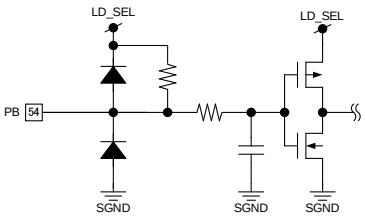
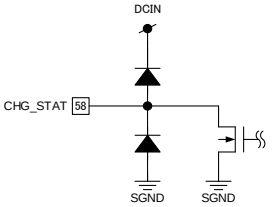
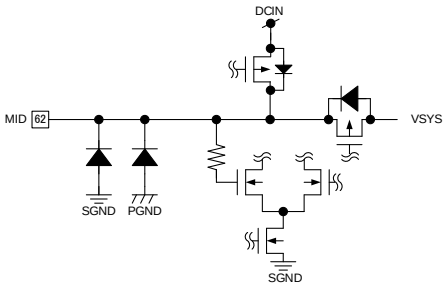
Terminal Name	Equivalent Circuit
LX2	
LX3	
FB4	
TEST2	

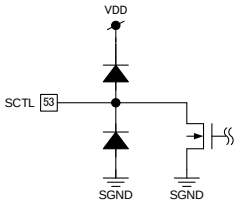
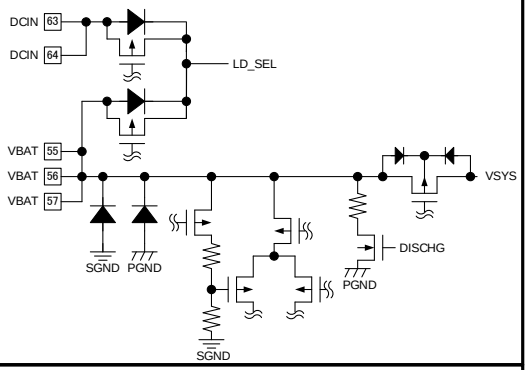
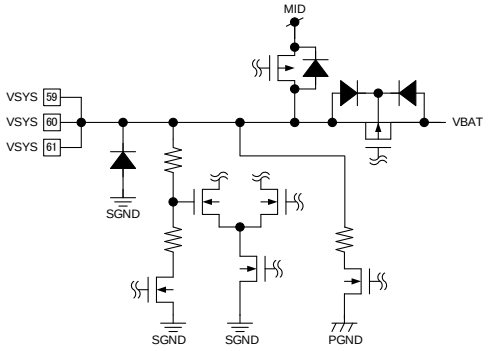
Terminal Name	Equivalent Circuit
SW	
LED1	
FBLED	
EXT_EN	

Terminal Name	Equivalent Circuit
ISET	
LED2	
OUT7	
OUT8	

Terminal Name	Equivalent Circuit
OUT9	
LEDD_EN	
TH	
SCL	

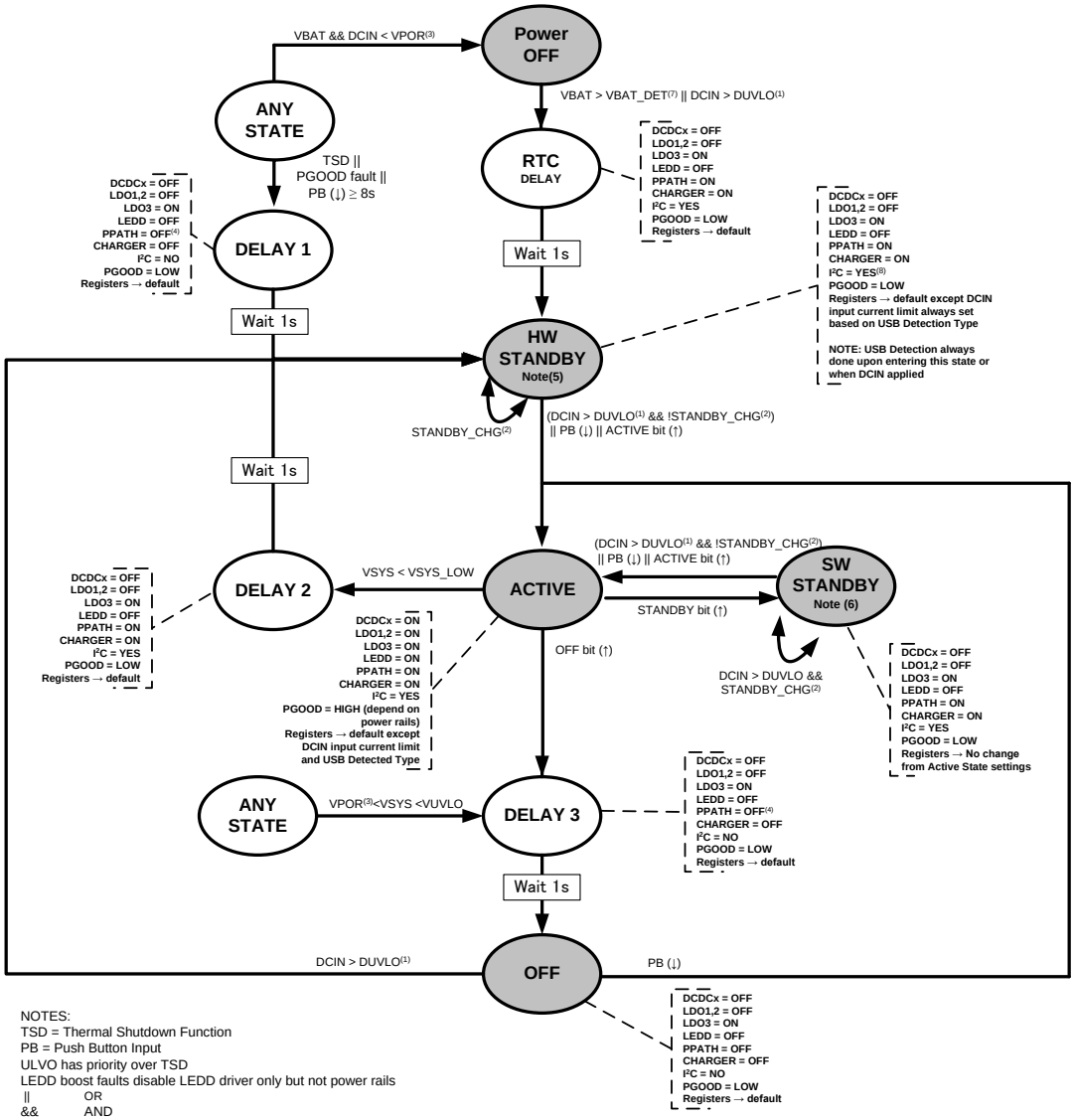
Terminal Name	Equivalent Circuit
FB9	
TH_REF	
SDA	
DM	

Terminal Name	Equivalent Circuit
DP	
PB	
CHG_STAT	
MID	

Terminal Name	Equivalent Circuit
SCTL	
VBAT DCIN	
VSYS	

7. State Diagram

Figure: 3 State diagram



NOTES:
TSD = Thermal Shutdown Function
PB = Push Button Input
ULVO has priority over TSD
LEDD boost faults disable LEDD driver only but not power rails

||	OR
&&	AND
PB (↓)	pushed bottom

Footnotes:
(1) At this event, PMIC shall detect USB type (DCP, SDP, CDP,Other), and set DCIN input current limit accordingly.
(2) STANDBY_CHG = (((Detect USB DCP || Detect Non-Compliant USB) && DCP_CHG_EN = '1') || (Detect USB SDP && SDP_CHG_EN = '1' && VBAT < VSYS_LOW) || (Detect USB CDP && CDP_CHG_EN = '1' && VBAT < VSYS_LOW)).
(3) VPOR(Power On Reset) is defined by design. Target voltage: 2.4V
(4) Battery voltage always supplies the system by Q3 in P.19 (From VBAT to VSYS)
(5) HW STANDBY state: Always detect USB Type (DCP, SDP, CDP,Other) when state change from OFF state and RTC delay by "DCIN > DUVLO".
(6) SW STANDBY state: Only detect USB Type (DCP, SDP, CDP,Other) on "DCIN > DUVLO" timing.
(7) VBAT_DET is defined by design. Target voltage: 2.6V
(8) I²C cannot accept in beginning of ACTIVE state (around 40µs)

HW_STANDBY state change condition

	From DELAY1,2	from RTC DELAY, OFF
Move to ACTIVE	PB (↓) || ACTIVE bit (↑)	(DCIN (↑) (1) && !STANDBY_CHG(2)) || PB (↓) || ACTIVE bit (↑)
STANDBY_CHG (CDP or SDP)	(Detect USB SDP && SDP_CHG_EN = '1') || (Detect USB CDP && CDP_CHG_EN = '1').	(Detect USB SDP && SDP_CHG_EN = '1' && VBAT < VSYS_LOW) || (Detect USB CDP && CDP_CHG_EN = '1' && VBAT < VSYS_LOW)

8. DCDC converter and LDO Functions

8.1. Operation description

DCDC converter and LDO Functions are determined by the internal registers set by I^2C bus. ACTIVE mode can be full mode where all outputs are turned on or selective rails can be turned on. Value of the register can be changed by writing data to the register.

8.2. Voltage Supply Terminal (VDD)

VDD is a power supply for DCDCn converter / LDO and for internal control circuit of TC7734FTG. VDD operation range is 3.4V to 5.5V. It can be connected to VSYS for power.

8.3. DCDC Converter (DCDC1 to DCDC3) Default Options

They are synchronous DCDCn Buck Converter of PFM/PWM type. Switching frequency is fixed of 1MHz (typ.). Select of the default options of DCDC1-3 are set by fuse options. For different defaults needed, please contact to Toshiba.
DCDC1 default options are 0.9 - 1.4 V@50 mV and the default is 1.0 V
DCDC2 default options are 1.05 - 1.95 V@150 mV and the default is 1.35 V
DCDC3 default options are 2.7 – 3.4 V@100 mV and the default is 3.3 V

8.4. LDO1 and LDO2 Default Options

Select of the default options of LDO1,2 are set by fuse options. For different defaults needed, please contact Toshiba factory.
LDO1 default options are 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8, 1.9 V and the default is 1.8 V
LDO2 default options are 1.5, 1.6, 1.7, 1.8, 2.3, 2.5, 2.8 V and the default is 2.8 V

8.5. DCDC1-4 and LDO1-3 Power-Up Sequence and Turn-Off Sequence

Once the VBAT is asserted or the DCIN is asserted, VSYS is available with LDO3 is ON. In the active mode, DCDCn and LDOn converters power up with output voltage in the sequence as below.

Power-Up Sequence 1**:** DCDC1 -> EXT_EN -> DCDC2 -> DCDC4-> LDO2, DCDC3 -> LDO1
Power-Up Sequence 2**:** DCDC1 -> DCDC2 -> EXT_EN -> DCDC4-> LDO2, DCDC3 -> LDO1.
Turn-Off Sequence 1**:** LDO1 -> DCDC3, LDO2 -> DCDC4 -> DCDC2 -> EXT_EN -> DCDC1
Turn-Off Sequence 2**:** LDO1 -> DCDC3, LDO2 -> DCDC4 -> EXT_EN -> DCDC2 -> DCDC1

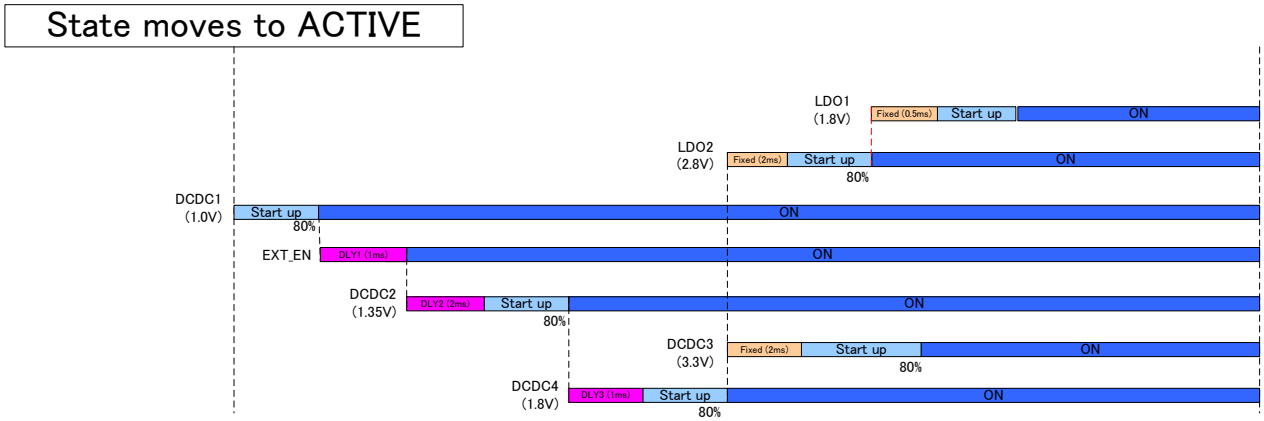
Power up/Turn off sequence can be controlled by register (0x07[D7]).
At the power up sequence, when the output voltage of a given rail reaches 80% (Typ.) of the set voltage, the following rail will start after adding setting delay time.
At the turn down sequence, when the output voltage of a given rail reaches 20% (Typ.) of the set voltage, the following rail will start after adding setting delay time.

All turn off sequences use active discharge mode. Refer to specification of resistance for active discharge.
Active discharge is always on at disable of each DCDCs and LDOs.
LDO3 is always ON. Only time LDO3 is OFF is in Power Down state.

Turn-Off Sequence is the reverse of power up sequence or same time (no delay). The Turn Off sequence is selected by register (0x07[D6]).

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Figure: 4 Power Up Sequence (0x07[D7]=0)



*Delay 1 to 3 Set by Register (0x06)

Figure: 5 Turn Off Sequence (0x07 [D6] =1)

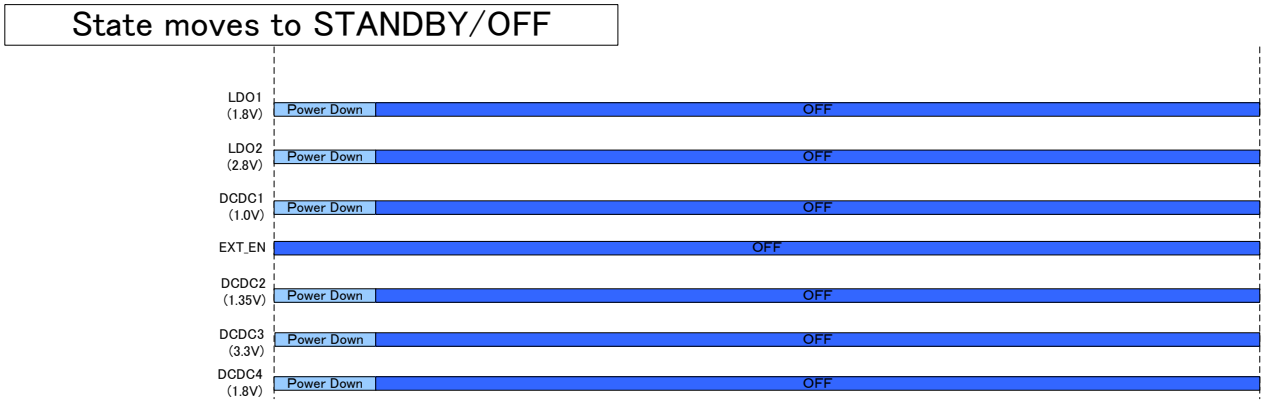
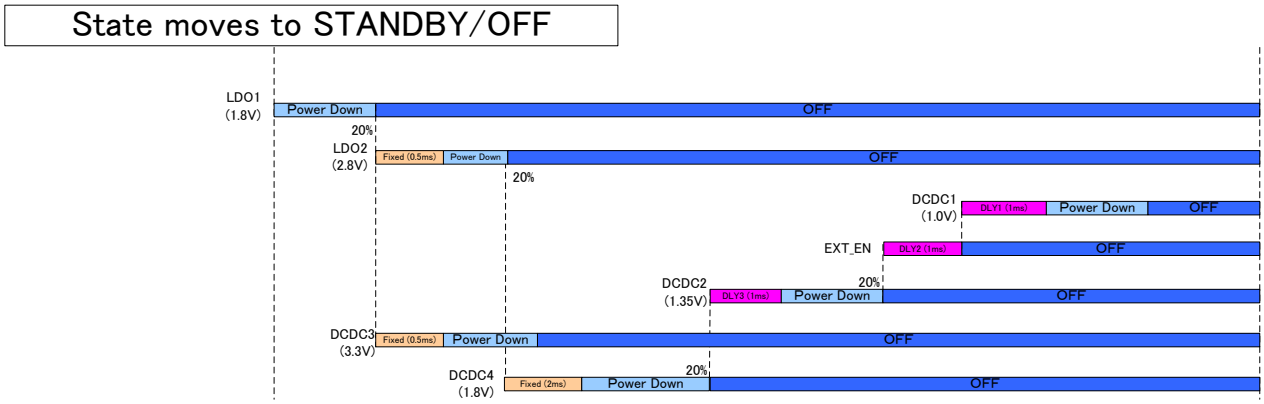
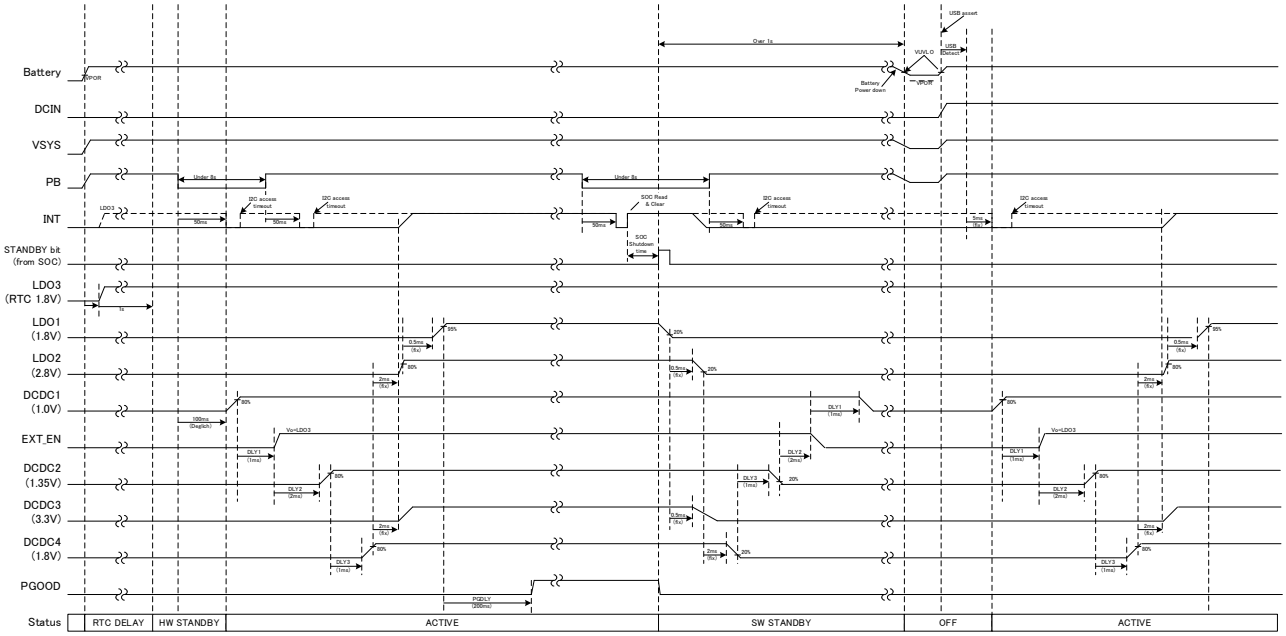


Figure: 6 Turn Off Sequence (0x07[D6]=0, 0x07[D7] =0)



*Delay 1 to 3 Set by Register (0x06)

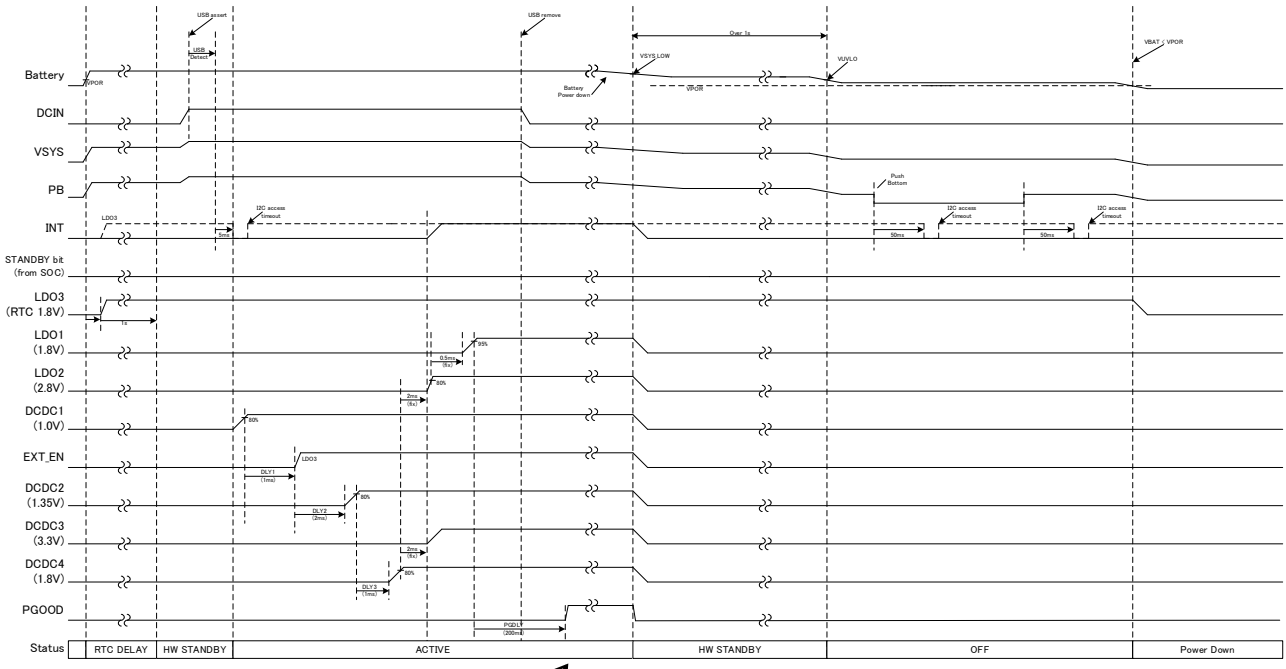
Figure: 7 Example 1: (VBAT assert -> PB -> PB -> VUVLO-> DCIN assert) 0x07[D7]=0



0x07[D6]=0

Figure: 8 Example 2 0x07[D7]=0

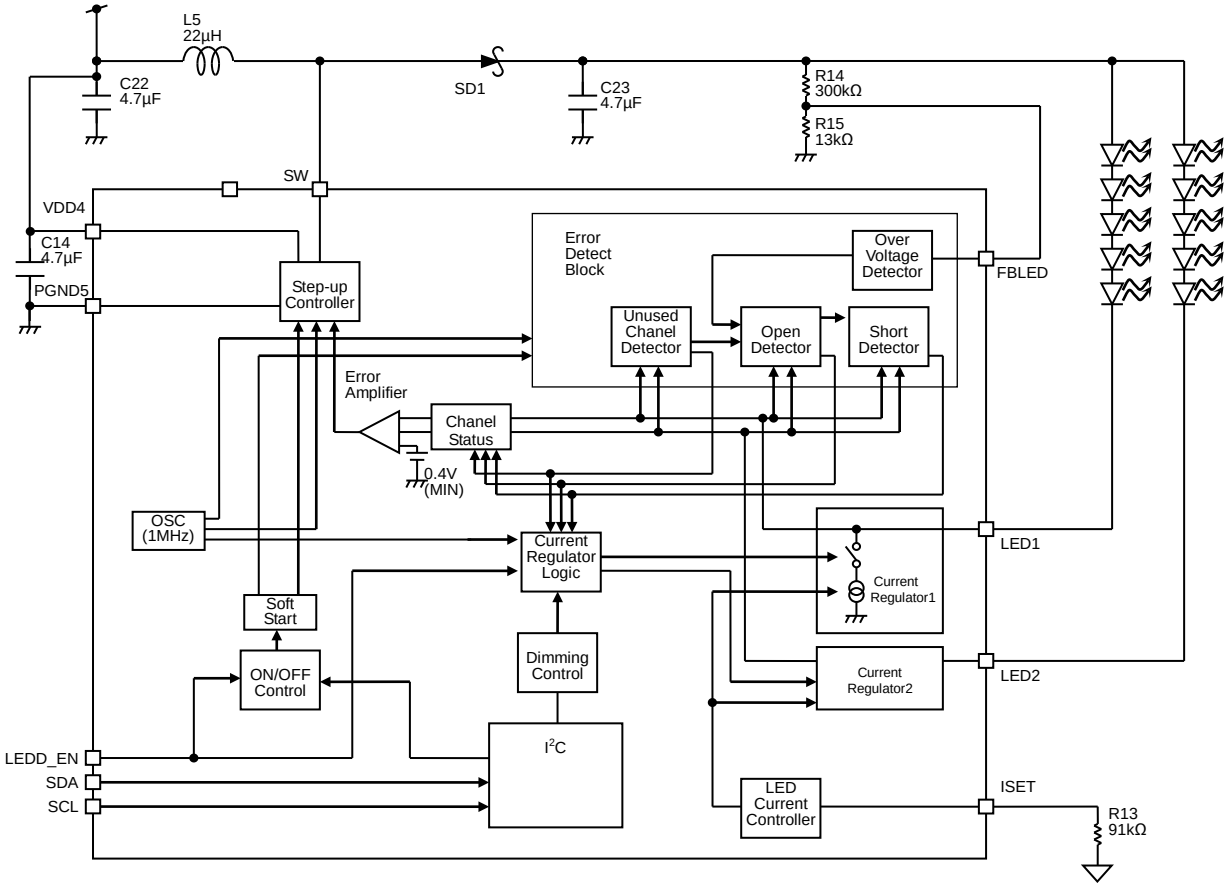
(VBAT assert -> DCIN assert -> DCIN removed -> SYS_LOW -> VUVLO-> PB -> VPOR)



0x07[D6]=1

9. LED Driver for LCD backlight Function

Figure: 9 LED Driver Block diagram



State of this function is transferred to the operation mode by LEDD setting register (0x08). DCDC controller and constant current regulators are controlled by inputting signal from LEDD_EN terminal or I^2C command (0x00[D7]).

TC7734FTG contains a boost converter and two current sinks capable of driving up to 2 LED strings at 80 mA. The numbers of LEDs per string can be up to 20 V. But need to care the SW current limit (1 A).
Power supply for step-up Controller is from VDD4. So, VDD4 must connect decoupling capacitance.

Unused OUT terminals are detected when the State moves to Active state. When unused LED terminals is detected, it is eliminated from object of control and its constant current operation is turned off.
Then, voltage boosting starts and the operation moves to the soft start. Soft start function is limited the SW terminal peak current. It is increased step by step.
The condition in which a soft start completes is constant current regulators (LED1, LED2) are generated by operation and the voltage of minimum LEDn terminal reaches about 0.4 V.
Brightness dimming is supported by I^2C control (0x08 [5**:**0]).
The PWM frequency is set to 195 Hz. The brightness dimming can be adjusted by 32 steps.

9.1. **LED Driver Operating Mode Chart**

Figure: 10 controlled by I²C command

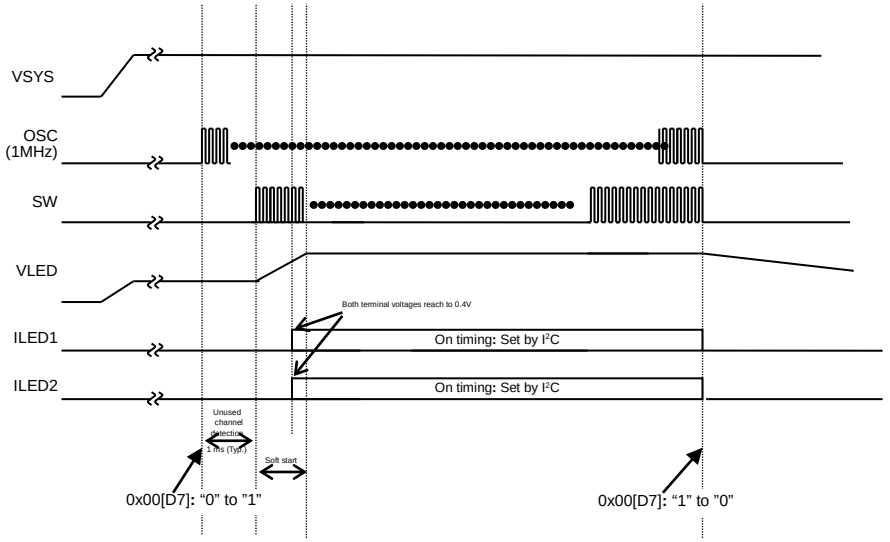


Figure: 11 LEDD_EN control

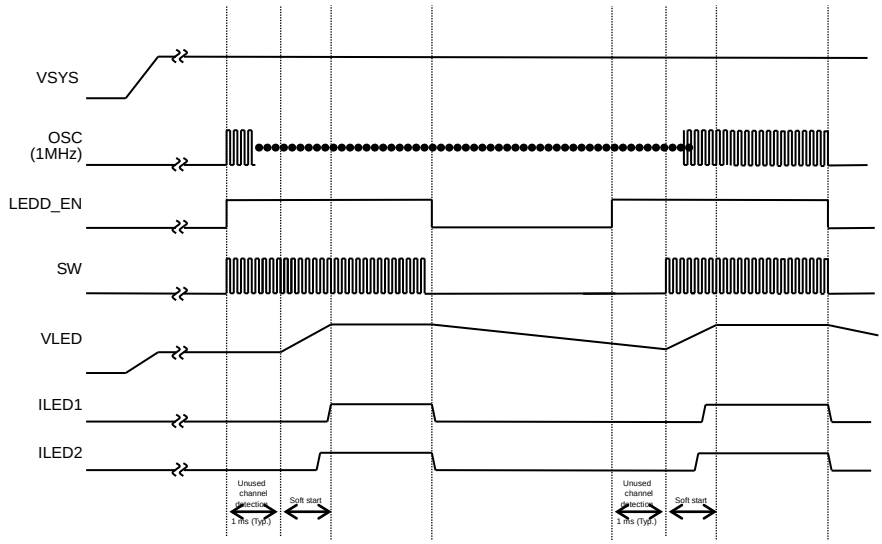
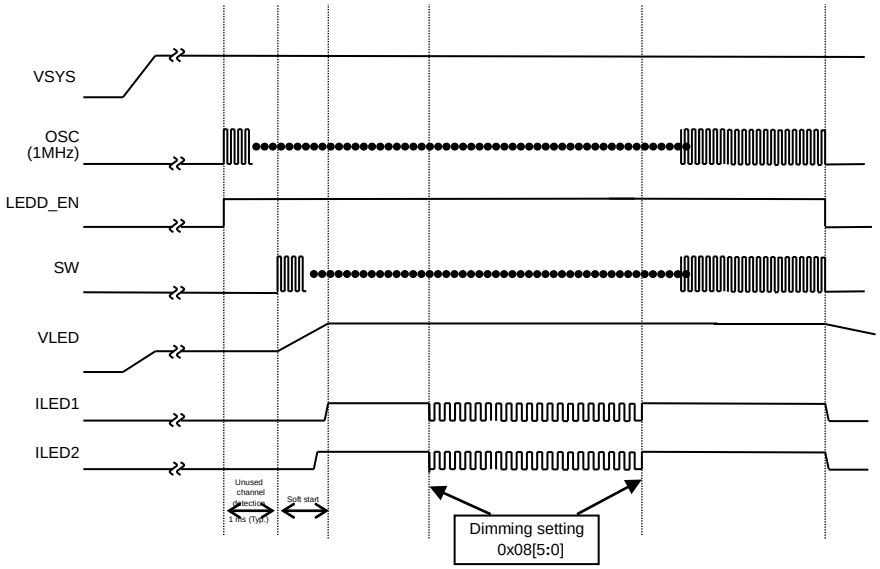


Figure: 12 LEDD_EN control and dimming control



9.2. Unused Channel Detection

When change the state of LED driver to active by LEDD_EN or I^2C, unused channel detection is operated before soft start. This function detects that the LEDn terminals (LED1 or LED2) is connected to PGND at the same voltage.
Connect the LEDn terminals of unused channel to PGND.
The constant current block of unused channel is turned off and removed from the object of LED open detection and LED short detection.

9.3. Dimming Control

Dimming function can operate by internal register setting. The PWM frequency is set to 195 Hz. The PWM duty cycle can be adjusted by 32 steps through the LEDDCTRL register (0x08[5:0]).

9.4. Constant Current Setting

Constant current (ILED) is set by RISET resistance connected between ISET terminal and GND.
ILED is provided by the equation 1 below.

$$ILED\ (mA) = 1.24(V) \times 1487 \div (RISET\ (k\Omega) + 1.19\ (kA))$$

9.5. **LED Driver Error Detection Function**

Refer to “Protection Functions” section in detail

Table: 2 Function of Detections

Detection	Function	Conditions for starting detection
OVD	SW (Switch) operation stops when the voltage of FB_LED rises to the detecting voltage or more. SW operation restarts when the voltage falls below the detecting voltage.	Always active
LED open	Operations of LEDn terminals, which are detecting voltage or less just after OVD detection, are turned off. They are eliminated from object of controlling the minimum LEDn terminal voltage. When all operations of LEDn terminal are turned off because of the abnormal state, all LED driver functions are turned off.	Just after OVD detection
LED short	Detection starts 6µs (typ.) after Dimming start timing, which are detecting voltage or more, are turned off. They are eliminated from object of controlling the minimum LEDn terminal voltage. When all operations of LEDn terminal are turned off because of the abnormal state, all LED driver functions are turned off.	From 6 µs (typ.) after Dimming start timing.

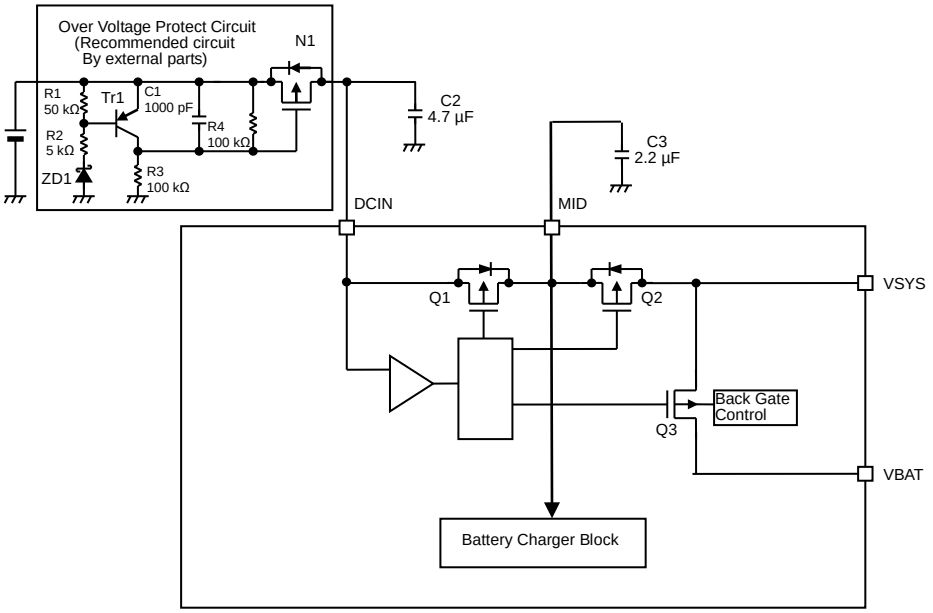
Table: 3 State of Each Block in Detection

Detection		Conditions	LED Driver Block		Method of re-startup
			Step-up control	Constant current	
OVD		VOVD > 1.228 V (Typ.) @ VFB_LED rising	Stop	Continue	The voltage is OVD recovery voltage or less.
LED Open	LED1 or LED2	VLEDn < 0.2 V (Typ.)	Active	Only error terminal: Stop	Re-started the LED driver
	LED1 and LED2		Stop	Stop	Re-started the LED driver
LED Short	LED1 or LED2	VLEDn > 5 V (Typ.)	Active	Only error terminal: Stop	When short error is released, it is resumed at the next dimming cycle
	LED1 and LED2		Stop	Stop	

10. Power Path Function

Power path function consists of Q1, Q2 and Q3

Figure: 13 Power path block diagram



Q1**:** 1) Detect current from DCIN. If this current reaches over-current condition, IC reduces the supply current to the charger block. If need to reduce further, IC conducted the current limit to VSYS by Q2.
2) Block the backflow current from VBAT to DCIN.

Q2**:** 1) Current limit to VSYS when it requires the over current.
2) Block the voltage to VSYS when DCIN voltage is over 5.8 V.

Q3**:** 1) Voltage supplies from VBAT to VSYS when no DCIN power source.
2) Stop the voltage supply from VBAT to VSYS when discharge mode is OFF or the current is over the limit of VBAT to VSYS.
3) Supplement current from VBAT to VSYS when the load demands higher current than the DCIN can support

The power path allows simultaneous and independent charging of the battery and powering of the system. This feature enables the system to run with a defective or absent battery pack and allows instant system turn-on even with a totally discharged battery. Charging current is automatically reduced when system load increases and if the system load exceeds the maximum current of the DCIN supply.

A block diagram of the power path is shown in Figure**:** 13 and an example of the power path management function is shown in Figure**:** 14 and Figure**:** 15.

10.1. Dead Battery (DUVLO > VBAT)

DCIN input is valid and the chip powers up if DCIN rises above 4.3 V. Note that the rise time of DCIN must be less than 50 ms for the detection circuits to operate properly. If the rise time is longer than 50 ms, the IC may fail to power up.

10.2. Good Battery (VBAT > DUVLO)

DCIN supply is detected when the input is 125 mV above the VBAT voltage and is considered absent when the voltage difference to the VBAT is less than 40 mV. This feature ensures that DCIN supply is used whenever possible to save battery life. DCIN input is current limited and controlled through the register (0x0D[D3**:**D0]).
In case DCIN is not present or blocked by the power path control logic (e.g. in OFF state), VBAT always supplies the system (VSYS pin).

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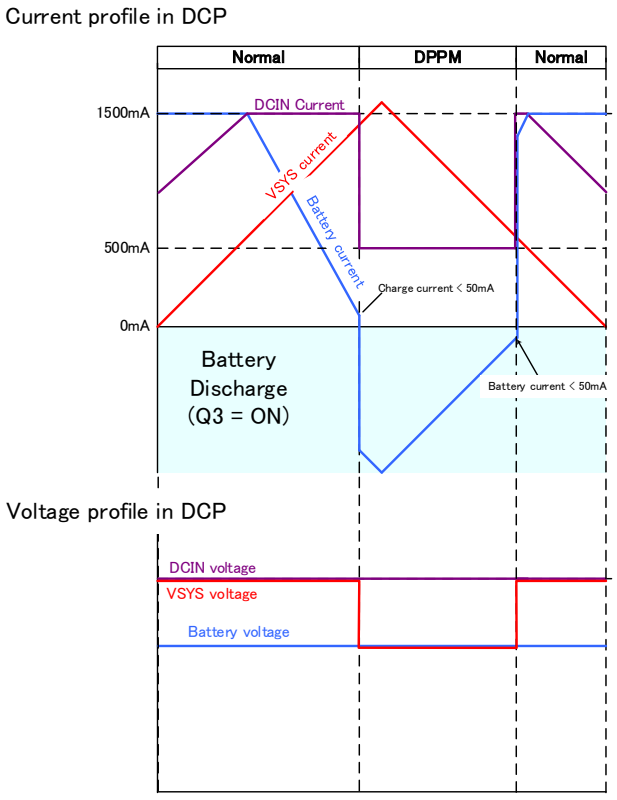
10.3. DCIN Input Discharge

DCIN inputs have 25 kΩ internal resistor which are used to discharge the input pins to avoid false detection of an input source.

Table: 4 DCIN Current limit setting and how to supply to VSYS

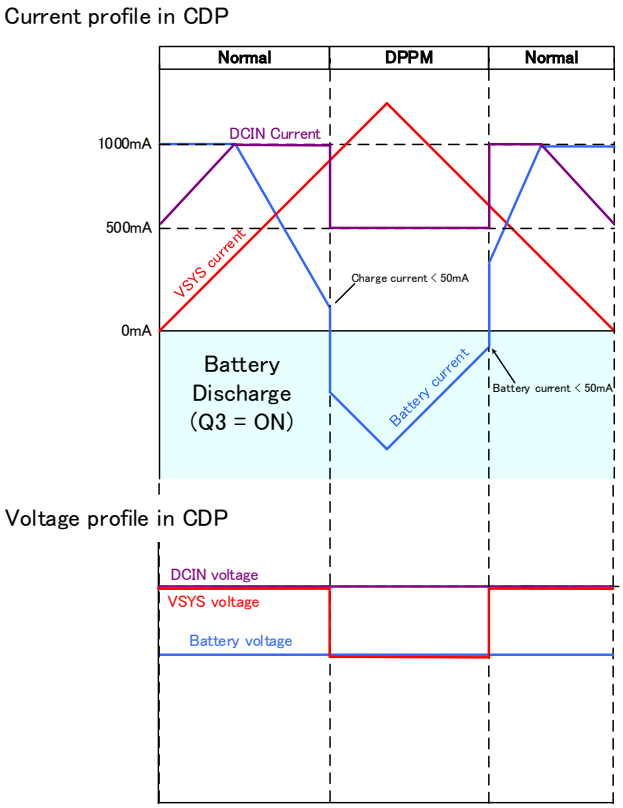
Mode / Current Limit	Normal (ISYS < DCIN Current limit)	DPPM (ISYS > DCIN Current limit)
1500 mA(DCP)	SYS power is supplied from DCIN	DCIN current save to 500 mA
1000 mA(CDP)	SYS power is supplied from DCIN	DCIN current save to 500 mA
500 mA(SDP)	SYS power is supplied from DCIN	DCIN current save to 500 mA

Figure: 14 Timing chart in DCP or Other (DCIN current limit = 1500 mA setting)



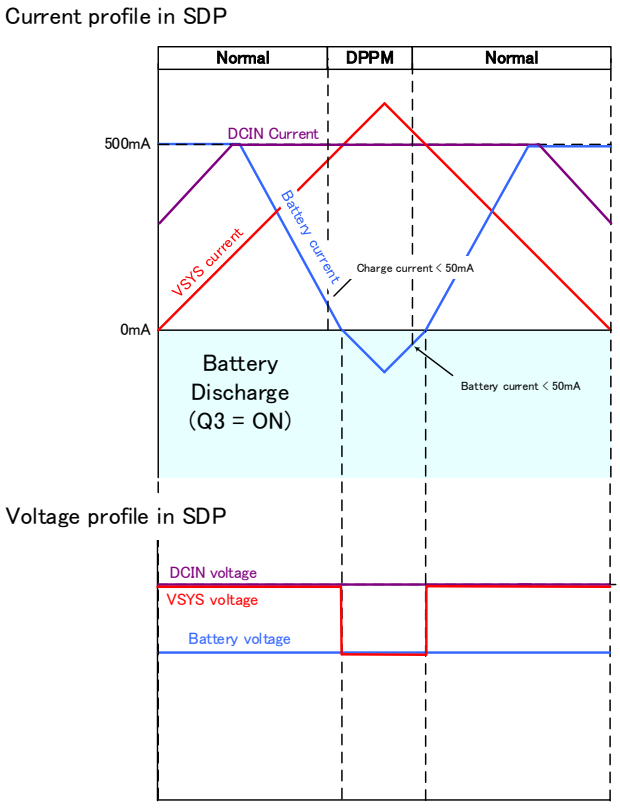
Actual current curve is depended on switching regulator's efficiency and input voltage such as DCIN, VBAT. So, this curve is reference.

Figure: 15 Timing chart in CDP (DCIN current limit = 1000 mA setting)



Actual current curve is depended on switching regulator's efficiency and input voltage such as DCIN, VBAT. So, this curve is reference.

Figure: 16 Timing chart in SDP (DCIN current limit = 500 mA setting)



Actual current curve is depended on switching regulator's efficiency and input voltage such as DCIN, VBAT. So, this curve is reference.

11. Charging Functions

11.1. Input Current Limit

Input current from DCIN pin can be limited to a set current automatically or I^2C. When input current exceeds the set current, the IC limits the current to the set current automatically. When DCIN voltage falls below the threshold set by I^2C, interrupting signal is generated by setting the current limit to USB100 level (Max 100 mA). To resume the current limit to the former level, interrupt must be deactivated.

Table: 5 Input Current Limit Command

Command	Register No.	Bit No.	Contents
USBILMT[3:0]	0x0D	D3-D0	DCIN input current limit
ATILMT	0x0B	D3	Limit of Automatic Input Current by DCIN voltage
INTATIL	0x20	D7	Limit of Automatic Input Current Interrupt

Table: 6 Apply Result of USB Automatic Detection(Default)

Result of source detection (DP / DM detection)	DCIN Input Current limit setting	Fast Charge Current limit (Typ.)
SDP	500 mA	500mA
CDP	1000 mA	Reg 0x0D [D5:D4]
DCP/AC	1,500 mA	Reg 0x0D [D7:D6]
Non-Compliance USB	1,500 mA	Reg 0x0D [D7:D6]

DCP: Dedicated Charging Port
SDP: Standard Downstream Port
CDP: Charging Downstream Port

11.2. CHG_STAT Function

CHG_STAT terminal drives current in charge state.

11.3. DCIN Over Voltage Protection Function(OVP)

It protects the IC from destruction caused by over voltage. Charger function is turned off when the voltage of DCIN pin reaches 5.8 V (typ.). To resume the operation, DCIN voltage needs to be below (5.65 V (typ.)) for reset.

11.4. Charging Operation

When DCIN pin is connected, following confirmations start for charge power up. When one of the following conditions is not met, the charge is interrupted.

(1) DCIN voltage ≥ DUVLO voltage, DCIN voltage ≤ OVP voltage
(2) DCIN voltage > Battery voltage + 125 mV
(3) Charge enable mode (Set by I^2C)
(4) Battery temperature is between high limit and low limit.

Table: 7 Charge Command

Command	Register No.	Bit No.	Contents
CHG_EN	0x02	D3	Control by I^2C

11.5. Trickle Charge

If Pre-charge state has no problem, charge starts at trickle charge (50% Pre-charge current) under the condition that battery voltage is 2.05 V or less.

11.6. Pre-charge

When battery voltage exceeds 2.05 V (typ.), Pre-charge starts with the charge current which is set by the register. Charge continues until the battery voltage reaches the fast charge threshold voltage set by the register. In case Pre-charge has not completed by Pre-charge timer finish, charge stops and informs the timer with interrupting error.

Table: 8 Pre-charge Command

Command	Register No.	Bit No.	Contents
PCI[1:0]	0x0A	D7,D6	Pre-charge Current and Trickle charge current
CCVTH[2:0]	0x09	D5-D3	Voltage Threshold from Pre-charge to Fast Charge

11.7. Fast Charge (Constant-Current Charge Mode)

When fast charge mode enabled, constant-current charge starts under the condition that the battery voltage exceeds the fast charge threshold voltage set by the register. Charge current is limited to the input limit current.

Table: 9 Fast Charge Command

Command	Register No.	Bit No.	Contents
CCI[3:0]	0x0A	D5-D2	Current of Fast Charge

11.8. Taper Charge (Constant-Voltage Charge Mode)

When the voltage becomes the float voltage set by the register in the fast charge mode, the operation moves to the Taper charge mode.

Table: 10 Constant-Voltage Charge Mode Command

Command	Register No.	Bit No.	Contents
FLTV[1:0]	0x09	D1,D0	Float voltage

11.9. Charge Completion

When charge completion is valid, charge is completed if the charge current decreases to the value set by the register. In case charge is not completed within the charge timer finish, charge stops and informs with the interrupt flag.
Important, in case Charge Completion function is invalid, interrupt flag is not output with CV charge despite of the charge current decreases to the value set by the register. Users should pay attention that an I^2C control is required to stop the charge.

Table: 11 Charge Completion Command

Command	Register No.	Bit No.	Contents
CT	0x0B	D0	Charge Termination
CEI[1:0]	0x0A	D1,D0	Charge completion current

11.10. Re-charge

Re-charge starts when the VBAT voltage falls at a voltage set by the register from the float voltage. However, the following two conditions that charge permission state is in DCIN and charge conditions are prepared before charge input state must be provided to re-start. Whether re-charge is automatic or not depends on the register.

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Table: 12 Re-charge Command

Command	Register No.	Bit No.	Contents
ATRCHGTH	0x0B	D7	Threshold for automatic Re-charge
ATRCHG	0x0B	D6	Automatic Re-charge function setting

11.11. **Safety Timer**

Safety timer has Pre-charge Safety Timer of 30 min (Default) and Charge Safety Timer of 480 min (Default). Timer of 30 min (Default) starts and trickle charge starts after Pre-charge is ready. And it is reset when the operation transferred from Pre-charge mode to fast-charge mode. Timer of 480 min (Default) also starts after Pre-charge is ready and stop when charge completion current does not reach the set value within timer on. Whether trickle charge is included or not at start both timers can be selected. Both timers function is defined as below.
When ISYS > DCIN current limit, battery charging will stop, safety timer will be paused, and the power path will draw current from the battery. When ISYS drops back below DCIN current limit, battery charging will resume and the timer will resume from last paused timer value. If the battery voltage drops below ATRCHGTH threshold during ISYS > DCIN current limit, the timer will be cleared and restarted when battery charging is resumed.

The above timer operation will occur in both Active and Standby states and transitions between these states.

Charge Safety Timer will be cleared and restarted with the following conditions**:**

DCIN insertion
Battery voltage drops below ATRCHGTH threshold
Charge Safety Timer is disabled and then enabled by I^2C(0x0C, D1)
Auto Re-charge is disabled and then enabled by I^2C (0x0B, D6)

Pre-charge Safety Timer will be cleared and restarted with the following conditions**:**

DCIN insertion
Charge restart
Pre-charge Safety Timer is disabled and then enabled by I^2C (0x0C, D2)
Auto Re-charge is disabled and then enabled by I^2C (0x0B, D6)

Table: 13 Safety Timer Command

Command	Register No.	Bit No.	Contents
PRCHGTMS	0x0C	D5	Pre-charge Safety Timer
CGTMS[1:0]	0x0C	D4,D3	Charge Safety Timer
TCSTON	0x0C	D0	Trickle Charge Safety Timer
CHGTMCLR	0x0C	D6	Clear of Pre-charge and Charge Safety Timer
PCGTM_EN	0x0C	D2	Pre-charge Safety Timer enable
CGTM_EN	0x0C	D1	Charge Safety Timer enable

Table: 14 Charge Error Function

Occurrence factor	Charger Circuit Action	Deactivate(Resume)
Input OVLO generation	Charge stop	Re-start from main standby mode depending on the improvement.
Input DUVLO generation	Charge stop	Re-start from main standby mode depending on the improvement.
DCIN<Vbat+125 mV	Charge stop	Re-start from main standby mode depending on the improvement.
Exceed chip temperature	Charge stop temporary	The operation resumes automatically depending on the improvement.
Battery OVLO generation	Charge stop	CHG_EN is turned on manually after improvement.
Unconnected battery	Charge stop	CHG_EN is turned on manually after improvement.
Charge Timer pass	Charge stop	CHG_EN is turned on manually.
Input voltage fall	Charge continues by limiting the current of 100 mA (ATILMT = 0)	Voltage rises to the former current limit level by resetting interrupt.

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Table: 15 Charge Completion Function

Occurrence factor	Charger Circuit Action	Deactivate(Resume)
Ichg < Iterm	Charge completion (0x0B[D0] = 0)	-

Table: 16 Interrupt Command

Command	Register No.	Contents
INT***	0x10, 0x20	Factor of interrupt
ST_***	0x21, 0x22, 0x23 0x24, 0x25, 0x26	Details of interrupting factor

11.12. Chip Temperature Monitor

Chip temperature is monitored during charge. When chip temperature exceeds T_{OVT}, chip temperature monitoring bit is set high (ST_OVT). When chip temperature falls below T_{OVT} - T_{OVT_HYS}, it is set low. Charger and Pre-charge Safety timers and Charge Safety timers stop when chip temperature monitoring bit is set high. Charger re-starts automatically when ST_OVT is set low again. Pre-charge Safety timer and Charge Safety timer resume at time before automatic stop. Timers are not reset.

Table: 17 Chip Temperature Monitor Command

Command	Register No.	Bit No.	Contents
ST_ OVT	0x22	D2	Status**:** Initial value depends on charger block temperature

11.13. Battery Temperature Monitor

Battery thermal detection uses thermistor integrated in battery. (Figure**:** 18 Thermal detector for battery block diagram)
Changing charge profile is set by register (HOTTEMP 0x0E [D2**:**D1], COLDTEMP 0x0E [D3])

Charge profile: Temperature range 0ºC to 60ºC (See Figure**:** 17 Battery Charger Profile**)**
(HOTTEMP 0x0E[D2**:**D1]=01, COLDTEMP (0x0E[D3]=0)
Under 0ºC **:** Stop the charging function
Under 10ºC **:** Fast charge current limit change under 500 mA in DCP and CDP detect.
Over 45ºC **:** Change the float voltage to 4.15 V
Over 50ºC **:** Change the float voltage to 4.10 V
Over 60ºC **:** Stop the charging function

When Change the register of HOTTEMP (0x0E[D2**:**D1]) and COLDTEMP (0x0E[D3]), Stopping charge point is changed.

Charge profile: Temperature range 10ºC to 45ºC
(HOTTEMP 0x0E[D2**:**D1]=00, COLDTEMP (0x0E[D3]=1)
Under 10ºC **:** Stop the charging function
Over 45ºC **:** Stop the charging function

Discharge profile: Temperature greater than 65ºC
If the following two conditions are satisfied**:**
1) Battery voltage is over 4 V
2) Temperature greater than 65ºC

The Battery is discharged using the Active discharge circuit until battery voltage is under 3.7 V. Active discharge current is defined by internal pull down resistor (45 Ω)

Discharge function is set by register (DISBAT 0x0E [D4])

Figure: 17 Battery Charger Profile

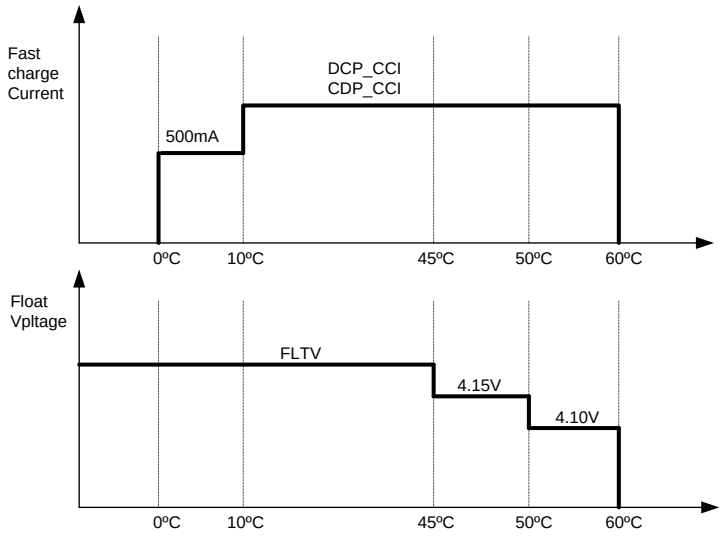


Figure: 18 Thermal detector for battery block diagram

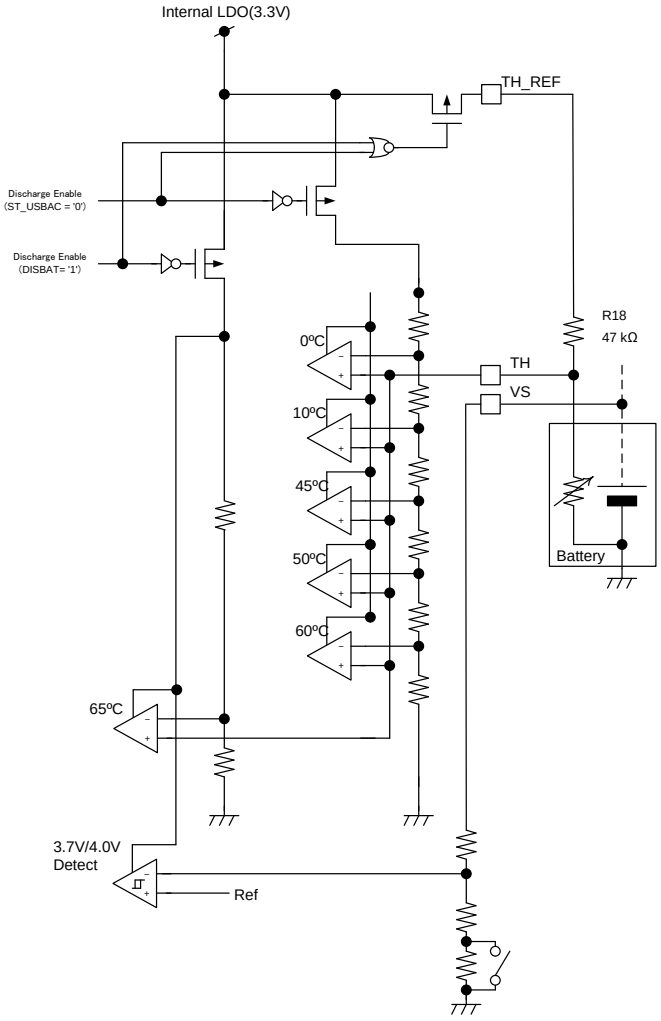


Figure: 19 Thermal detector for battery function 1

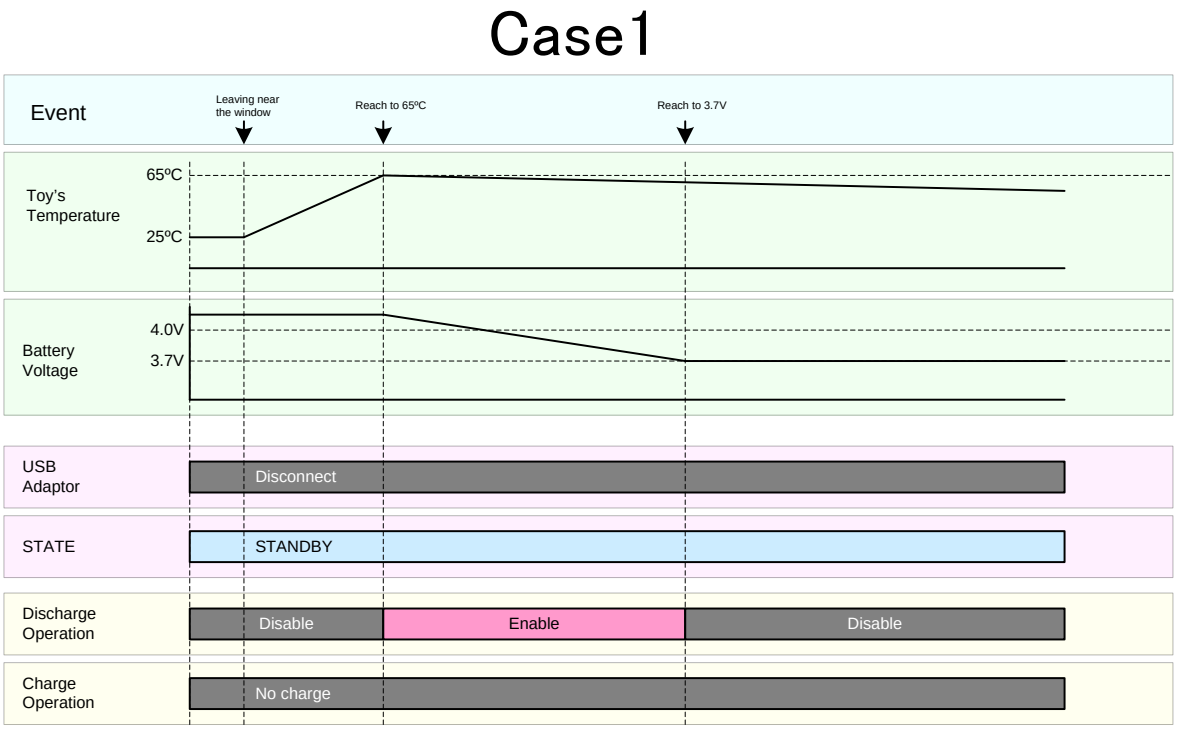
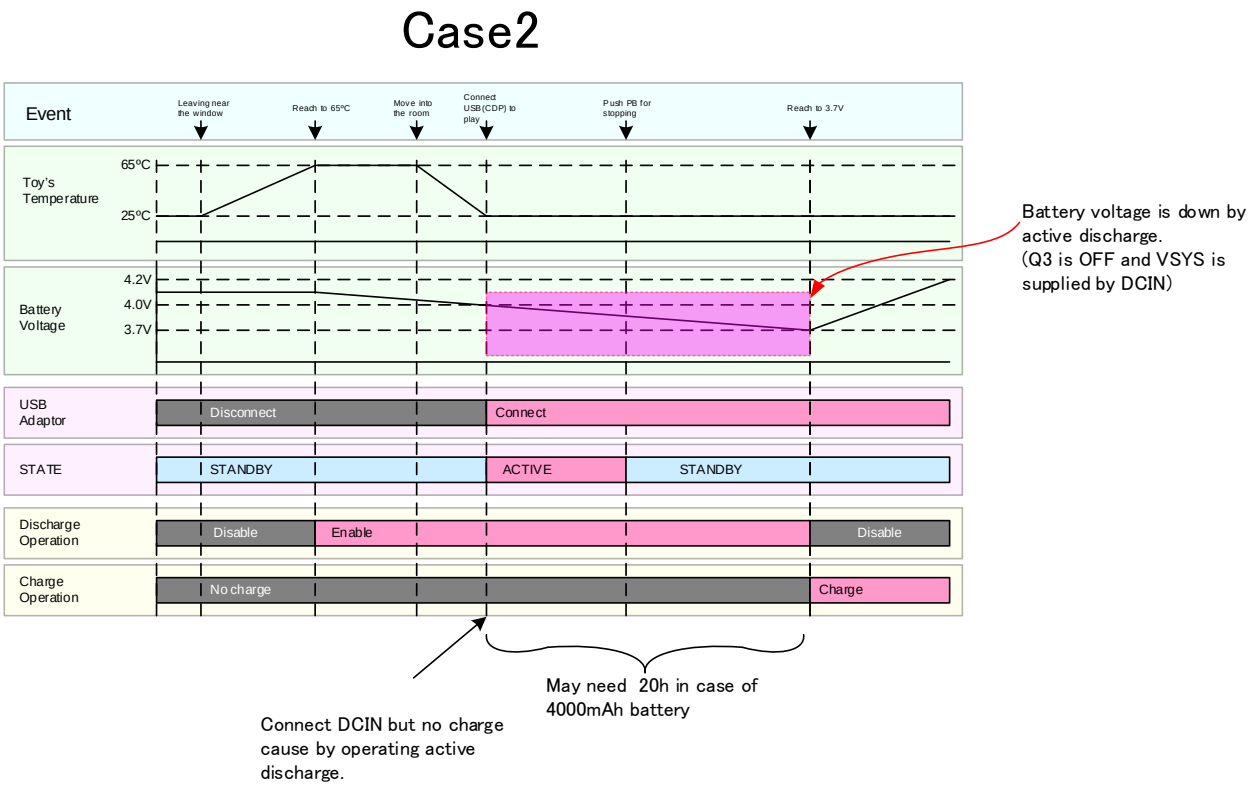


Figure: 20 Thermal detector for battery function 2



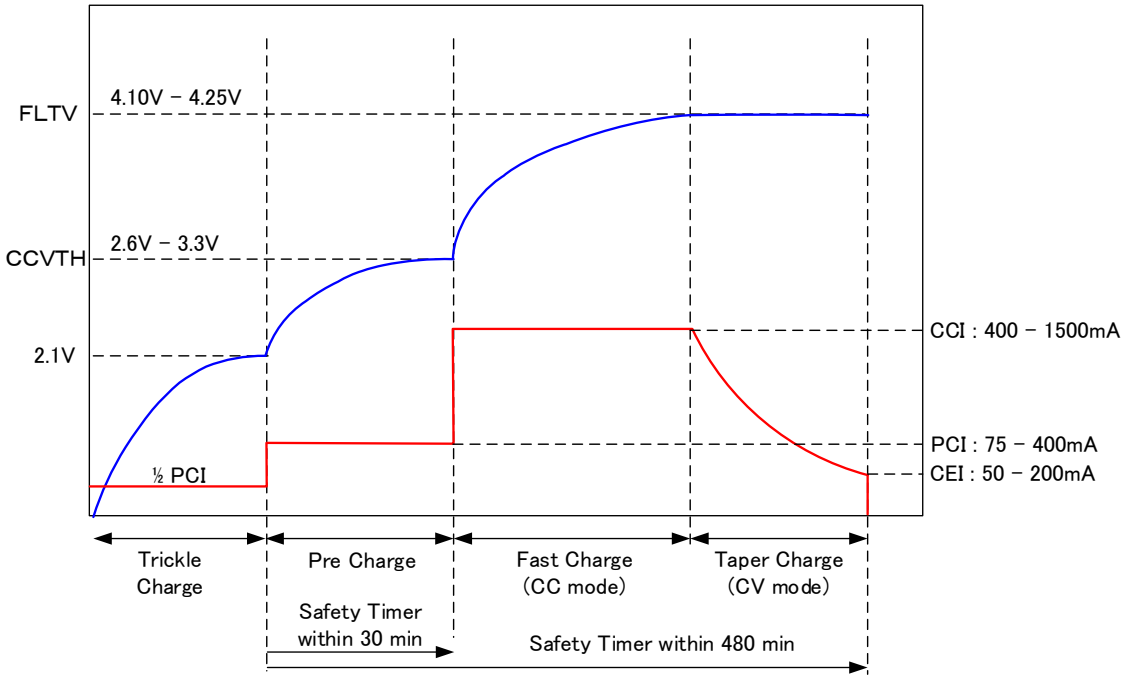
11.14. Power Source Detection

Automatic power source detection can be set by the register. Source detection starts as soon as DCIN is connected. Result of detection has four types as follows; non-connection, SDP (Standard Downstream Port), CDP (Charging Downstream Port), and DCP (Dedicated Charging Port). Input current limit can be set depending on the detection state.

Table: 18 Power Source Detection Command

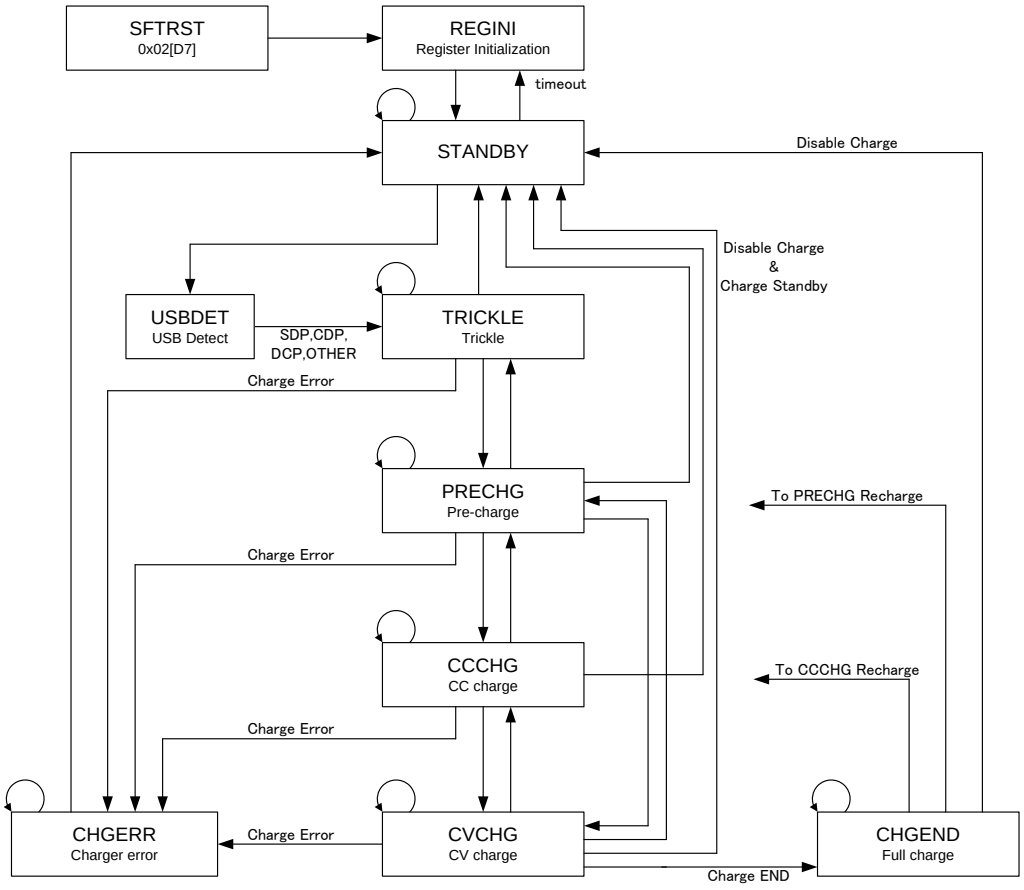
Command	Register No.	Bit No	Contents
ST_STYP<1:0>	0x21	D2,D1	Source detection result

Figure: 21 Battery Charge Profile



11.15. **Charge Mode Transition Diagram**

Figure: 22 Flow Chart of Charger Function



11.16. **USB detect diagram with TC7USB40MU**

Figure: 23 How to connect USB line using TC7USB40MU

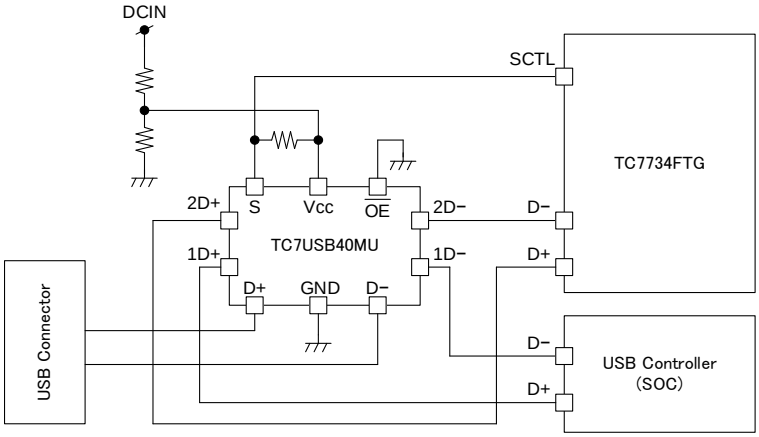


Figure: 24 Timing chart using TC7USB40MU

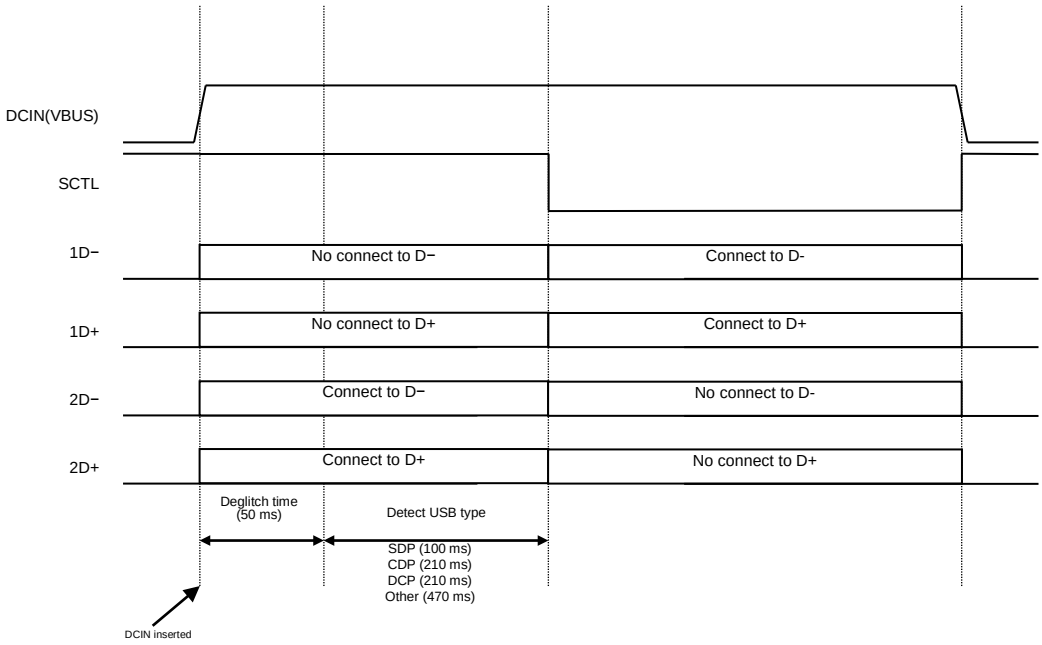


Figure: 25 Function timing chart detecting USB and charger current setting

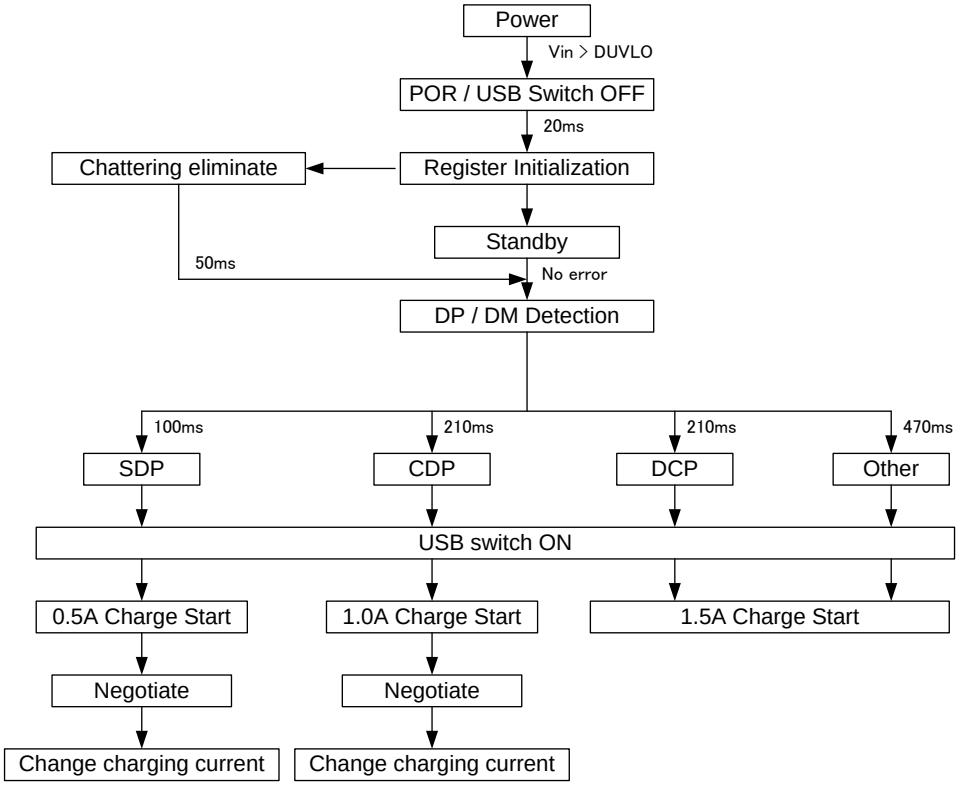
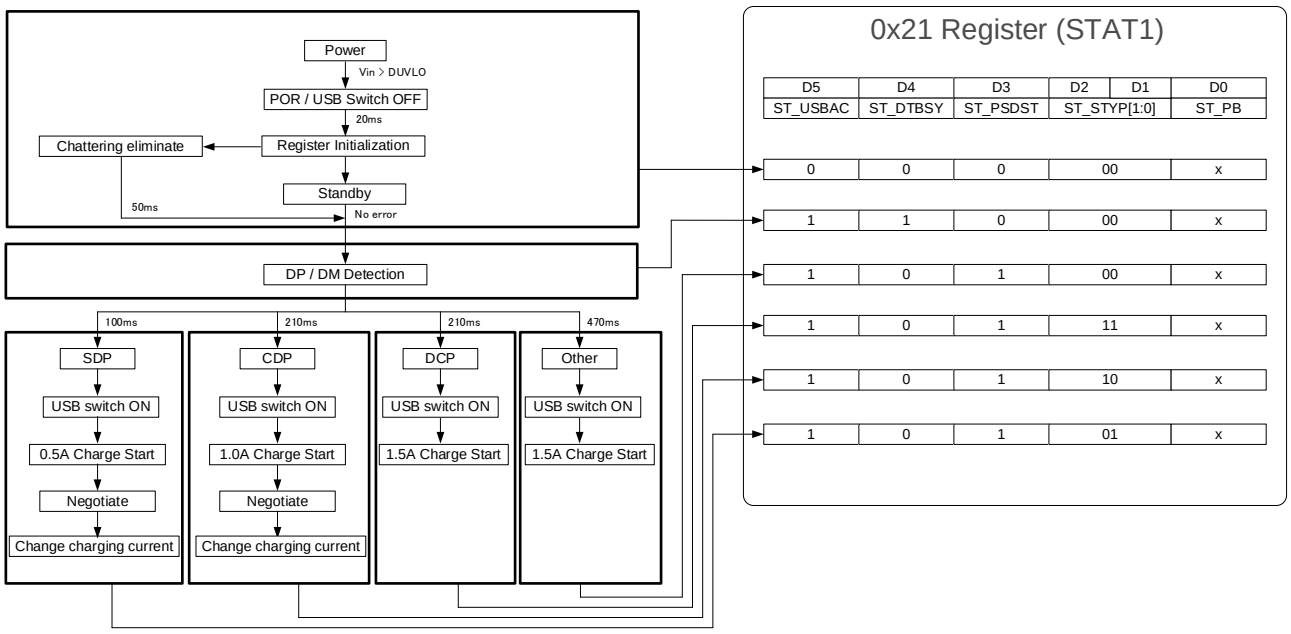


Figure: 26 Relation with Function timing chart detecting USB and 0x21 register



12. LOGIC Functions

12.1. Interrupt/Abnormal Detection

The INT pin is used to signal any event or fault condition to the host processor. Whenever a fault or event occurs in the IC the corresponding interrupt bit is set in the INT register (0x20), and the open-drain output is pulled low. The INT pin is released (returns to Hi-Z state) and fault bits are cleared when the interrupting INT register is read by the host. Reads of non-interrupting registers shall not clear the INT pin. If a fault persists after reading of INT register, the corresponding INT bit remains set and the INT pin is pulled low again after a maximum of 32 μs. Interrupt events include pushbutton pressed/released, DCIN voltage status change and others as specified in Interrupt/abnormal register section. The MASK bits in the INT register are used to mask events from generating interrupts that may be used for debugging purpose. The MASK settings affect the INT pin only and have no impact on protection and monitor circuits themselves. Note that persisting event conditions such as LED1 or LED2 enabled shutdown can cause the INT pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT register to see when the event condition has disappeared. Then unmask the interrupt bit again.

Interrupt Function

1. Automatic Input Current Limit
2. Re-charge
3. Charger Error
4. Charge Completion
5. System Error
6. Push Button
7. USB Detection
8. DCDCn, LDOn, LEDD Error

Table: 19 Interrupt Function Table1

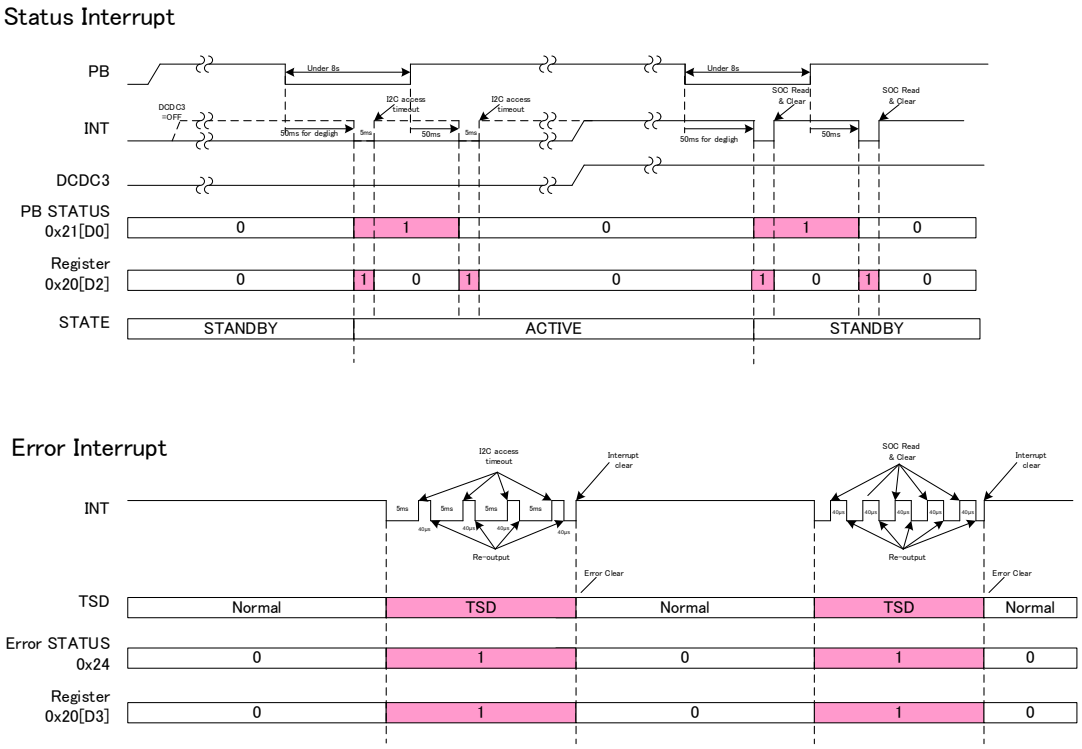
<table>
<tr><td>1</td><td>Automatic input current limit</td><td>Limit of Automatic Input Current Interrupt
<table><tr><td>0 (Default)</td><td>no change in status</td></tr><tr><td>1</td><td>Status changes (DCIN voltage falls below the threshold set by I²C[0x0B(D5,D4)])</td></tr></table>NOTE: To disable interrupt, set ATILMT(0x0B[D3]) register to “0”.</td></tr>
<tr><td>2</td><td>Re-charge</td><td>Re-Charge Status Change Interrupt
<table><tr><td>0 (Default)</td><td>Charge is completed or no change in charge status</td></tr><tr><td>1</td><td>Charge status changes by “Vbat < Vfloat – 150/300 mV” after charge completion</td></tr></table>NOTE: To disable interrupt, set ATRCHG(0x0B[D6]) register to “0”.</td></tr>
<tr><td>3</td><td>Charge Error</td><td>Charge Status Change Interrupt
<table><tr><td>0 (Default)</td><td>No charger error in status</td></tr><tr><td>1</td><td>Charger status error change</td></tr></table>NOTE: Status information is available in STATUS register 0x22.</td></tr>
<tr><td>4</td><td>Charge Completion</td><td>Charge Completion Status Change Interrupt
<table><tr><td>0 (Default)</td><td>No charge in charging status or not charging</td></tr><tr><td>1</td><td>Charge completion status changes when “Ichg < Iterm”</td></tr></table>NOTE: Status information is available in STATUS register 0x23.</td></tr>
<tr><td>5</td><td>System Error</td><td>System Status Change Interrupt
<table><tr><td>0 (Default)</td><td>no change error in status</td></tr><tr><td>1</td><td>System status error change</td></tr></table>NOTE: Status information is available in STATUS register 0x24.</td></tr>
<tr><td>6</td><td>Push Button</td><td>Pushbutton Status Change Interrupt
<table><tr><td>0 (Default)</td><td>No change in status</td></tr><tr><td>1</td><td>Pushbutton status change
(PB_IN changed high to low or low to high)</td></tr></table></td></tr>
</table>

		NOTE: Status information is available in STATUS register 0x21[D0].
7	USB Detection	USB Detection Interrupt 0 (Default): no change in status 1: DCIN power status detect (power to DCIN pin has either been applied or removed) NOTE: Status information is available in STATUS register 0x21[D5, D2,D1].
8	DCDCn , LDOn, and LEDD Error	DCDCn, LDOn and LEDD Status Change Interrupt 0 (Default): no change in status 1: DCDCn or LDOn or LEDD status error change NOTE: Status information is available in STATUS registers 0x25 and 0x26.

			Timeout (SOC does not read)	SOC Read
Error Interrupt	INTATIL	D7	INT: Clear Register: Not clear (0x20[D0,D3,D5,D7]) Status: Not clear (0x0B[D3],0x22,0x24,0x25,0x26) And if status error continues after INT cleared , Re-output INT output	INT: Clear Register: Not clear (0x20[D0,D3,D5,D7]) Status: Not clear (0x0B[D3],0x22,0x24,0x25,0x26) And if status error continues after INT cleared , Re-output INT output
	INTCHGER	D5		
	INTSYSFAULT	D3		
	INTPWFAULT	D0		
Status Interrupt	INTRCHG	D6	INT: Clear Register: Clear (0x20[D1,D2,D4,D6]) Status: Not change (0x21[D1,D2,D5])	INT: Clear Register: Clear (0x20[D1,D2,D4,D6]) Status: Not change (0x21[D1,D2,D5])
	INTCHGCMP	D4		
	INTPB	D2		
	INTUSBAC	D1		

Table: 20 Interrupt Function Table2

Figure: 27 Interrupt Function timing chart



12.2. **Password Protection**

This function prevents specific registers from accidental write access. Read access is not locked for the protected registers so host processor can read them anytime without unlock. But write access is locked by password, so host processor needs to unlock it by writing correct password data (0xAB) to the Password register. When the correct password data (0xAB) is written to Password register, the one I^2C transaction (Note1) is unlocked right after the I^2C transaction of password writing. The unlocked one transaction allows host processor to write to the protected registers. The host processor can write one or more the protected registers at once in the one unlocked transaction. After the one unlocked I^2C transaction, the write access to the protected registers is locked. Writing incorrect password data to password register is discarded.

Note1**:** One I^2C transaction is from I^2C start condition to stop condition, regardless of the access type (read/write).

The following registers are protected by this function.

- 0x03 DEFLDO12
- 0x04 DEFDCDC12
- 0x05 DEFDCDC34
- 0x06 SEQDLY1
- 0x07 SEQDLY2
- 0x0F STATE_CONF
- 0x14 PGMASK

12.3. **Power-good Function**

Power-good is a signal used to indicate if an output rail is in regulation or at fault. Internally, all Power-good signals of the enabled rails are monitored at all times and if any of the signals goes low, a fault is declared. All Power-good signals are internally deglitched. When a fault occurs, all output rails are powered down and the device enters STANDBY state. The following rules apply to the PGOOD output**:**

- The power up default state for Power-good is low. When all rails are disabled, PGOOD is low.
- Only enabled rails are monitored. Disabled rails are ignored.
- The user can set Power-good mask bits in the PG register (0x14) to define which rails affect the PGOOD pin.
- LEDD has no effect on the Power-good signal.
- Power-good monitoring of a particular rail starts 6ms after the rail has been enabled.
- PGOOD output is delayed by the PGDLY (PG register 0x0F[D1**:**D0]) after the sequencer is done.
- If an enabled rail goes down due to a fault (output shorted, TSD, VUVLO), PGOOD is declared low, and all rails are shut-down.
- If the user disables a rail, it has no effect on the PGOOD pin.
- If the user disables all rails, PGOOD is pulled low.

In normal operation PGOOD is high in active state but low in STANDBY and OFF state.

13. Protection Functions

13.1. VDD Under Voltage Lockout (VUVLO) Function

VUVLO circuit initializes (Defaults) each register and the state enters OFF state in case voltage of VDD drops by I^2C control (0x0F, STATE_CONF register). VUVLO function is deactivated by DCIN asserted or PB pressed and the operation recovers in accordance with each register setting.
VUVLO circuit monitors the VDD voltage. Need to connect directly between VSYS and VDD for detecting VSYS voltage.

13.2. Thermal Shutdown (TSD) Function

In the case that IC temperature exceeds 150°C (Typ.), after wait 1 second, moves to STANDBY state.

13.3. Over Current Limit (OCL) Function

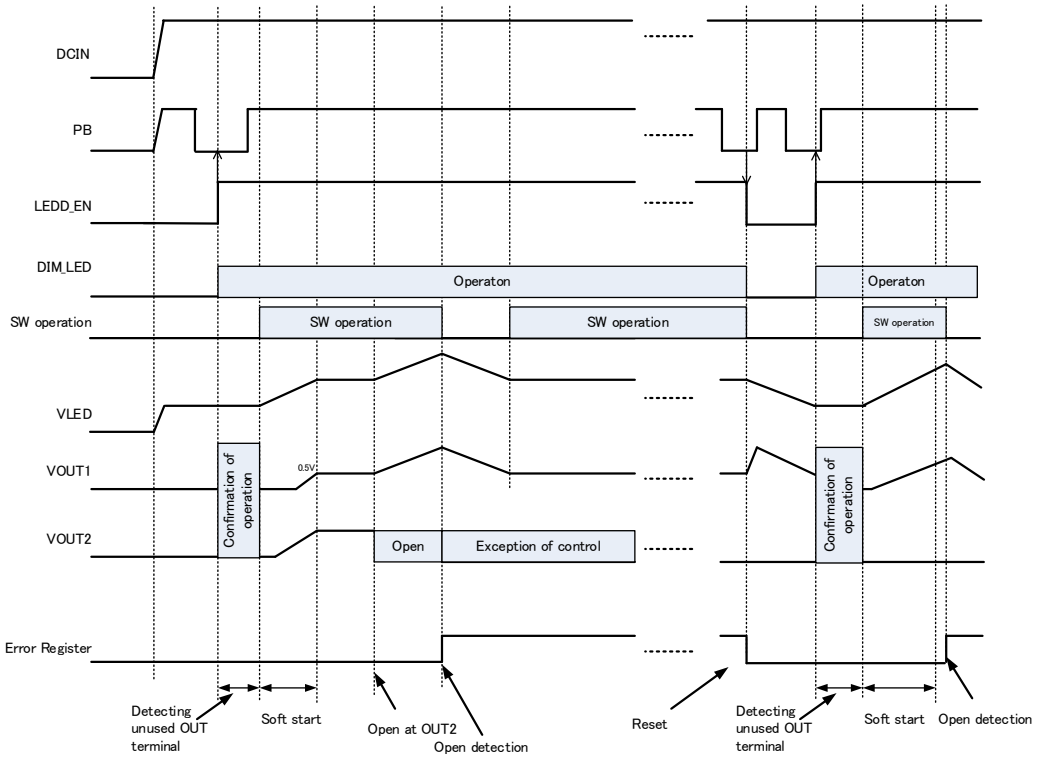
OCL function limits the load current of each DCDC converters.
Each current limit is as follows:

DCDC1: 3.5 A (Min)
DCDC2: 2.0 A (Min)
DCDC3: 2.0 A (Min)
DCDC4: 2.0 A (Min)
LDO1: 300 mA (Min)
LDO2: 350 mA (Min)
LDO3: 120 mA (Min)

13.4. LED Output Open Detection (OOD) and Over Voltage Detection(OVD)

In the case that VLED rises and overvoltage is detected while object of feedback control is the minimum of LEDn (LED1 and/or LED2) terminal, voltage boosting stops and the open state of LEDn terminal is detected. Voltage of LEDn terminal that is open does not rise though VLED rises. So, open state is detected by monitoring the voltage of this LEDn terminal. Normal detecting voltage is 0.2 V (typ.) or less. Output Open Voltage Detection (FB_LED terminal voltage) is 1.228 V (typ.)
When open state is detected, operation of only object LEDn terminal is turned off. They are eliminated from feedback control target and report the error status to register.
When voltage of FB_LED terminal falls 70 mV (typ.) lower than the detecting voltage after overvoltage is detected, SW operation is resumed. In the case that operation is resumed without abnormity of open, IC resumes to normal operation.

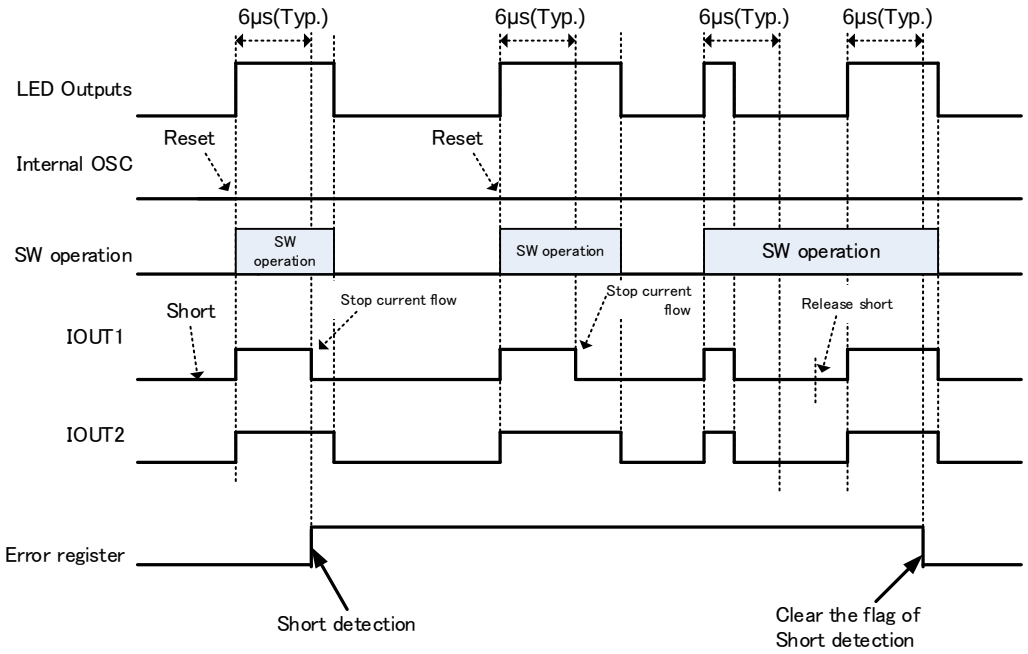
Figure: 28 LED Open Detection function chart



13.5. **LED Short Detection**

When LED current is ON by internal oscillator, short detection starts in the IC after 6 µs (Typ.) passes.
Voltage of LEDn terminal that detects short is defined 5V (Typ.).
Short detection operates while LED current outputs. When short state is detected for 2 µs or longer, operation of target LEDn terminal is turned off and they are eliminated from feedback control target. Then IC report the error status to register.
However, short state is released during operation, operation of target LEDn terminal is resumed and they become object of feedback control. Then IC erases the error status. To confirm the release of short state, detected LEDn terminal operates with constant current drive for 6 µs(Typ.) after LED current outputs.

Figure: 29 LED Short Detection function chart



14. External Parts Selection

This IC evaluates the characteristics with the following external parts.
So, please select an appropriate external parts in reference to following lists.

	Value	Parts name	Parts name	Vender
Inductor	2.2 μH	L1	CDRH4D28NP-2R2NC	SUMIDA CORPORATION
	2.2 μH	L2	CDRH4D28NP-2R2NC	SUMIDA CORPORATION
	2.2 μH	L3	CDRH4D28NP-2R2NC	SUMIDA CORPORATION
	2.2 μH	L4	CDRH4D28NP-2R2NC	SUMIDA CORPORATION
	22 μH	L5	CDRH40D26NP-220NC	SUMIDA CORPORATION
	2.2 μH	L6	CDRH4D28NP-2R2NC	SUMIDA CORPORATION
Capacitance	4.7 μF	C2	C2012X5R1A475K125AA	TDK Corporation
	2.2 μF	C3	C1608X5R1A225K080AC	TDK Corporation
	10 μF	C7	C2012X5R1E106K125AB	TDK Corporation
	10 μF	C8	C2012X5R1E106K125AB	TDK Corporation
	10 μF	C9	C2012X5R1E106K125AB	TDK Corporation
	10 μF	C11	C2012X5R1E106K125AB	TDK Corporation
	10 μF	C13	C2012X5R1E106K125AB	TDK Corporation
	10 μF	C15	C2012X5R1E106K125AB	TDK Corporation
	4.7 μF	C17	C2012X5R1A475K125AA	TDK Corporation
	4.7 μF	C19	C2012X5R1A475K125AA	TDK Corporation
	4.7 μF	C21	C2012X5R1A475K125AA	TDK Corporation
	4.7 μF	C23	C2012X5R1V475K125AC	TDK Corporation
	10 μF	C24	C2012X5R1E106K125AB	TDK Corporation
	4.7 μF	C26	C2012X5R1A475K125AA	TDK Corporation
SBD	-	SD1	CUS15I30A	TOSHIBA CORPORATION

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15. I²C Functions

15.1. I²C IF

Table: 21 Chip Address

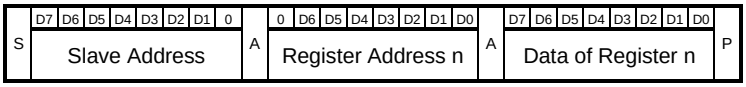
	MSB							LSB
ADD	1	0	0	1	1	1	0	R/$\overline{W}$

15.2. I²C write mode (Slave address: 0x9C)

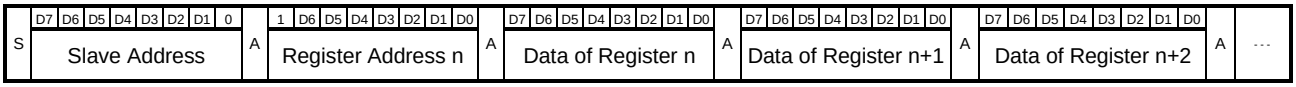
Each transmissions needs to keep more than one clock between each of them. And TC7734FTG supports the following 2 formats.

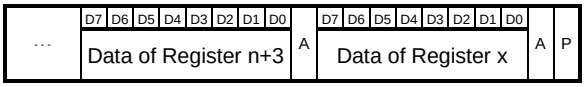
Figure: 30 Format of write mode

Mode1



Mode2





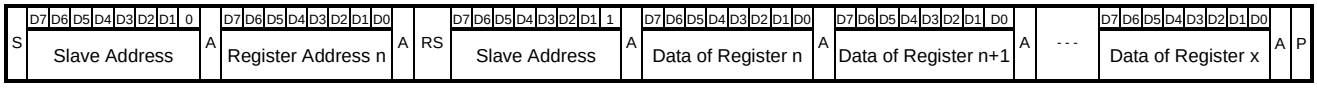
S: Start condition, A: Acknowledge, P: Stop condition

15.3. I²C read mode (Slave address: 0x9D)

Setting Bit [8] of Slave Address switches I²C to read mode. The host should send the stop condition (P) finally after it sent the Acknowledge (high). TC7734FTG supports the following 2 formats.

Figure: 31 Format of read mode

Mode1



S: Start condition, A: Acknowledge, RS: Repeat start condition, P: Stop condition

16. Description of Register

Register is set by writing data to I²C.

The register addresses from 0x00 to 0x29 are for operations. Do not access any other register addresses.

16.1. Register map

Table: 22 I²C Register and Function

Address	Register Name	PASSWORD	R/W	Function
0x00	PWR_EN	-	R/W	Enable/Disable DCDCn converter and LDOn and LEDD.
0x01	STATE1	-	R/W	Status register1
0x02	STATE2	-	R/W	Status register2
0x03	DEFLDO12	Protect	R/W	Set output level of LDO1 and LDO2
0x04	DEFDCDC12	Protect	R/W	Set output level of DCDC1 and DCDC2
0x05	DEFDCDC34	Protect	R/W	Set output level of DCDC3 and DCDC4
0x06	SEQDLY1	Protect	R/W	Set delay time of sequence1
0x07	SEQDLY2	Protect	R/W	Set delay timing of sequence2
0x08	LEDDIM	-	R/W	Set LEDD PWM Dimming
0x09	CHGCNF1	-	R/W	Set Charger configration1
0x0A	CHGCNF2	-	R/W	Set Charger configration2
0x0B	CHGCNF3	-	R/W	Set Charger configration3
0x0C	CHGCNF4	-	R/W	Set Charger configration4
0x0D	CHGCNF5	-	R/W	Set Charger configration5
0x0E	CHGCNF6	-	R/W	Set Charger configration6
0x0F	STATE_CONF	Protect	R/W	Set status migration condition
0x10	INTMASK	-	R/W	Set Interrupt mask
0x11	SYSERRMASK		R/W	Set System error Masking
0x12	PWERRMASK		R/W	Set DCDCn and LDOn error Masking
0x13	LEDDERRMASK		R/W	Set LEDD error Masking
0x14	PGMASK	Protect	R/W	Set Power-good masking
0x15	PASSWORD	-	R/W	Password Protect
0x20	INT_STAT	-	R	Interrupt
0x21	STAT1	-	R	Status confirmation1
0x22	STAT2	-	R	Status confirmation2
0x23	STAT3	-	R	Status confirmation3
0x24	STAT4	-	R	Status confirmation4(SYSTEM error Status)
0x25	STAT5	-	R	Status confirmation5(Power_OCL error Status)
0x26	STAT6	-	R	Status confirmation6(LED Driver error Status)
0x27	PGMON	-	R	PGOOD monitor
0x28	PRODUCTID	-	R	PRODUCT ID (for Toshiba)
0x29	VALUATIONID	-	R	VALUATION ID (for customer)

16.1.1Power Control Register 0x00 (PWR_EN)

Table: 23: 0x00

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LEDD EN	DCDC4EN	DCDC3EN	DCDC2EN	DCDC1EN	not used	LDO2 EN	LDO1 EN
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Default	0	1	1	1	1	0	1	1
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear ：Register set to default in DELAY1 to 3 and OFF
Default clear2：Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
LEDD EN	LEDD Enable/ Disable Control 0 (Default) Disable 1 Enable
DCDC4EN	DCDC4 Enable/ Disable Control 0 Disable 1 (Default) Enable
DCDC3EN	DCDC3 Enable/ Disable Control 0 Disable 1 (Default) Enable
DCDC2EN	DCDC2 Enable/ Disable Control 0 Disable 1 (Default) Enable
DCDC1EN	DCDC1 Enable/ Disable Control 0 Disable 1 (Default) Enable
not used	N/A
LDO2 EN	DCO2 Enable/ Disable Control 0 Disable 1 (Default) Enable
LDO1 EN	LDO1 Enable/ Disable Control 0 Disable 1 (Default) Enable

16.1.2 Status Register1: 0x01 (STATE1)

Table: 24: 0x01

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	OFF	SW STANDBY	ACTIVE
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
OFF	OFF bit. A logic “1” enters the OFF state in the following conditions: . 1) VPOR < VSYS < VUVLO 2) Set “1” by I^2C OFF bit is automatically reset to 0 when it changes to other states.
SW STANDBY	STANDBY bit. A logic “1” enters STANDBY state in the following conditions: . 1) Set “1” by I^2C STANDBY bit is automatically reset to 0 when it changes to other states.
ACTIVE	ACTIVE bit. A logic “1” enters ACTIVE state in the following conditions: . 1) DCIN(IC detect CDP/SDP) asserted from STANDBY state 2) PB pushed down from STANDBY state (PB = “L”) 3) Set “1” by I^2C 4) PB pushed down from OFF state (PB = “L”) 5) DCIN(CDP/SDP) asserted from OFF state Active bit is automatically reset to 0 when it changes to other states.

16.1.3 Status Register2: 0x02 (STATE2)

Table: 25: 0x02

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	SFTRST	not used	DISCHG	CHG	CHG_EN	SDP_CHG_EN	CDP_CHG_EN	DCP_CHG_EN
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	0	1
Default clear	-	-	-	-	Yes	Yes	Yes	Yes
Default clear2	-	-	-	-	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
SFTRST	Soft Reset Command for charger block 0 (Default): Disable 1: Enable NOTE: Charger register is cleared and default value is reloaded. 0x02[D3:D0],0x09 to 0x0E
not used	N/A
DISCHG	Discharge Current Monitor from VBAT to VSYS 0 (Default): No current from VBAT to VSYS 1: Flow current from VBAT to VSYS
CHG	Charge Current Monitor from DCIN to VBAT 0 (Default): No current from DCIN to VBAT 1: Flow current from DCIN to VBAT
CHG_EN	Charger Enable/Disable Control 0: Disable 1 (Default): Enable
SDP_CHG_EN	SDP Charger Enable in STANDBY and OFF states when VBAT < VSYS_LOW[2:0] threshold. 0: Disable 1 (Default): Enable
CDP_CHG_EN	CDP Charger Enable in STANDBY and OFF states when VBAT < VSYS_LOW[2:0] threshold. 0 (Default): Disable 1: Enable
DCP_CHG_EN	DCP Charger Enable in STANDBY and OFF states. 0: Disable 1 (Default): Enable

16.1.4 LDO1 and LDO2 Control Register: 0x03(DEFLDO12)

Table: 26: 0x03

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	VLDO2[2:0]			not used	VLDO1[2:0]		
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Default	0	1	1	0	0	1	1	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
VLDO2[2:0]	LDO2 Output Voltage Selection 000 → 1.50 V 001 → 1.60 V 010 → 1.70 V 011 → 1.80 V 100 → 2.30 V 101 → 2.50 V 110 (Default) → 2.80 V 111 → N/A
VLDO1[2:0]	LDO1 Output Voltage Selection 0000 → 1.2 V 0001 → 1.3 V 0010 → 1.4 V 0011 → 1.5 V 0100 → 1.6 V 0101 → 1.7 V 0110(Default) → 1.8 V 0111 → 1.9 V

16.1.5 DCDC1 and DCDC2 Control Register: 0x04 (DEFDCDC12)

Table: 27: 0x04

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	VDCDC2[2:0]			VDCDC1[3:0]			
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	1	0	0	0	1	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
VDCDC2[2:0]	DCDC2 Output Voltage Selection

	DCDC2 [V]
000	1.05
001	1.20
010(Default)	**1.35**
011	1.50
100	1.65
101	1.80
110	1.95
111	N/A

VDCDC1[3:0] — DCDC1 Output Voltage Selection

	DCDC1 [V]
0000	0.90
0001	0.95
0010(Default)	1.00
0011	1.05
0100	1.10
0101	1.15
0110	1.20
0111	1.25
1000	1.30
1001	1.35
1010	1.40
1011	N/A
1100	N/A
1101	N/A
1110	N/A
1111	N/A

16.1.6 DCDC3 and DCDC4 Control Register: 0x05 (DEFDCDC34)

Table: 28: 0x05

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DC4_PS	not used	not used	not used	DC3_PS	VDCDC3[2:0]		
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	0
Default clear	Yes	-	-	-	Yes	Yes	Yes	Yes
Default clear2	Yes	-	-	-	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
DC4_PS	Phase Select Bit for DCDC4 0 (Default): Phase 1 select (same phase with DCDC1) 1: Phase 2 select (different phase with DCDC1)
not used	N/A
not used	N/A
not used	N/A
DC3_PS	Phase Select Bit for DCDC3 0: Phase 1 select (same phase with DCDC1) 1 (Default): Phase 2 select (different phase with DCDC1)
VDCDC3[2:0]	DCDC3 output voltage control

	DCDC3 [V]
000	2.70
001	2.80
010	2.90
011	3.00
100	3.10
101	3.20
110 (Default)	3.30
111	3.40

16.1.7 Delay Time Setting Register: 0x06 (SEQDLY1)

Table: 29: 0x06

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	DLY 3		DLY 2		DLY 1	
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	0
Default clear	-	-	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	-	-	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

<table>
<tr><th>Field name</th><th>BIT DEFINITION</th></tr>
<tr><td>not used</td><td>N/A</td></tr>
<tr><td>DLY 3</td><td>DCDC4 Turn-ON Delay Setting
<table>
<tr><th></th><th>Delay time</th></tr>
<tr><td>00 (Default)</td><td>1 ms</td></tr>
<tr><td>01</td><td>2 ms</td></tr>
<tr><td>10</td><td>4 ms</td></tr>
<tr><td>11</td><td>8 ms</td></tr>
</table></td></tr>
<tr><td>DLY 2</td><td>DCDC2 Turn-ON Delay Setting
<table>
<tr><th></th><th>Delay time</th></tr>
<tr><td>00</td><td>1 ms</td></tr>
<tr><td>01(Default)</td><td>2 ms</td></tr>
<tr><td>10</td><td>4 ms</td></tr>
<tr><td>11</td><td>8 ms</td></tr>
</table></td></tr>
<tr><td>DLY 1</td><td>Ext Enable Turn-ON Delay Setting
<table>
<tr><th></th><th>Delay time</th></tr>
<tr><td>00 (Default)</td><td>1 ms</td></tr>
<tr><td>01</td><td>2 ms</td></tr>
<tr><td>10</td><td>4 ms</td></tr>
<tr><td>11</td><td>8 ms</td></tr>
</table></td></tr>
</table>

16.1.8 Output Delay Setting Register: 0x07 (SEQDLY2)

Table: 30: 0x07

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	SEQTYPE	PWROFFSEQ	not used	not used	not used	DLY3EN	DLY2EN	DLY1EN
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	0
Default clear	Yes	Yes	-	-	-	Yes	Yes	Yes
Default clear2	Yes	Yes	-	-	-	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
SEQTYPE	DCDCn and LDOn power up/turn off sequence setting bit 0 (Default): Power up: DCDC1 -> EXT_EN -> DCDC2 -> DCDC4-> LDO2, DCDC3 -> LDO1 Power down: LDO1 -> DCDC3 , LDO2 -> DCDC4 -> DCDC2 -> EXT_EN -> DCDC1 1: Power up: DCDC1 -> DCDC2 -> EXT_EN -> DCDC4-> LDO2, DCDC3 -> LDO1 Power down: LDO1 -> DCDC3 , LDO2 -> DCDC4 -> EXT_EN -> DCDC2 -> DCDC1
PWROFFSEQ	Turn off sequence setting bit 0 (Default): Each turn off delay time is set by and 0x06 0x07[4:0]. (Same as power on sequence delay time) 1: (DCDC1 to 4 and LDO1,2 shutdown at same time
not used	N/A
not used	N/A
not used	N/A
DLY3EN	DCDC4 Delay Time Disable Bit (without 80% monitor) 0: DLY3 delay time is disable 1 (Default): DLY3 delay time is enable
DLY2EN	DCDC2 Delay Time Disable Bit (without 80% monitor) 0: DLY2 delay time is disable. 1 (Default): DLY2 delay time is enable
DLY1EN	EXT_EN Delay Time Disable Bit (without 80% monitor) 0 (Default): DLY1 delay time is disable. 1: DLY1 delay time is enable

16.1.9 LED Driver Dimming Control Register: 0x08 (LEDDIM)

Table: 31: 0x08

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LEDD_PS	not used	LEDDIM[5:0]					
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	1	1	0	1
Default clear	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
LEDD_PS	Phase Select Bit for LED Driver 0 : Phase 1 select (same phase with DCDC1) 1 (Default) : Phase 2 select (different phase with DCDC1)
not used	N/A
not used	N/A
LEDDIM[5:0]	6-Bit PWM Dimming Control

	LED Current [%]
00 0000	0.0
00 0001	3.1
00 0010	6.3
00 0011	9.4
00 0100	12.5
00 0101	15.6
00 0110	18.8
00 0111	21.9
00 1000	25.0
00 1001	28.1
00 1010	31.3
00 1011	34.4
00 1100	37.5
00 1101(Default)	40.6
00 1110	43.8
00 1111	46.9
01 0000	50.0

	LED Current [%]
01 0001	53.1
01 0010	56.3
01 0011	59.4
01 0100	62.5
01 0101	65.6
01 0110	68.8
01 0111	71.9
01 1000	75.0
01 1001	78.1
01 1010	81.3
01 1011	84.4
01 1100	87.5
01 1101	90.6
01 1110	93.8
01 1111	96.9
1X XXXX	100

16.1.10 Charger Configuration Register1: 0x09 (CHGCNF1)

Table: 32: 0x09

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	CCVTH[2:0]			FLTV[1:0]	
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	1	0	0	1	0
Default clear	-	-	-	Yes	Yes	Yes	Yes	Yes
Default clear2	-	-	-	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
CCVTH[2:0]	Voltage Threshold from Pre-charge to Fast Charge. 000 – 2.5 V 001 – 2.6 V 010 – 2.7 V 011 – 2.8 V 100 (Default) – 2.9 V 101 – 3.0 V 110 – 3.1 V 111 – 3.2 V
FLTV[1:0]	Float Voltage 00 – 4.10 V 01 – 4.15 V 10 (Default) – 4.20 V 11 – 4.25 V

16.1.11 Charger Configuration Register2: 0x0A (CHGCNF2)

Table: 33: 0x0A

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PCI[1:0]		CCI[3:0]				CEI[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	0	0	0	0	1	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

<table>
<tr><th>Field name</th><th>BIT DEFINITION</th></tr>
<tr><td>PCI[1:0]</td><td>Pre-charge Current and Trickle charge current
<table>
<tr><td></td><td>Pre-charge</td><td>Trickle charge</td></tr>
<tr><td>00</td><td>75 mA</td><td>37 mA</td></tr>
<tr><td>01</td><td>100 mA</td><td>50 mA</td></tr>
<tr><td>10</td><td>250 mA</td><td>125 mA</td></tr>
<tr><td>11(Default)</td><td>400 mA</td><td>200 mA</td></tr>
</table></td></tr>
<tr><td>CCI[3:0]</td><td>Current of Fast Charge
<table>
<tr><td>0000 (Default)</td><td>No change, use Auto Detect CC</td><td></td><td>1001</td><td>1,200 mA</td></tr>
<tr><td>0001</td><td>400 mA</td><td></td><td>1010</td><td>1,300 mA</td></tr>
<tr><td>0010</td><td>500 mA</td><td></td><td>1011</td><td>1,400 mA</td></tr>
<tr><td>0011</td><td>600 mA</td><td></td><td>1100</td><td>1,500 mA</td></tr>
<tr><td>0100</td><td>700 mA</td><td></td><td></td><td></td></tr>
<tr><td>0101</td><td>800 mA</td><td></td><td></td><td></td></tr>
<tr><td>0110</td><td>900 mA</td><td></td><td></td><td></td></tr>
<tr><td>0111</td><td>1,000 mA</td><td></td><td></td><td></td></tr>
<tr><td>1000</td><td>1,100 mA</td><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>CEI[1:0]</td><td>Charge Completion Current.
Charging is judged as completed when charging current decreases to the value set by CEI[1:0] or less.
<table>
<tr><td>00</td><td>50 mA</td></tr>
<tr><td>01</td><td>75 mA</td></tr>
<tr><td>10 (Default)</td><td>100 mA</td></tr>
<tr><td>11</td><td>200 mA</td></tr>
</table></td></tr>
</table>

16.1.12 Charger Configuration Register3: 0x0B (CHGCNF3)

Table: 34: 0x0B

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ATRCHGTH	ATRCHG	ATLMTTH[1:0]		ATILMT	OVTHL[1:0]		CT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	1	1	1	0	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
ATRCHGTH	Threshold for Automatic Re-Charge. If battery voltage is down below “Float voltage - ATRCHGTH”, IC restart the charge function. 0 (Default) : 150 mV 1 : 300 mV
ATRCHG	Auto Re-Charge function setting 0 : Disable 1 (Default) : Enable
ATLMTTH[1:0]	Threshold Voltage of Automatic Input Current Limit If DCIN voltage is down, DCIN input current sets the limit as 100 mA. 00 : 3.75 V 01 (Default) : 4.00 V 10 : 4.25 V 11 : 4.50 V
ATILMT	Limit of Automatic Input Current , ON /OFF control of ATLMTTH function 0 : Disable 1 (Default) : Enable Limit of input current is set the limit as 100mA when DCIN falls to the level set by ATLMTTH<1:0>. When interrupt is cleared, it is set to the previous limit level.
OVTHL[1:0]	Voltage threshold in over charge If battery voltage is over “Float voltage + OVTHL”, IC outputs the interrupt. 00 : 200 mV 01 : 150 mV 10 (Default) : 100 mV 11 : 50 mV
CT	Charge Termination setting. If set to “1”, IC continues to charge even after reaching the battery charge current to CEI setting current. 0 (Default) : Permitting termination of charging cycle. 1 : Not permitting termination of charging cycle.

16.1.13 Charger Configuration Register4: 0x0C (CHGCNF4)

Table: 35: 0x0C

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	CHGTMCLR	PRCHGTMS	CGTMS[1:0]		PCGTM_EN	CGTM_EN	TCSTON
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	1	1	1	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
CHGTMCLR	Clear of Pre-charge Safety Timer and Charge Safety Timer 0 (Default): Normal operation of timer 1: Both Pre-charge timer and Charge timer are cleared. (Pulse command) In this time, status information of Pre-charge and charge timer is cleared.
PRCHGTMS	Pre-charge Safety Timer 0 (Default): 30 min 1: 60 min
CGTMS[1:0]	Charge Safety Timer 00: 240 min 01: 300 min 10: 360 min 11 (Default): 480 min
PCGTM_EN	Pre-charge Safety Timer Enable 0: Pre-charge safety timer: Invalid 1 (Default): Pre-charge safety timer: Valid
CGTM_EN	Charge Safety Timer Enable 0: Charge safety timer: Invalid 1 (Default): Charge safety timer: Valid
TCSTON	Trickle Charge Safety Timer 0 (Default): Pre-charge safety timer and charge safety timer do not operate in trickle charging. 1: Pre-charge safety timer and charge safety timer operate in trickle charging.

16.1.14 Charger Configuration Register5: 0x0D (CHGCNF5)

Table: 36: 0x0D

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DCP Auto CC		CDP Auto CC		USBILMT[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	0	0	0	0	0
Default clear	-	-	-	-	Yes	Yes	Yes	Yes
Default clear2	-	-	-	-	-	-	-	-

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
DCP Auto CC[1:0]	DCP Auto Charge Current 00 — 750 mA 01 — 1000 mA 10 — 1250 mA 11 (Default) — 1500 mA
CDP Auto CC[1:0]	CDP Auto Charge Current 00 — 500 mA 01 — 750 mA 10 (Default) — 1000 mA 11 — 1500 mA
USBILMT[3:0]	Limit of DCIN Input Current

	Normal	DPPM
0000 (Default)	DCP or Other: 1500 mA CDP: 1000 mA SDP: 500 mA	DCP or Other: 500 mA CDP: 500 mA SDP: 500 mA
0001	100 mA	100 mA
0010	300 mA	100 mA
0011	400 mA	100 mA
0100	500 mA	500 mA
0101	700 mA	500 mA
0110	1,000 mA	500 mA
0111	1,200 mA	500 mA
1000	1,400 mA	500 mA
1001	1,500 mA	500 mA

16.1.15 Charger Configuration Register6: 0x0E (CHGCNF6)

Table: 37: 0x0E

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	DISBAT	COLDTEMP	HOTTEMP[1:0]		RTYPE
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0
Default clear	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
DISBAT	Battery auto discharge enable/disable 0(Default) – Disable 1 – Enable
COLDTEMP	Stop charge current in cold temperature 0 (Default) – 0 ºC 1 – 10ºC
HOTTEMP[1:0]	Stop charge current in hot temperature. 00 – 45ºC 01(Default) – 60ºC 10 – 50ºC 11 – N/A
RTYPE	Using thermistor type 0 (Default) – 10 kΩ, ß = 3435 1 – 100 kΩ, ß = 4100

16.1.16 State Configuration Register: 0x0F (STATE_CONF)

Table: 38: 0x0F

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VSYS_LOW[2:0]			Not used	VUVLO[1:0]		PGDLY[1:0]	
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default	0	1	1	0	1	0	1	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
VSYS_LOW[2:0]	000 2.90 V; 001 3.00 V; 010 3.15 V; 011 (Default) 3.30 V; 100 3.45 V; 101 3.55 V; 110 3.65 V; 111 3.75 V
not used	N/A
VUVLO[1:0]	00 2.60 V; 01 2.90 V; 10 (Default) 3.10 V; 11 3.35 V Notes: VUVLO voltage should set lower voltage than VSYS_LOW voltage.
PGDLY[1:0]	Power-good Delay 00 20 ms; 01 100 ms; 10 (Default) 200 ms; 11 400 ms

16.1.17 Interrupt MASK Setting Register1: 0x10 (INTMASK)

Table: 39: 0x10

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	INTATIL_MK	INTRCHG_MK	INTCHGER_MK	INTCHGCMP_MK	INTSYSFAULT_MK	INTPB_MK	INTUSBAC_MK	INTPWFAULT_MK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Default clear	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
INTATIL_MK	Limit of Automatic Input Current interrupt Mask 0 (Default): interrupt is issued when status changes (DCIN voltage falls below the threshold) 1: No interrupt is issued when status changes(DCIN voltage falls below the threshold) NOTE: If no interrupt is issued when status changes, set ATILMT(0x0B[D3]) register to "0".
INTRCHG_MK	Re-charge Status Change Interrupt Mask 0 (Default): Interrupt is issued when charge status change by "Vbat < Vfloat – 150/300 mV" after charge completion 1: No interrupt is issued when charge status change by "Vbat < Vfloat – 150/300 mV" after charge completion NOTE: If no interrupt is issued when charge status changes, set ATRCHG(0x0B [D6]) register to "0".
INTCHGER_MK	Charge Status Change Interrupt Mask 0 (Default): interrupt is issued when charger detects error in status 1: No interrupt is issued even when charger detects the error in status NOTE: Status information is available in STATUS register 0x22.
INTCHGCMP_MK	Charge Completion Status Change Interrupt Mask 0 (Default): interrupt is issued when charger detects the charge completion 1: No interrupt is issued when Charger detects the completion in status NOTE: Status information is available in STATUS register 0x23.
INTSYSFAULT_MK	System Status Change Interrupt Mask 0 (Default): interrupt is issued when System status error change 1: no interrupt is issued when System status error change NOTE: Status information is available in STATUS register 0x24.
INTPB_MK	Pushbutton Status Change Interrupt Mask 0 (Default): interrupt is issued when PB status changes 1: no interrupt is issued even when PB status changes NOTE: Status information is available in STATUS register 0x21[D0].
INTUSBAC_MK	USB Detection Interrupt Mask 0 (Default): interrupt is issued when DCIN is detect or removed 1: no interrupt is issued when DCIN input is detect or removed NOTE: Status information is available in STATUS register 0x21[D5, D2,D1].
INTPWFAULT_MK	DCDCn and LDOn and LEDD Status Change Interrupt Mask 0 (Default): interrupt is issued when DCDCn and LDOn and LEDD status error change 1: no interrupt is issued when DCDCn and LDOn and LEDD status error change NOTE: Status information is available in STATUS registers 0x25 and 0x26.

16.1.18 System error Masking Setting Register: 0x11 (SYSERRMASK)

Table: 40: 0x11

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	SYS_LOW_MK	TSD_MK
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0
Default clear	-	-	-	-	-	-	Yes	Yes
Default clear2	-	-	-	-	-	-	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
VSYS_LOW _MK	VSYS_LOW Masking Bit 0 (Default): interrupt is issued when VSYS_LOW status changes 1: no interrupt is issued even when VSYS_LOW status changes
TSD _MK	TSD Masking Bit 0 (Default): interrupt is issued when TSD status changes 1: no interrupt is issued even when TSD status changes

16.1.19 DCDCn and LDOn error Masking Setting Register: 0x12 (PWERRMASK)

Table: 41: 0x12

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	DC4_OCL_MK	DC3_OCL_MK	DC2_OCL_MK	DC1_OCL_MK	not used	LDO2_OCL_MK	LDO1_OCL_MK
R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W
Default	0	0	0	0	0	0	0	0
Default clear	-	Yes	Yes	Yes	Yes	-	Yes	Yes
Default clear2	-	Yes	Yes	Yes	Yes	-	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
DC4_OCL_MK	DC4_OCL Masking Bit 0 (Default): interrupt is issued when DCDC4_OCL error status changes 1: no interrupt is issued even when DCDC4_OCL error status changes
DC3_OCL_MK	DC3_OCL Masking Bit 0 (Default): interrupt is issued when DCDC3_OCL error status changes 1: no interrupt is issued even when DCDC3_OCL error status changes
DC2_OCL_MK	DC2_OCL Masking Bit 0 (Default): interrupt is issued when DCDC2_OCL error status changes 1: no interrupt is issued even when DCDC2_OCL error status changes
DC1_OCL_MK	DC1_OCL Masking Bit 0 (Default): interrupt is issued when DCDC1_OCL error status changes 1: no interrupt is issued even when DCDC1_OCL error status changes
not used	N/A
LDO2_OCL_MK	LDO2_OCL Masking Bit 0 (Default): interrupt is issued when LDO2_OCL error status changes 1: no interrupt is issued even when LDO2_OCL error status changes
LDO1_OCL_MK	LDO1_OCL Masking Bit 0 (Default): interrupt is issued when LDO1_OCL error status changes 1: no interrupt is issued even when LDO1_OCL error status changes

16.1.20 LEDD error Masking Setting Register: 0x13 (LEDDERRMASK)

Table: 42: 0x13

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	OSD2_MK	OSD1_MK	OOD2_MK	OOD1_MK	UULED2_MK	UULED1_MK	OVD_MK
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	0
Default clear	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Default clear2	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
OSD2_MK	OSD2 Masking Bit 0 (Default): interrupt is issued when LED2 OSD error status changes 1: no interrupt is issued even when LED2 OSD error status changes
OSD1_MK	OSD1 Masking Bit 0 (Default): interrupt is issued when LED1 OSD error status changes 1: no interrupt is issued even when LED1 OSD error status changes
OOD2_MK	OOD2 Masking Bit 0 (Default): interrupt is issued when LED2 OOD error status changes 1: no interrupt is issued even when LED2 OOD error status changes
OOD1_MK	OOD1 Masking Bit 0 (Default): interrupt is issued when LED1 OOD error status changes 1: no interrupt is issued even when LED1 OOD error status changes
UULED2_MK	Un-used LED2 Masking Bit 0: interrupt is issued when LED2 un-used flag status changes 1(Default): no interrupt is issued even when LED2 un-used flag status changes
UULED1_MK	Un-used LED1 Masking Bit 0: interrupt is issued when LED1 un-used flag status changes 1 (Default): no interrupt is issued even when LED1 un-used flag status changes
OVD_MK	OVD Masking Bit 0 (Default): interrupt is issued when OVD error status changes 1: no interrupt is issued even when OVD error status changes

16.1.21 Power-good Masking Setting Register: 0x14 (PGMASK)

Table: 43: 0x14

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	DC4PG_MK	DC3PG_MK	DC2PG_MK	DC1PG_MK	not used	LDO2PG_MK	LDO1PG_MK
R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W
Default	0	0	0	0	0	0	0	0
Default clear	-	Yes	Yes	Yes	Yes	-	Yes	Yes
Default clear2	-	Yes	Yes	Yes	Yes	-	Yes	Yes

Default clear : Register set to default in DELAY1 to 3 and OFF
Default clear2 : Register set to default in HW STANDBY and ACTIVE

Field name	BIT DEFINITION
not used	N/A
DC4PG_MK	DCDC4 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if DCDC4_PG is low (DCDC4 does not power up) 1: DCDC4_PG status does not affect the status of the PGOOD output pin
DC3PG_MK	DCDC3 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if DCDC3_PG is low (DCDC3 does not power up) 1: DCDC3_PG status does not affect the status of the PGOOD output pin
DC2PG_MK	DCDC2 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if DCDC2_PG is low (DCDC2 does not power up) 1: DCDC2_PG status does not affect the status of the PGOOD output pin
DC1PG_MK	DCDC1 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if DCDC1_PG is low (DCDC1 does not power up) 1: DCDC1_PG status does not affect the status of the PGOOD output pin
not used	N/A
LDO2PG_MK	LDO2 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if LDO2_PG is low (LDO2 does not power up) 1: LDO2_PG status does not affect the status of the PGOOD output pin
LDO1PG_MK	LDO1 Power-good Masking Bit 0 (Default): PGOOD pin is pulled low if LDO1_PG is low (LDO1 does not power up) 1: LDO1_PG status does not affect the status of the PGOOD output pin

16.1.22 Password Protect Register: 0x15 (PASSWORD)

Table: 44: 0x15

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PWD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
PWD[7:0]	PWD: Password to unlock the password protected registers 0xAB: Password protected registers are unlocked in the next write cycle The others: No effect (Password protected registers are locked for write access)

16.1.23 Interrupt Register: 0x20 (INT_STAT)

Table: 45: 0x20

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	INTATIL	INTRCHG	INTCHGER	INTCHGCMP	INTSYSFAULT	INTPB	INTUSBAC	INTPWFAULT
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
INTATIL	Limit of Automatic Input Current Interrupt 0 (Default): no change in status 1: Status changes (DCIN voltage falls below the threshold set by I^2C[0x0B (D5,D4)]) NOTE: To disable interrupt, set ATILMT(0x0B[D3]) register to “0”.
INTRCHG	Re-Charge Status Change Interrupt 0 (Default): Charge is completed or no change in charge status 1: Charge status changes by “Vbat < Vfloat – 150/300 mV” after charge completion NOTE: To disable interrupt, set ATRCHG(0x0B [D6]) register to “0”.
INTCHGER	Charge Status Change Interrupt 0 (Default): No charger error in status 1: Charger status error change NOTE: Status information is available in STATUS register 0x22.
INTCHGCMP	Charge Completion Status Change Interrupt 0 (Default): No charge in charging status or not charging 1: Charge completion status changes when “Ichg < Iterm” NOTE: Status information is available in STATUS register 0x23.
INTSYSFAULT	System Status Change Interrupt 0 (Default): no change error in status 1: System status error change NOTE: Status information is available in STATUS register 0x24.
INTPB	Pushbutton Status Change Interrupt 0 (Default): No change in status 1: PB status change (PB_IN changed high to low or low to high) NOTE: Status information is available in STATUS register 0x21[D0].
INTUSBAC	USB Detection Interrupt 0 (Default): no change in status 1: USB or AC power status detect (power to DCIN pin has either been applied or removed) NOTE: Status information is available in STATUS register 0x21[D5, D2,D1].
INTPWFAULT	DCDCn and LDOn and LEDD Status Change Interrupt 0 (Default): no change in status 1: DCDCn or LDOn or LEDD status error change NOTE: Status information is available in STATUS registers 0x25 and 0x26.

These fields are cleared by SOC read access.

16.1.24 State Monitoring Register1: 0x21 (STAT1)

Table: 46: 0x21

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	ST_USBAC	ST_DTBSY	ST_PSDST	ST_STYP[1:0]		ST_PB
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
not used	N/A
not used	N/A
ST_USBAC	DCIN detection result. 0 – Not detect DCIN 1 – Detect DCIN
ST_DTBSY	Detection of Power Source 0 – Not busy 1 – Busy
ST_PSDST	Detection of Power Source 0 – Detecting or not detect DCIN 1 – Finish (after judge)
ST_STYP[1:0]	USB detection result 00 – No connection / No detection / Other 01 – SDP (Standard Downstream Port) 10 – CDP (Charging Downstream Port) 11 – DCP (Dedicated Charging Port)
ST_PB	Detection of Push Button 0 – Released Button 1 – Pushed button

*Please refer to Figure: 26 Relation with Function timing chart detecting USB and 0x21 register

16.1.25 State Monitoring Register2: 0x22 (STAT2)

Table: 47: 0x22

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ST_DISBAT	ST_VBATN	ST_BATOV	ST_DCOVL	ST_DCUVL	ST_OVT	ST_BATHT	ST_BATLT
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
ST_DISBAT	0 – No Battery Discharge 1 – Battery Discharge Note: Interrupt shall only occur on transition from no discharge to discharge.
ST_VBATN	Status: Initial value depends on DCIN input and battery voltage. 0 – DCIN – 125 mV >= VBATT 1 – DCIN – 125 mV < VBATT
ST_BATOV	Status: Initial value depends on battery voltage. 0 – Battery OVLO not detect 1 – Battery OVLO detect
ST_DCOVL	Status: Initial value depends on DCIN voltage. 0 – DCIN OVLO not detect 1 – DCIN OVLO detect
ST_DCUVL	Status: Initial value depends on DCIN voltage. 0 – DCIN UVLO not detect 1 – DCIN UVLO detect
ST_OVT	Status: Initial value depends on charger block temperature. 0 – Chip temperature is normal. Charger operates 1 – IC detects high Chip temperature (T_{OVT}). Charger stops to limit internal temperature
ST_BATHT	Status: Initial value depends on battery temperature. Detect temperature is set by 0x0E[D2:D1]. 0 – High temperature of battery is not detected 1 – High temperature of battery is detected.
ST_BATLT	Status: Initial value depends on battery temperature. Detect temperature is set by 0x0E[D0]. 0 – Low temperature of battery is not detected. 1 – Low temperature of battery is detected.

16.1.26 State Monitoring Register3: 0x23 (STAT3)

Table: 48: 0x23

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ST_TMER[1:0]		ST_CGED1	ST_CGED0	ST_TRCHG	ST_CGMD[1:0]		not used
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
ST_TMER[1:0]	Safety Timer 00: Time out is not generated. 01: Pre-charge timer: pass. 10: Charging timer: pass. 11: Charge start is waited.
ST_CGED1	Charge completion 0: Not complete the Charge function 1: At least, one cycle starts and completes. And output interrupt. If DCIN is disconnected, this status is cleared.
ST_CGED0	Charge completion: Initial value depends on charge current. 0: Charge current does not reach the CEI current in Taper Charge mode 1: Charge current reaches the CEI current in Taper Charge mode
ST_TRCHG	Trickle charge mode Status 0: No Trickle charge mode 1: Trickle charge mode (VBATT < 2.05 V)
ST_CGMD[1:0]	Charge Mode 00: No charge 01: Pre-charge, Trickle charge 10: Fast Charge (Constant-Current Charge Mode) 11: Taper Charge (Constant-Voltage Charge Mode)
not used	N/A

16.1.27 State Monitoring Register4: 0x24 (STAT4)

Table: 49: 0x24

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	ST_VSYS_LOW	ST_TSD
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
ST_VSYS_LOW	SYS_LOW detection 0 VSYS > VSYS_LOW 1 VSYS =< VSYS_LOW
ST_TSD	TSD error status check 0 IC chip temperature < TSD 1 IC chip temperature >= TSD

16.1.28 State Monitoring Register5: 0x25 (STAT5)

Table: 50: 0x25

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	ST_OCLDC4	ST_OCLDC3	ST_OCLDC2	ST_OCLDC1	not used	ST_OCLLDO2	ST_OCL LDO1
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
not used	N/A
ST_OCLDC4	DCDC4 OCL detection 0 DCDC4 OCL not detect 1 DCDC4 OCL detect
ST_OCLDC3	DCDC3 OCL detection 0 DCDC3 OCL not detect 1 DCDC3 OCL detect
ST_OCLDC2	DCDC2 OCL detection 0 DCDC2 OCL not detect 1 DCDC2 OCL detect
ST_OCLDC1	DCDC1 OCL detection 0 DCDC1 OCL not detect 1 DCDC1 OCL detect
not used	N/A
ST_OCL LDO2	LDO2 OCL detection 0 LDO2 OCL not detect 1 LDO2 OCL detect
ST_OCL LDO1	LDO1 OCL detection 0 LDO1 OCL not detect 1 LDO1 OCL detect

16.1.29 State Monitoring Register6: 0x26 (STAT6)

Table: 51: 0x26

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	ST_OSD2	ST_OSD1	ST_OOD2	ST_OOD1	ST_UULED2	ST_UULED1	ST_OVD
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
not used	N/A
ST_OSD2	LED2 OSD detection 0: LED2 OSD not detect 1: LED2 OSD detect
ST_OSD1	LED1 OSD detection 0: LED1 OSD not detect 1: LED1 OSD detect
ST_OOD2	LED2 OOD detection 0: LED2 OOD not detect 1: LED2 OOD detect
ST_OOD1	LED1 OOD detection 0: LED1 OOD not detect 1: LED1 OOD detect
ST_UULED2	LED2 Un-used detection 0: LED2 Un-used not detect 1: LED2 Un-used detect
ST_UULED1	LED1 Un-used detection 0: LED1 Un-used not detect 1: LED1 Un-used detect
ST_OVD	LEDD OVD detection 0: FBLED < OVD detecting threshold 1: FBLED >= OVD detecting threshold

16.1.30 PGOOD Monitoring Register: 0x27 (PGMON)

Table: 52: 0x27

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	DC4 PGM	DC3PGM	DC2 PGM	DC1 PGM	not used	LDO2 PGM	LDO1 PGM
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	1

Field name	BIT DEFINITION
not used	N/A
DC4 PGM	DCDC4 Power-good 0: DCDC4 is either disabled or not in regulation 1: DCDC4 is in regulation
DC3PGM	DCDC3 Power-good 0: DCDC3 is either disabled or not in regulation 1: DCDC3 is in regulation
DC2 PGM	DCDC2 Power-good 0: DCDC2 is either disabled or not in regulation 1: DCDC2 is in regulation
DC1 PGM	DCDC1 Power-good 0: DCDC1 is either disabled or not in regulation 1: DCDC1 is in regulation
not used	N/A
LDO2 PGM	LDO2 Power-good 0: LDO2 is either disabled or not in regulation 1: LDO2 is in regulation
LDO1 PGM	LDO1 Power-good 0: LDO1 is either disabled or not in regulation 1: LDO1 is in regulation

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16.1.31 PRODUCT ID Register: 0x28 (PRODUCTID)

Table: 53: 0x28

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PRODUCT_CODE[3:0]				not used	not used	not used	not used
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	-	-	-	-

Field name	BIT DEFINITION
PRODUCT_CODE	Product code 0000: TC7734FTG other: N/A(future use)
not used	N/A
not used	N/A
not used	N/A
not used	N/A

16.1.32 Valuation ID Register: 0x29 (VALUATIONID)

Table: 54: 0x29

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	VAL_CODE[3:0]			
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Field name	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
VAL_CODE[3:0]	Valuation code 0000 Valuation 1 other N/A(future use)

17.Electrical Characteristics

17.1. Absolute Maxumum Ratings

(Ta = 25ºC)

Characteristic	Symbol	Rating	Unit
DC IN terminal voltage	VINMAX	-0.3 to 6.0	V
Supply voltage	VDDMAX	-0.3 to 6.0	V
Maximum of applied voltage for each terminal	V_{I1} (without LED1,LED2,SW, CHG_STAT, VREF)	GND – 0.3 to VDD+0.3 or 6.0 V (Lower value is applied)	V
	LED1,LED2,SW	30	V
	CHG_STAT	GND – 0.3 to DCIN+0.3	V
	VREF	GND – 0.30 to 1.65	
Power dissipation	P_D (Note1,2)	3.5	W
Operating temperature	T_{opr}	-40 to 85	°C
Operating junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

*The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing design, refer to and comply with the precautions and conditions set forth in this document.

Note1**:** PCB condition is 74 mm × 74 mm × 1.6 mm, 4 layer, FR-4

Note2**:** When ambient temperature is 25°C or more, reciprocal of saturated heat resistance (1/Rth(j-a)) should be reduced every 1°C rise.

17.2. Operating Voltage Range

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply Voltage	DCIN	4.3	-	5.5	V
	V_{DD}	3.4	-	5.5	V

17.3. Power Consumption

(Unless otherwise specified VDD = 3.6 V, and Ta = 25ºC)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Power Consumption	IVDD1	OFF State LDO3 No-load DCIN no connect	-	80	104	µA
	IVDD2	Standby State, LDO3 No-load, 0x0E[D4]=0 (default) DCIN no connect	-	130	170	µA
		Standby State, LDO3 No-load, 0x0E[D4]=1 DCIN no connect	-	150	200	µA
	IVDD3	Active State DCDC1,2,3,4**:** ON No-load LDO1,2,3**:** ON No-load LEDD**:** OFF DCIN no connect	-	2.1	-	mA

17.4. **System Protection Characteristics**

(Unless otherwise specified, VDD = 3.6 V, and Ta = 25ºC).

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
VUVLO operation voltage	V_{UVLO1}	Apply to VDD VUVLO[1:0]=00	-	2.60	-	V
		Apply to VDD VUVLO[1:0]=01	-	2.90	-	V
		Apply to VDD VUVLO[1:0]=10	-	3.10	-	V
		Apply to VDD VUVLO[1:0]=11	-	3.35	-	V
VUVLO hysteresis voltage	$V_{UVLOHYS}$	-	0.05	0.10	0.15	V
Thermal shutdown temperature (Design target)	T_{TSD}	-	120	150	-	ºC

17.5. **LDO Characteristics**

(Unless otherwise specified, VDD = 3.6 V, and Ta = 25ºC)

Characteristics		Symbol	Condition		Min	Typ.	Max	Unit
LDO1	Output voltage accuracy	V_{OUT7}	0 to I_{OUT7} (max)		-3	-	+3	%
	Maximum of output current	I_{OUT7}	-		300	-	-	mA
	Resistance for Active discharge	R_{DLDO1}	-		320	400	480	Ω
LDO2	Output voltage accuracy	V_{OUT8}	0 to I_{OUT8} (max)		-3	-	+3	%
	Maximum of output current	I_{OUT8}	-		350	-	-	mA
	Resistance for Active discharge	R_{DLDO2}	-		320	400	480	Ω
LDO3	Output voltage accuracy	V_{OUT9}	0 to I_{OUT9} (max)		-3	-	+3	%
	Maximum of outpcurrent	I_{OUT9}	-		120	-	-	mA
	Resistance for Active discharge	R_{DLDO3}	-		-	400	-	Ω
	Feedback Regulation Voltage	V_{FBLDO3}	-		1.164	1.200	1.236	V
Ripple rejection LDO1-3		R_R	Vinput = 0.2 Vpp IOUT = 100 mA Design target	f = 1kHz	-	60	-	dB
				f = 10 kHz	-	40	-	
Noise of LDO1		-	Vout=1.8 V, 10 Hz to 100 kHz, Cout = 4.7 µF, Iout = 200 mA Design target		-	110	-	µVrms
Noise of LDO2		-	Vout = 2.8 V, 10Hz to 100 kHz, Cout = 4.7 µF, Iout = 200 mA Design target		-	130	-	µVrms
Noise of LDO3		-	Vout = 1.8 V, 10 Hz to 100 kHz, Cout = 4.7 µF, Iout = 100 mA Design target		-	110	-	µVrms

17.6. **DCDCn Converter Characteristics**

(Unless otherwise specified, VDD=3.6V, and Ta=25ºC)

Characteristics			Symbol	Condition	Min	Typ.	Max	Unit
DCDCn	Output voltage accuracy		V_{OUT1}	PWM mode(Design target)	-2	-	+2	%
			$V_{OUT2,3,4}$	PWM mode(Design target)	-3	-	+3	%
	Output current DC		I_{OUT1}	-	-	1.5	1.8	A
			I_{OUT2}	-	-	1.0	1.2	
			I_{OUT3}	-	-	0.8	0.96	
			I_{OUT4}	-	-	0.5	0.6	
	Output current AC transient		I_{OUT1AC}	-	-	-	3.5	A
			I_{OUT2AC}	-	-	-	1.5	
			I_{OUT3AC}	-	-	-	1.5	
			I_{OUT4AC}	-	-	-	1.0	
	High side current limited(OCL)		I_{LMT1}	-	3.5	-	-	A
			I_{LMT2}	-	2.0	-	-	
			I_{LMT3}	-	2.0	-	-	
			I_{LMT4}	-	2.0	-	-	
	Discharge Resistance for Active discharge		R_{DDC1}	-	160	250	340	Ω
			R_{DDC2}	-	160	250	340	Ω
			R_{DDC3}	-	160	250	340	Ω
			R_{DDC4}	-	160	250	340	Ω
	DCDC4 Feedback Regulation Voltage		V_{FBDC4}	-	1.164	1.200	1.236	V
	Switching frequency		F_{PWM}	-	0.8	1.0	1.2	MHz
	Soft start time	DCDC1 DCDC2 DCDC3 DCDC4	-	-	-	680	-	µs
FET on-resistance	DCDC1		R_{DSON1}	High-side (VDD1 to LX1)	-	110	-	mΩ
				Low-side (LX1 to PGND1)	-	70	-	mΩ
	DCDC2		R_{DSON2}	High-side (VDD2 to LX2)	-	180	-	mΩ
				Low-side (LX2 to PGND2)	-	170	-	mΩ
	DCDC3		R_{DSON3}	High-side (VDD3 to LX3)	-	280	-	mΩ
				Low-side (LX3 to PGND3)	-	200	-	mΩ
	DCDC4		R_{DSON4}	High-side (VDD4 to LX4)	-	280	-	mΩ
				Low-side (LX4 to PGND4)	-	210	-	mΩ

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17.7. **LED Driver Characteristics**

(Unless otherwise specified, VDD=3.6V, and Ta=25ºC)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Switching Frequency	f_{SW}	-	0.8	1.0	1.2	MHz
Maximum Duty Cycle		-	90	-	-	%
PWM dimming Frequency		I^2C Controlled PWM Dimming	157	195	234	Hz
LEDn Regulation Voltage		10 mA < ILED < 80 mA	-	0.4	-	V
Trans conductance	gM	Design target	-	0.1	-	μS
SW On Resistance	R_{SW_ON}	-	-	200	300	mΩ
SW Leakage Current	I_{SW_leak}	V_{SW} = 20 V	-	-	4	μA
SW current limit	I_{SW_lim}	Peak current	1.0	-	-	A
ISET terminal voltage		-	-	1.24	-	V
Channel to Channel Matching		ILEDn = 20 mA	-	-	±3	%
		ILEDn = 80 mA, Design target	±2			%
ILED Current Accuracy		ILEDn = 20 mA, Ta = 25°C	-	-	±1	mA
		ILEDn = 20 mA, Ta = -40 to 85°C	-	-	±1.5	mA
		ILEDn = 80 mA, Ta = -40 to 85°C Design target	±4			mA
OSD (LED Short Detection) Threshold		-	-	5.0	-	V
OOD (LED Open Detection) Threshold		-	-	0.2	-	V
FB_LED terminal input current		-	-	0	-	μA
FB_LED terminal Over voltage detecting Threshold	VOUT	Output rising	1.19	1.228	1.266	V
FB_LED terminal Over voltage Hysteresis		-	-	70	-	mV

17.8. **Charger Characteristics (1)**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Input voltage	DCIN	-	4.3	-	5.5	V
Input DUVLO voltage	$V_{UVLODCIN}$	DCIN rising	3.45	3.60	3.75	V
		DCIN falling	3.35	3.50	3.65	V
Input OVP voltage	$V_{OVPDCIN}$	DCIN rising (no glitch filter)	5.65	5.80	5.95	V
		DCIN falling	-	5.65	-	V
Detect voltage threshold accuracy of DCIN falling in charging	V_{CLACC}	ATLMTT[]1:0]=01	-4	-	+4	%
Battery OVLO voltage	V_{BOV}	N=4,3,2,1	-	VFLT+ 0.05*N	-	V
Automatic shutdown threshold	V_{ASHDN}	DCIN - VBAT, DCIN rising (Recover)	87.5	125.0	162.5	mV
		DCIN - VBAT, DCIN falling(Detection)	20	40	60	mV
DCIN current (Active)	$I_{DCIN-ACTIVE}$	Charging, not including ICHG, PWM	-	2.5	-	mA
DCIN shutdown current	$I_{SHDNDCIN}$	Charging invalid DCIN = 5 V, VBAT = 3.7 V, no load, DCIN>DUVLO, Main Standby mode	-	0.6	-	μA
VS terminal Shutdown current	I_{SHDNVS}	Charging invalid DCIN = open, VBAT = 3.7 V	-	0	2	μA
DCIN Reverse current	I_{DCINLK}	DCIN current when charging is forbidden. DCIN = 0 V, VBAT = 4.2 V	-	-	2	μA
Over-temperature status threshold, Charge block	T_{OVT}	-	110	130	-	°C
Over-temperature status threshold hysteresis, Charge block	T_{OVT_HYS}	-	-	10	-	°C

Test condition is only 25 °C

17.9. **Charger Characteristics (2) SW-mode Controller**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
FET on-resistance	$R_{DSONCHG}$	High-side (DCIN to LX6),	-	233	367	mΩ
		Low-side (LX6 to PGND6),	-	125	200	mΩ
Duty cycle	D.C.	Maximum, High side ON Duty	-	100	-	%
		Minimum, High side ON Duty	-	0	-	%

Test condition is only 25 °C

17.10. **Charger Characteristics (3) Battery Charger**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Trickle charge to Pre-charge voltage threshold	$V_{TRICKLECHG}$	-	1.90	2.05	2.20	V
Trickle charge current accuracy	$I_{TRICKLECHG}$	VBATT = 1.7 V. Percentage of Pre-charge Current PCI[1:0]	-	50	-	%
Pre-charge to fast charge voltage threshold accuracy	V_{PRECHG}	CCVTH[2:0] =100 (CCVTH = 2.9 V)	-3.5	-	3.5	%
Constant current sense voltage	V_{SENSE}	IPRECHG = 100 mA	-	6.8	-	mV
		IFCHG = 1000 mA	-	68	-	mV
Pre-charge current (Programmable 75mA to 400mA)	I_{PRECHG}	RSENSE = 68 mΩ, IPRECHG = 400 mA,	-80	-	80	mA
Fast charge current (Programmable 400mA to 1500mA)	I_{FCHG}	RSENSE = 68 mΩ, IFCHG = 500 mA,	-50	-	50	mA
Charge termination current (Programmable 50mA to 200mA)	I_{TERM1}	RSENSE = 68 mΩ, IFCHG = 100 mA	-30	-	30	mA
Float voltage accuracy (Programmable 4.10V to 4.25V,50mV/step)	V_{FLT}	VFLT = 4.2 V, ICHG = 150 mA	-1	-	1	%
Automatic Re-charge threshold voltage	V_{RECH}	0x0B (ATRCHGTH) setting	-	150	-	mV
			-	300	-	mV

Test condition is only 25 °C

17.11. **Charger Characteristics (4) Thermal Monitor (Factory Programmable Option)**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
High temperature trip point(65°C)	VHOT1	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH falling	34.10	35.23	36.35	$\%V_{TH_REF}$
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k, TH falling	28.28	29.46	30.64	
High temperature trip point(60°C)	VHOT2	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH falling	37.54	38.78	40.02	
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k, TH falling	32.04	33.38	34.72	
High temperature trip point(50°C)	VHOT3	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH falling	45.09	46.58	48.07	
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k, TH falling	40.62	42.31	44.01	
High temperature trip point(45°C)	VHOT4	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH falling	49.13	50.75	52.38	
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k,TH falling	45.36	47.25	49.14	
Low temperature trip point(10°C)	VCOLD1	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH rising	77.84	79.67	81.51	
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k, TH rising	79.48	81.52	83.56	
Low temperature trip point(0°C)	VCOLD2	Rth = 10k NTC(10 kΩ@25°C B:3435), Rs = 4.7k, TH rising	84.31	85.94	87.58	
		Rth = 100k NTC(100 kΩ@25°C B:4100), Rs = 47k, TH rising	86.56	88.24	89.91	
NTC thermistor temperature hysteresis	I_{NTCHYS}	Rth = 100k NTC	-	2	-	ºC
		Rth = 10k NTC	-	2	-	ºC
Discharge resister in High temperature trip	-	-	-	45	-	Ω

Test condition is only 25 °C

17.12. **Power Path**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
FET on-resistance	-	DCIN to VSYS	-	220	-	mΩ
DPPM mode set threshold	-	VBAT > 2.5 V	-	VBAT -30mV	-	V
DPPM mode unset threshold	-	VBAT > 2.5 V	-	VBAT -10mV	-	V
FET on-resistance	-	VBAT to VSYS	-	45	-	mΩ
Q3 current limit	-	VBAT to VSYS	2.5	-	3.7	A
DCIN current limit	-	USBILMT[3:0] = 0001	-	90	-	mA
	-	SDP connection	400	450	500	
	-	DCP connection	1200	1350	1500	

Test condition is only 25 °C

17.13. **Automatic Power Source Detection (DP/DM)**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Data detect voltage	V_{DAT_REF}	-	0.25	0.33	0.40	V
D + source voltage	V_{DP_SRC}	-	0.50	0.60	0.70	V
D-source voltage	V_{DM_SRC}	-	0.50	0.60	0.70	V
D+ pull-up voltage	V_{DP_UP}	-	3.0	3.3	3.6	V
Logic threshold	V_{LGC}	-	0.8	1.2	2.0	V
D+ sink current	I_{DP_SINK}	-	25	100	175	μA
D-sink current	I_{DM_SINK}	-	25	100	175	μA
Current source for data connect detection	I_{DP_SRC}	-	7	10	13	μA
Data line leakage resistance	R_{DAT_LKG}	-	300	-	-	kΩ
D-pull-down resistance	R_{DM_DOWN}	-	14.25	20.0	24.80	kΩ

Test condition is only 25 °C

17.14. **Power Source Detection**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Data connect detection debounce	t_{DCD_DBNC}	-	10	-	-	ms
Data connect time out	$t_{DCD_TIMEOUT}$	-	300	-	-	ms
DP source on time	t_{VDPSRC_ON}	-	40	-	-	ms
DM source on time	t_{VDMSRC_ON}	-	40	-	-	ms

Test condition is only 25 °C

17.15. **Oscillator**

(Unless otherwise specified, VIN = 5.0 V, VFLOAT = 4.2 V, VBAT = 3.7 V, Ta = 0 to 60°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Oscillator frequency	f_{OSC}	-	0.8	1.0	1.2	MHz
Timer frequency	f_{TM}	-	80	100	120	kHz
Pre-charge time out	t_{PCTOFC}	Safety timer(Default)	24	30	36	min
Complete charge timeout	t_{CTOFC}	Safety timer(Default)	384	480	576	min
Unconnected battery timer	t_{BATMIS}	-	65	86	105	ms

Test condition is only 25 °C

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17.16. **Logic Inputs/Outputs**

(Unless otherwise specified VDD = 3.6 V, and Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Input low level	V_{IL}	SDA,SCL,LEDD_EN terminal	-	-	600	mV
Input high level	V_{IH}	SDA,SCL,LEDD_EN terminal	1.4	-	-	V
output low level	V_{OL}	INT,SDA,PGOOD terminal ISINK = 3 mA	-	-	300	mV
leakage current	I_{LK}	INT,SDA,PGOOD terminal V_{BIAS} = 3 V	-	-	1	μA
VREF Output Voltage	V_{REF}	-	-	1.5	-	V
PB “Hard Reset Detect” time	t_{HRST}	Not tested in production	-	8	-	s
PB deglitch time	t_{PBDG}	Not tested in production	-	50	-	ms
PB internal pull-up resistor	$R_{PBPULLUP}$	-	-	100	-	kΩ
PGOOD comparator threshold	V_{PGD}	Output voltage falling, % of set voltage LDO1 to 3, DCDC1 to 4	-	90	-	%
	V_{PGR}	Output voltage rising, % of set voltage LDO1 to 3, DCDC1 to 4	-	95	-	%
PGOOD deglitch time	t_{PGDG}	Output voltage falling DCDC1 to 4	2	-	4	ms
		Output voltage falling LDO1 to 3	1	-	2	ms
PGOOD delay time	t_{PGDLY}	PGDLY[1:0]=00	-	20	-	ms
		PGDLY[1:0]=01	-	100	-	ms
		PGDLY[1:0]=10	-	200	-	ms
		PGDLY[1:0]=11	-	400	-	ms

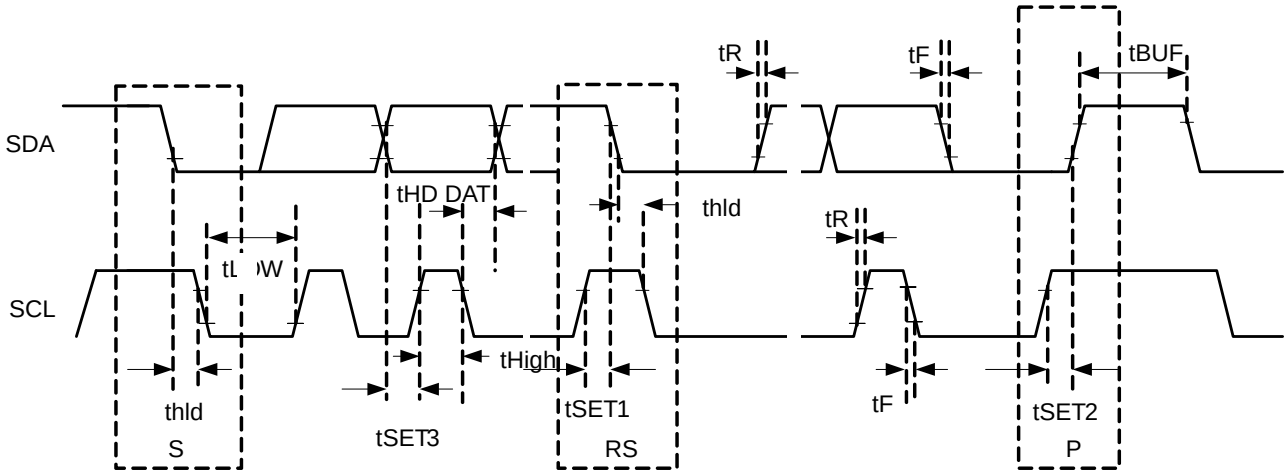
17.17. **AC Characteristics for I^2C**

(Unless otherwise specified VDD = 3.6 V, and Ta = 25°C)

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
SCL Clock Frequency	fSCL	C_L = 400 pF	-	-	400	kHz
Set-up time START condition	Thld	C_L = 400 pF	0.6	-	-	μs
Hold time START condition	tSET1	C_L = 400 pF	0.6	-	-	μs
Set-up time STOP condition	tSET2	C_L = 400 pF	0.6	-	-	μs
Data Set-up time	tSET3	C_L = 400 pF	100	-	-	ns
Data Hold time	tBUF	C_L = 400 pF	1.3	-	-	μs
LOW period of the SCL clock	tLOW	C_L = 400 pF	1.3	-	-	μs
High period of the SCL clock	tHigh	C_L = 400 pF	0.6	-	-	μs
Rise time of both SDA and SCL signals	tR	C_L = 400 pF	-	-	300	ns
Fall time of both SDA and SCL signals	tF	C_L = 400 pF	-	-	300	ns
Bus free time between a STOP and START condition	tHD DAT	C_L = 400 pF	0	-	-	μs

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Figure: 32 Definition of timing chart on the I^2C

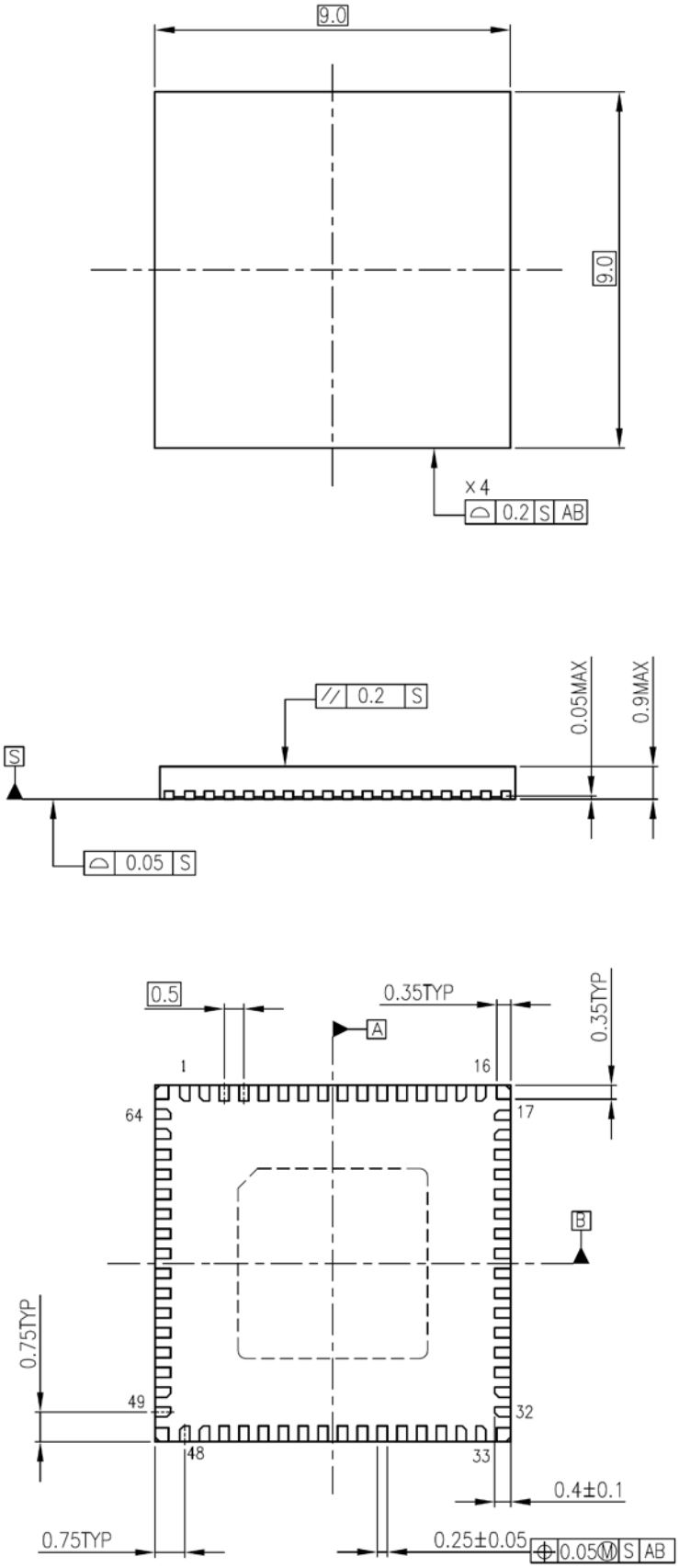


S: Start, RS: Repeat start, P: Stop

18. Package dimensions

P-VQFN64-0909-0.50-001

Unit: mm



Weight: 0.192 g (Typ.)

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