TCK321/2/3G series EVALUATION KIT user's guide

1. Introduction

The TCK321/2/3G EVALUATION KIT (EVK) helps designers evaluate the performance of the TCK32 series. Passive components and jumper are included in the EVK to evaluate easily. For the specification of the TCK321/2/3G, it is described in the data sheet. Please refer to it in conjunction with user guide.

Table 1-1 TCK32 series line up

Part number	package	VIN	IOUT	OVLO level	Input priority	Flag Operation	
						Monitored Input	Active Indication Level
TCK321G	WCSP16C	36V	2A	12.0V	VINA	VINA	Low
TCK322G				15.0V	VINA	VINA	Low
TCK323G				15.0V	VINA	VINB	Low

Table 1-2 Board Specification

Content	Specification
Board size	45.72 x 66.04 mm (17 x 26 inch), t:1.6 mm
Copper foil	Double-sided board (18μm)
Quality of the material	Glass epoxy (FR-4)

Usage Precautions

・The input voltage, output voltage, output current and temperature conditions should be considered when selecting capacitors, inductors and resistors. These components should be evaluated on an actual system prototype for best selection.

・ Parts of this product in the surrounding are examples of the representative, and the supply might become impossible. Please confirm latest information when using it.

Safety Precautions

・Do not touch the components and the device while the power is supplied. Contact to it may result in a burn or electrical shock.

・Do not touch the lead tips of a device. Some devices have leads with sharp tips. Contact to sharp tips may result in a puncture wound.

2. Schematic and BOM list

The schematic, Board Specification and BOM list for this EVK are shown in Fugure2-1 and Table2-1. Please refer to 3. SET UP for pin connection.

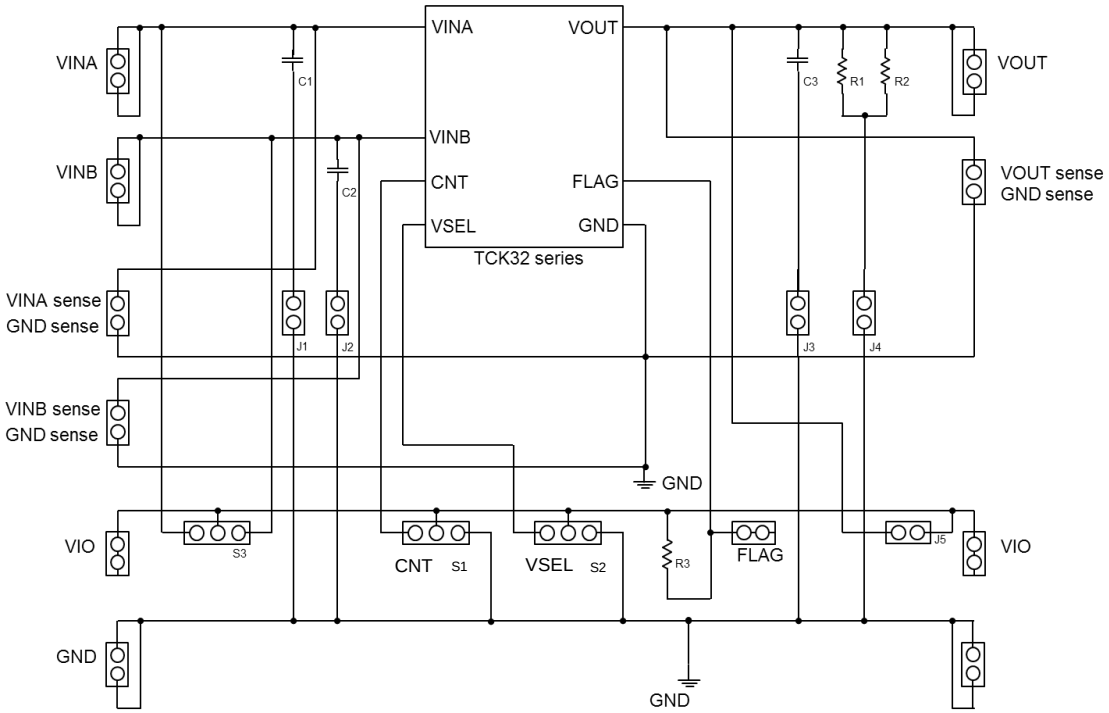

Figure 2-1 TCK321/2/3G EVK Schematic

Table 2-1 BOM list

Reference design	Value	Description	Size
C1, C2	1μF	Capacitor, 50V	3.2 x 1.6 mm
C3	1μF	Capacitor, 16V	1.6 x 0.8 mm
R1, R2	100Ω	Resistor, 5% 1/3W	3.2 x 1.6 mm
R3	10kΩ	Resistor, 1% 1/10W	1.6 x 0.8 mm
VINA/B, VOUT, GND, VIO, FLAG	-	Terminal, 2pin	-
VINA/B sense VOUT sense, GND sense	-	Terminal, 1pin	-
J1 to J5	-	Jumper, 2pin	2.54mm pitch
S1 to S3	-	Jumper, 3pin	2.54mm pitch
U1	-	IC, (TCK321/2/3G)	WCSP16 package
NA	NA	Shorting jumper (cap)	2.54mm pitch

3. Setup

This section describes how to properly set up and handling the jumper on the EVK. Please refer to the data sheet for test conditions.

INPUT (VINA, VINB)

VINA and VINB terminal are the input source connection. Connect the positive connection to the VINA or VINB terminal and the negative connection to the GND.

OUTPUT (VOUT)

VOUT terminal is the output connection of the EVK. Connect the positive connection of the load to the VOUT terminal and the negative connection to the GND terminal.

OUTPUT (FLAG)

FLAG terminal is the output connection to output flag signal depend on VIN level. FLAG terminal is pulled up to the VIO through R3.

VINA sense, VINB sense, VOUT sense and GND sense

These four terminals are used to measure the input or output voltage accurately by correcting the drop voltage of parasitic resistor. When the on resistance from VINA to VOUT is measured, it is calculated measuring the potential difference between VINA and VOUT sense terminal without influence of parasitic resistant.

S1 (CNT)

S1 terminal is used to select the input voltage of CNT. CNT pin in the center of S1 is connected to the device. Hi pin on the left side of S1 is connected to VIO terminal. Lo pin on the right side of S1 is connected to GND. Place a shorting jumper across Hi or Lo pin and CNT pin of S1 to select the operating state. Also, it is available even if CNT pin is left floating because it is internally connected to GND (Pull-down). In addition, it is possible to control operation by connecting CNT pin and a control signal source.

S2 (VSEL)

S2 terminal is used to select the input voltage of VSEL. VSEL pin on the center of S2 connected to the device. Hi pin on the left side of S2 is connected to VIO. Lo pin on the right side of S2 is connected to GND. Place a shorting jumper across the Hi or Lo pin and VSEL pin of S2 to select the operating state. Also, it is available even if VSEL pin is left floating because it is internally connected to voltage generator (Pull-up). In addition, it is possible to control operation by connecting VSEL pin and a control signal source.

VIO

VIO terminal is used to set the pull-up voltage of CNT, VSEL, and FLAG. The pull-up voltage is set to use an external power source. Or set to the same potential as VINA, VINB, or VOUT by shorting S3 or J5. VIO terminal is connected to Hi pin of S1to S2, a pin on the center of S3 and R3.

4. Operation / Test result

4-1 On resistance (Ron)

This section describes RON measurement. Figure 4-1 shows a test setup for measuring on resistance. On resistance can be calculated IOUT and measurement result of the potential difference between VIN and VOUT sense.

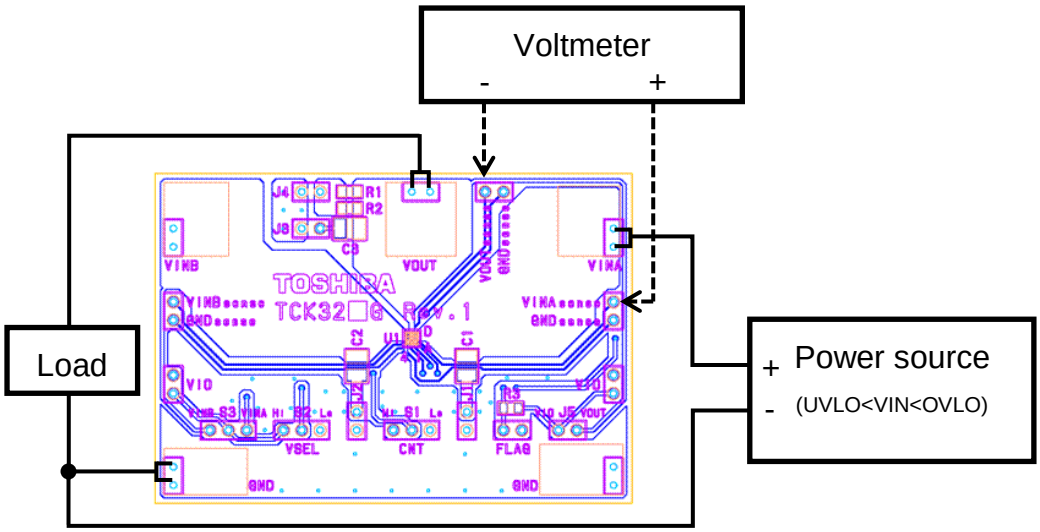

Figure 4-1 test circuit for RON

4-2 Output response (Auto select mode)

This section describes output response evaluation. TCK321/2/3G is equipped with two output response modes (manual select mode and Auto select mode). For details of each mode, please refer to application note and 4.4. Figure 4-2 shows a test setup.

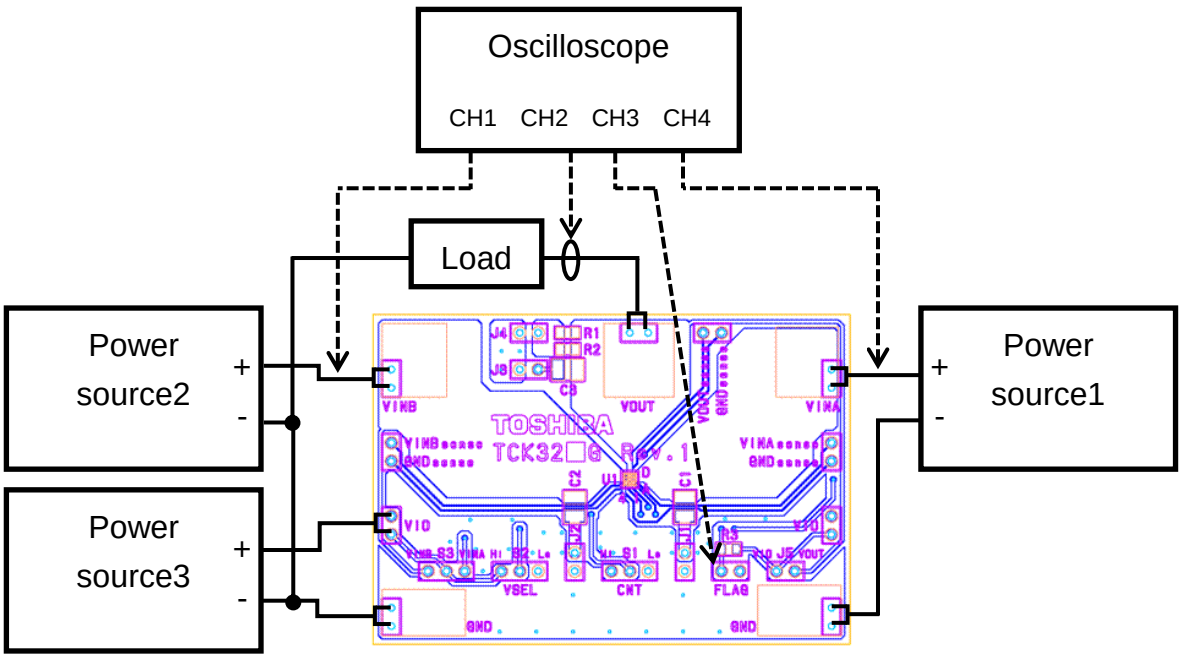

Figure 4-2 test circuit for Output response

5. Board Layout

This section provides the TCK321/2/3G EVK board layout.

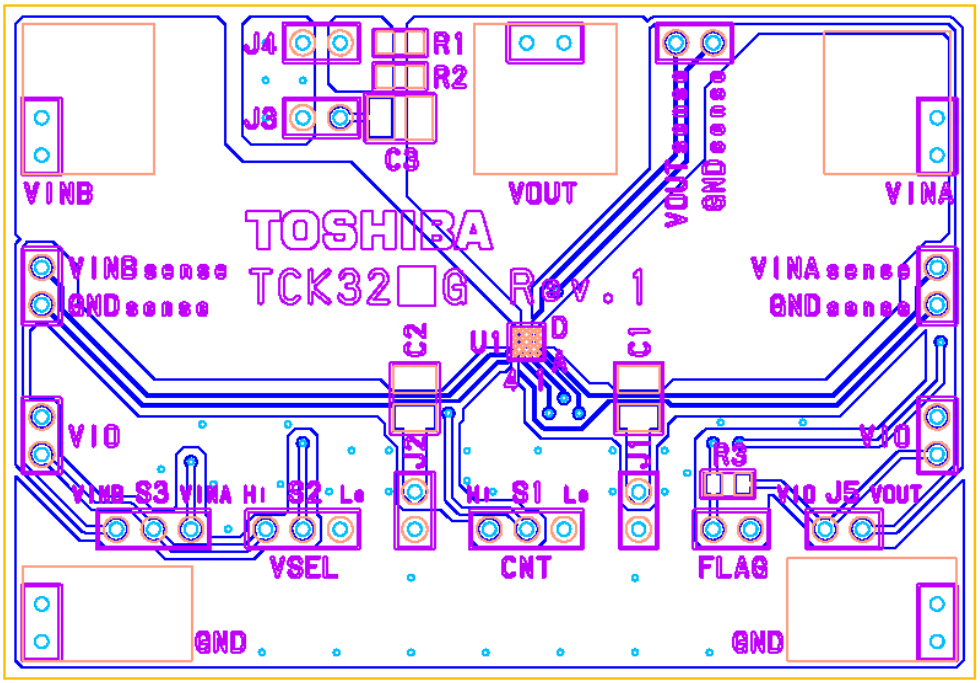

Figure 5-1 Top layer

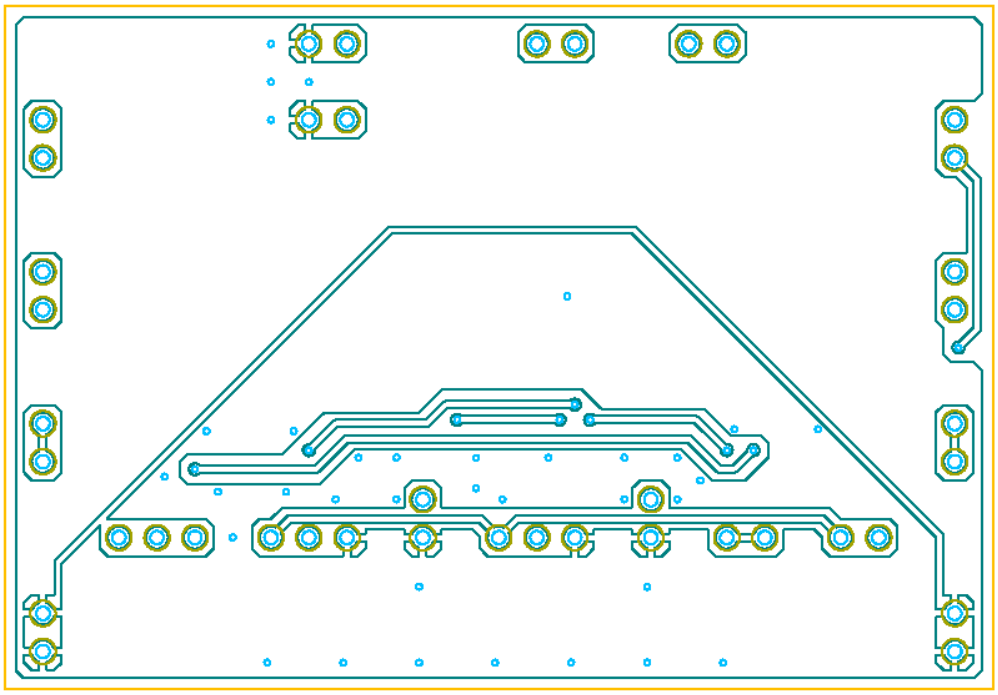

Figure 5-2 Bottom layer

PCB Layout Guideline

・All traces should be as short as possible to reduce influence of parasitic components.

・Capacitor of CIN and COUT must be placed as close as possible to the IC for stable power supply.

・It is possible to reduce the influence of parasitic and thermal impedance by taking widely IN, VOUT, and GND traces.

・It is possible to reduce the noise influence of the return current by dividing the power and small signal GND.

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