TOSHIBA
Leading Innovation

Jan, 2015

Product Types

TOSHIBA Microcontrollers TX03 series
TMPM367FDFG TMPM367FDXBG TMPM368FDFG TMPM368FDXBG
TMPM369FDFG TMPM369FDXBG TMPM36BFYFG TMPM36BF10FG

Restrictions on use of the DMA function

This is to inform you of restrictions on use of the DMA function.
If you need any further information, please contact your local Toshiba sales representative.

【Description】

When the synchronous serial interface (SSP) or the asynchronous serial communication circuit (UART) is used to transmit data or receive data, the following problem may occur:

At transmission: A part of communication data may be lost (the FIFO buffer may overflow).
At reception : Unnecessary data may be transferred (the FIFO buffer may underflow)

【Conditions】

The table below lists the peripheral functions that are connectable at DMA transfer. When the SSP<ch4 to 9> or UART<ch10 to 13> are used, if single-transfer is enabled (The connection channel of DMAxChnlUseburstSet is set to 0), the problem may occur.

Ch	Peripheral circuit	TMPM367FDFG TMPM367FDXBG TMPM368FDFG TMPM368FDXBG TMPM369FDFG TMPM369FDXBG	TMPM36BFYFG TMPM36BF10FG	Ch	Peripheral circuit	TMPM367FDFG TMPM367FDXBG TMPM368FDFG TMPM368FDXBG TMPM369FDFG TMPM369FDXBG	TMPM36BFYFG TMPM36BF10FG
0	ADC conversion completion	—	○	16	SIO/UART1 reception	○	○
	ADC A conversion completion	○	—	17	SIO/UART1 transmission	○	○
1	ADC B conversion completion	○	—	18	SIO/UART2 reception	○	○
2	DAC0 conversion trigger	○	—	19	SIO/UART2 transmission	○	○
3	DAC1 conversion trigger	○	—	20	SIO/UART3 reception	○	○
4	SSP0 reception	○	○	21	SIO/UART3 transmission	○	○
5	SSP0 transmission	○	○	22	I2C/SIO0 transmission/reception	○	○
6	SSP1 reception	○	○	23	I2C/SIO1 transmission/reception	○	○
7	SSP1 transmission	○	○	24	I2C/SIO2 transmission/reception	○	○
8	SSP2 reception	○	○	25	TMRB0 compare match	○	○
9	SSP2 transmission	○	○	26	TMRB1 compare match	○	○
10	UART4 reception	○	○	27	TMRB2 compare match	○	○
11	UART4 transmission	○	○	28	TMRB3 compare match	○	○
12	UART5 reception	○	○	29	TMRB4 compare match	○	○
13	UART5 transmission	○	○	30	DMA request pin	○	○
14	SIO/UART0 reception	○	○	31	Software trigger	○	—
15	SIO/UART0 transmission	○	○	○: Connectable peripheral circuit —: Not supported			

【Explanation】

At transmission:

Under the following circumstance, one additional DMA request may occur compared with the number of unused data space of the FIFO of the SSP or UART. Therefore, DMA transfer is executed even if the FIFO is full and the FIFO overflow occurs.

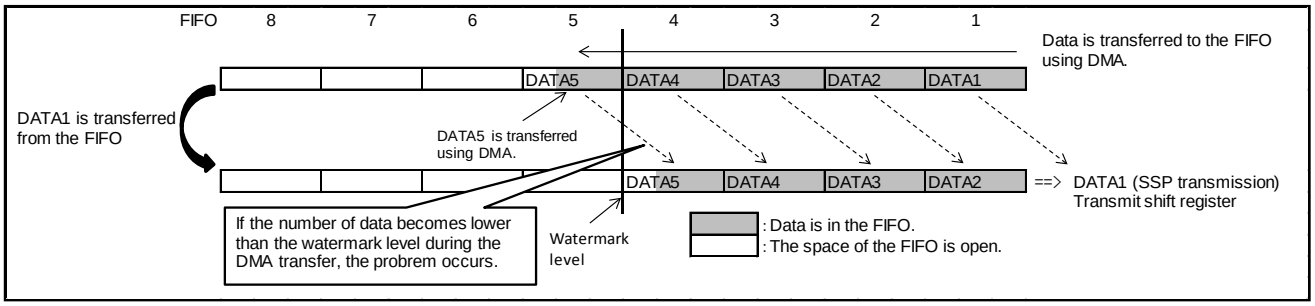
- The number of data of the FIFO becomes lower than the watermark level while the DMA is transferring data to the FIFO.

At reception:

Under the following circumstance, one additional DMA request may occur compared with the number of stored data. Therefore, invalid data is transferred from the FIFO of the SSP or UART and the FIFO underflow occurs.

- The number of data of the FIFO becomes higher than the watermark level while the DMA is tranferring data from the FIFO of the SSP or UART.

<Example of relationship between the condition of the FIFO and the watermark level>
(SSP transmission)



* Wartermark level:

SSP transmission: Fixed to 4

UART transmission: Full level of UARTxIFLS<RXIFSEL[2:0]> or <TXIFSEL[2:0]>

【Workaround】

When the DMA function is used, set “1” to the corresponding channel of DMAxChnlUseburstSet (single-transfer is prohibited)

However, there are several conditions and restrictions.

Note) These conditions and restrictions vary depending on transmission or reception.

1. At transmission

   When single-transfer is prohibited, arbitration setting is subject to a constraint. According to the number of transfers, select the appropriate method below:

   a) When the number of transfers is a multiple of the watermark level of the FIFO.

      Set the arbitration rates to the watermark level of the FIFO. After the number of specified transfers is complete, arbitration for the priorities between the peripheral functions that are connected to the DMA controller unit is issued. Therefore, the DMA transfer can be performed at high-speed.
      Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO.

   b) When the number of transfers is not a multiple of the watermark level of the FIFO.

Set the arbitration rates to "after one transfer". This setting can be used in every case. After each transfer is complete, arbitration for the priorities between the peripheral functions that are connected to the DMA controller unit is issued. Therefore, the DMA transfer is performed at slower speed than the case of (a).
Specify "0000" as the arbitration rate setting <R_power> for the control data.

2. At reception

Disable or Enable single-transfer according to the number of transfers of control data <n_minus_1>.

a) When the number of transfers is a multiple of the watermark level.

This setting can be used when the number of transfers is a multiple of the watermark level. For example, the watermark level is n, “n × integer number“ can be set as the number of transfers.
Set “1” (disable the single-transfer) to the corresponding channel of DMAxChnlUseburstSet.
Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO.

b) When the number of transfers is less than the watermark level.

This setting can be used when the number of transfers is less than the watermark level.
Set “0” (enable the single-transfer) to the corresponding channel of DMAxChnlUseburstSet.
Specify "0000" as the arbitration rate <R_power> for the control data.

c) When the number of transfers is other than the above.

This setting can be used when the number of transfers is set to over the watermark level and the setting is not a multiple of the watermark level.
Use “Peripheral scatter-gather” as the transfer mode and combine the two tasks at DMA transfer.

For example, in the case of the number of transfers = (n × watermark) + m

Set Task A to the same as (a).
Disable single-transfer. Set the number of arbitration rates <R_power> for the control data to the watermark level of the FIFO. Set “watermark level × n” as the number of transfers.

Set Task B to the same as (b).
Enable single-transfer. Set “0000” to <R_power>. Set “m” as the number of transfers.

[Example of setting]

The peripheral circuit that performs DMA transfer.		SSP reception
The number of DMA transfers to be set		15 times
Watermark level		4 (Fixed to 4 for SSP communication)
The DMA register setting		DMAxChnlUseburstSet<ch4>=1 : Disable single-transfer
Channel control data setting (Alternative data)	Task A Use the same setting as (a).	<n_minus_1>=0x00B : The number of transfers 4 x 3 = 12 times <R_power>=0011 : Arbitration is issued after four transfers are complete. <next_useburst>=0 : Enables Task B to perform single-transfer <cycle_ctrl>=111 : Peripheral scatter-gather mode
	Task B Use the same setting as (b).	<n_minus_1>=0x002 : The number of transfers 15 – 12 = 3 times <R_power>=0000 : Arbitration is issued after one transfer is complete. <cycle_ctrl>=001 : The transfer ends in basic mode.