

TOSHIBA Transistor Silicon PNP Epitaxial Type

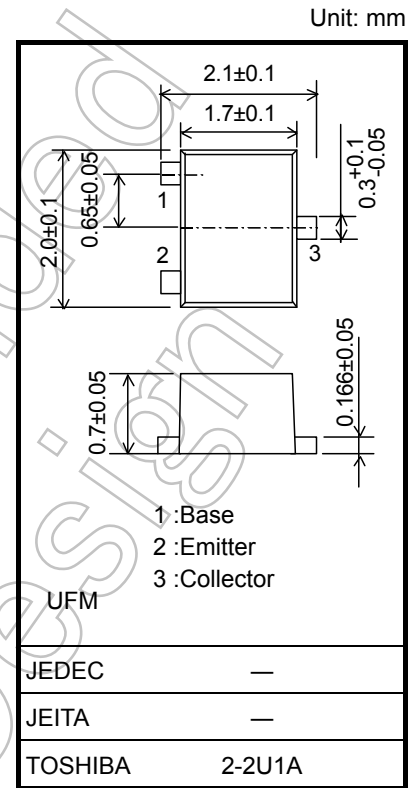
2SA2195

High-Speed Switching Applications
 DC-DC Converter Applications
 Strobe Applications

- High DC current gain: $hFE = 200$ to 500 ($I_C = -0.5$ A)
- Low collector-emitter saturation voltage: $V_{CE(sat)} = -0.2$ V (max)
- High-speed switching: $t_f = 90$ ns (typ.)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	-50	V
Collector-emitter voltage		V_{CEO}	-50	V
Emitter-base voltage		V_{EBO}	-7	V
Collector current	DC	I_C	-1.7	A
	Pulse	I_{CP}	-3.5	
Base current		I_B	-200	mA
Collector power dissipation	P_C	(Note 1)	800	mW
		(Note 2)	500	
Junction temperature		T_j	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$



Weight: 6.6 mg (typ.)

Note 1: Mounted on ceramic board, (25.4mm × 25.4mm × 0.8mm, Cu Pad: 645 mm²)

Note 2: Mounted on FR4 board, (25.4mm × 25.4mm × 1.6mm, Cu Pad: 645 mm²)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
 2007-08

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	$V_{CB} = -50\text{ V}, I_E = 0$	—	—	-100	nA
Emitter cut-off current		I_{EBO}	$V_{EB} = -7\text{ V}, I_C = 0$	—	—	-100	nA
Collector-emitter breakdown voltage		$V_{(BR) CEO}$	$I_C = -10\text{ mA}, I_B = 0$	-50	—	—	V
DC current gain	$h_{FE} (1)$		$V_{CE} = -2\text{ V}, I_C = -0.3\text{ A}$	200	—	500	
	$h_{FE} (2)$		$V_{CE} = -2\text{ V}, I_C = -1.0\text{ A}$	100	—	—	
Collector-emitter saturation voltage		$V_{CE (sat)}$	$I_C = -1.0\text{ A}, I_B = -33\text{ mA}$	—	—	-0.2	V
Base-emitter saturation voltage		$V_{BE (sat)}$	$I_C = -1.0\text{ A}, I_B = -33\text{ mA}$	—	—	-1.1	V
Collector output capacitance		C_{ob}	$V_{CB} = -10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	20	—	pF
Switching time	Rise time	t_r	See Figure 1 circuit diagram.	—	60	—	ns
	Storage time	t_{stg}	$V_{CC} \approx -30\text{ V}, R_L = 30\ \Omega$	—	250	—	
	Fall time	t_f	$I_{B1} = -I_{B2} = -33\text{ mA}$	—	90	—	

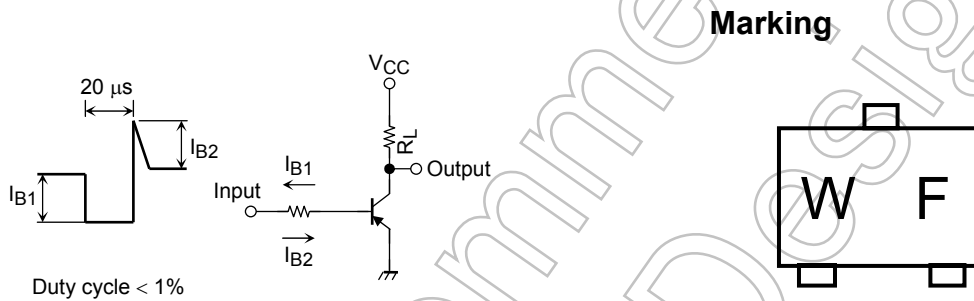
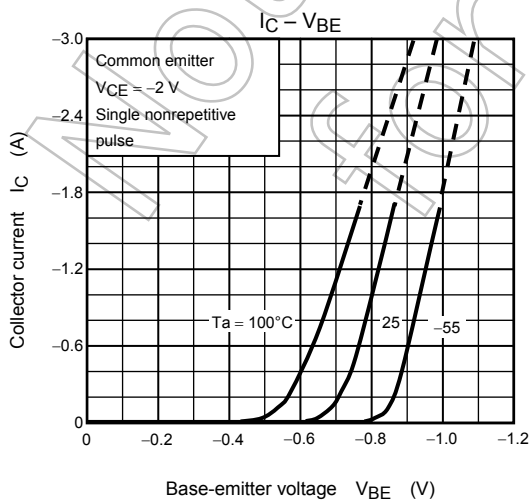
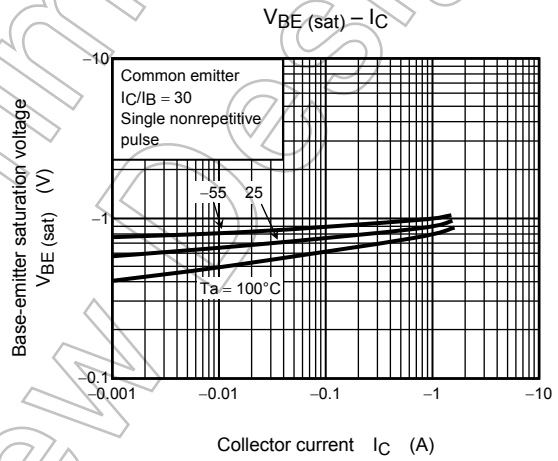
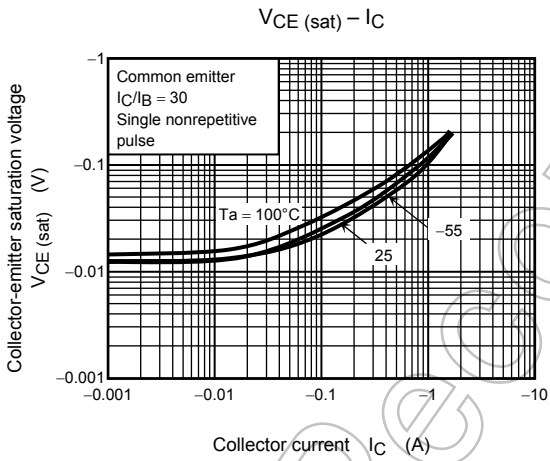
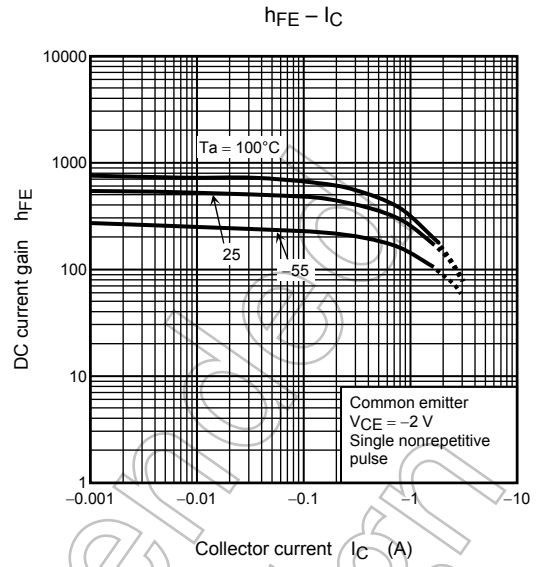
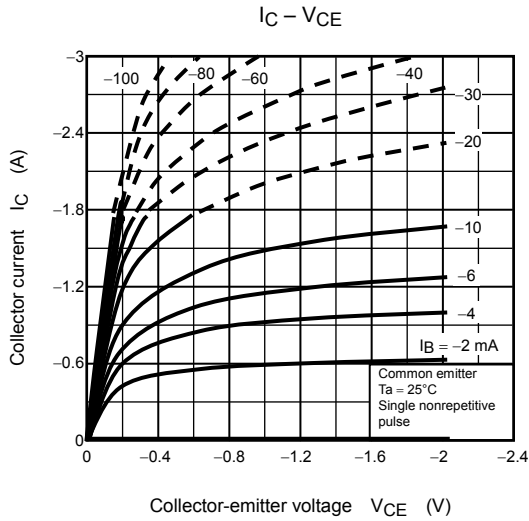


Figure 1 Switching Time Test Circuit & Timing Chart

Not Recommended for New Design



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