TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Π-MOS VII)

SSM6K30FE

- High-speed switching
- O DC-DC Converter
- Small package
- Low RDS (ON): RDS(ON) = 210 m Ω (max) (@VGS = 10 V)
 - $: R_{DS(ON)} = 420 \text{ m}\Omega \text{ (max) (@V_{GS} = 4 V)}$
- High-speed switching: ton = 19 ns (typ.)
 - $\vdots t_{\text{off}} = 10 \text{ ns (typ.)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	ΙD	1.2	Α
	Pulse	I _{DP}	2.4	
Drain power dissipation		P _D (Note 1)	500	(mW
Channel temperature		T _{ch}	150	°C/
Storage temperature		T _{stg}	-55 to 150	°C

1,2±0.05
1,2±0.05
1,2±0.05
1,2±0.05
1,2±0.05
1,2,5,6: Drain
3: Gate
4: Source

ES6

JEDEC

JEITA

TOSHIBA
2-2N1J

Weight: 3 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of

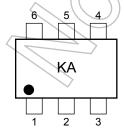
high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

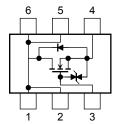
Note 1: Mounted on FR4 board

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm} \text{ (t)}, \text{ Cu pad: } 645 \text{ mm}^2)$

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

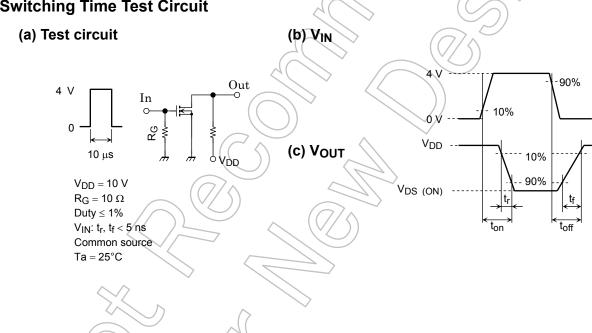
Start of commercial production 2003-04

Electrical Characteristics (Ta = 25°C)

Characteristic Symbol		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Drain-Source breakdown voltage		V (BR) DSS	$I_D = 1$ mA, $V_{GS} = 0$ V	20	_	_	V
Drain cut-off curren	t	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	7	_	1	μΑ
Gate threshold volta	age	V _{th}	V _{DS} = 5 V, I _D = 0.1 mA	11	_	2.3	V
Forward transfer ad	dmittance	Y _{fs}	$V_{DS} = 5 \text{ V}, I_D = 0.6 \text{ A}$ (Note 2)	0.68)/_	_	S
Drain-Source on-resistance		R _{DS} (ON)	$I_D = 0.6 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 2)		145	210	- mΩ
			$I_D = 0.6 \text{ A}, V_{GS} = 4 \text{ V}$ (Note 2)))	260	420	
Input capacitance		C _{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		60	_	pF
Reverse transfer ca	apacitance	C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	17	_	pF
Output capacitance	•	Coss	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	47	/	pF
Switching time	Turn-on time	t _{on}	V _{DD} = 10 V, I _D = 0.6 A,		19	\nearrow	ns
	Turn-off time	t _{off}	$V_{GS} = 0$ to 4 V, $R_G = 10 \Omega$	-6	10	> —	

Note 2: Pulse measurement

Switching Time Test Circuit



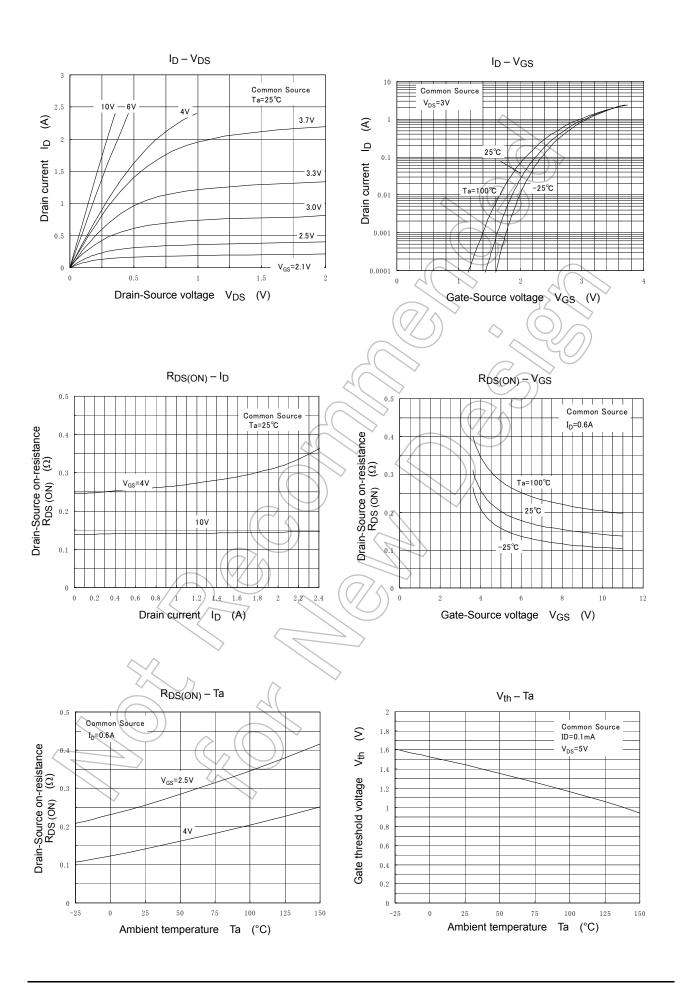
Precaution

 $V_{
m th}$ can be expressed as the voltage between the gate and source when the low operating current value is $I_D = 0.1 \text{ mA}$ for this product. For normal switching operation, $V_{GS (on)}$ requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} . (The relationship can be established as follows:

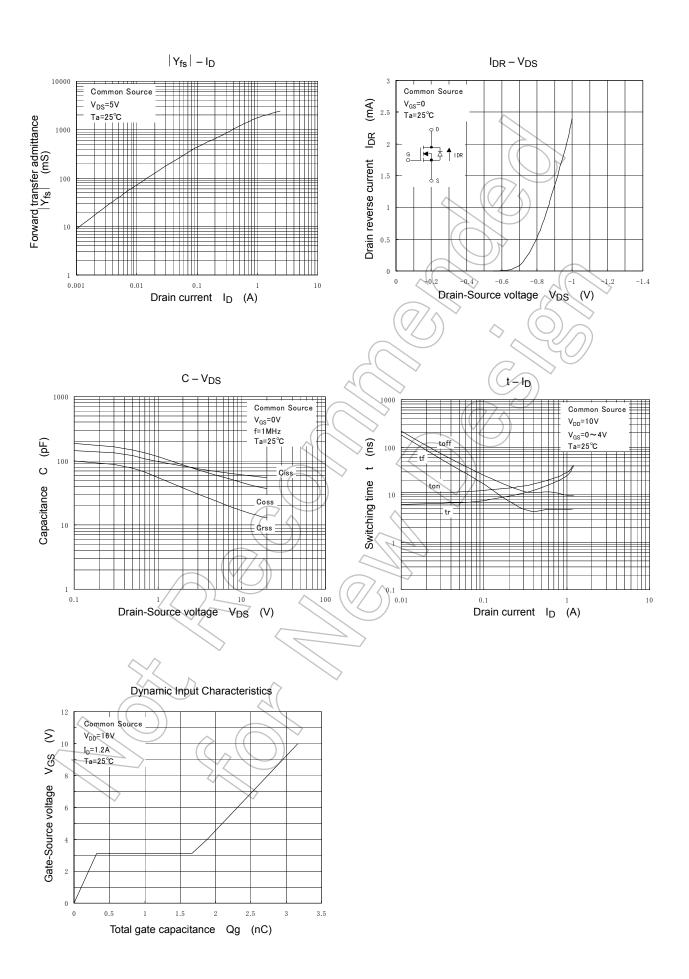
 $V_{GS (off)} < V_{th} < V_{GS (on)}$.)

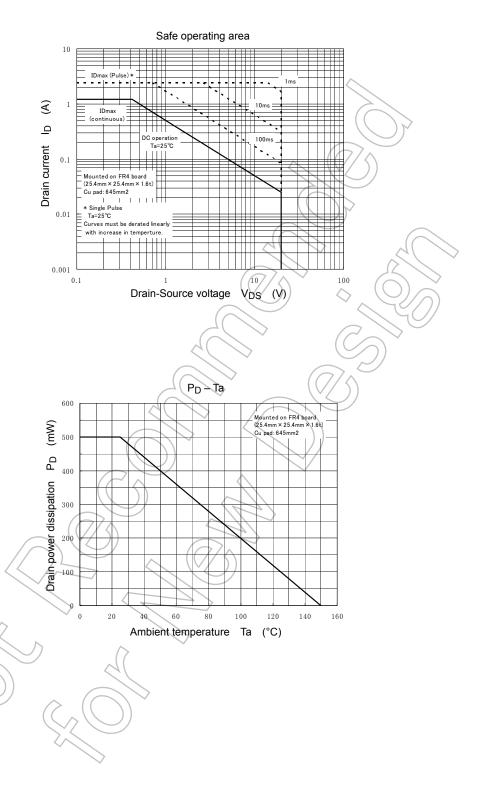
Be sure to take this into consideration when using the device.

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5 2014-03-01

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