

TC7SP57FU, TC7SP58FU

Low Voltage Single Configurable Multiple Function Gate with 3.6-V Tolerant Inputs and Outputs

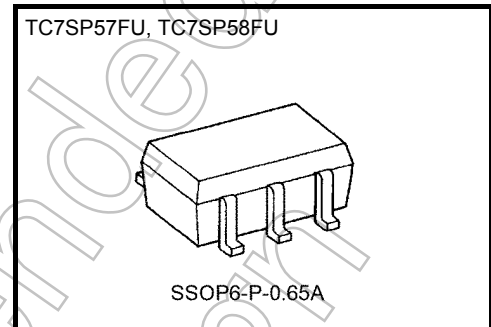
The TC7SP57,58 is a high performance CMOS multiple Function Gate which is guaranteed to operate from 1.2-V to 3.6-V. Designed for use in 1.5 V, 1.8 V, 2.5 V or 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

The output state is determined by seven patterns of 3-inputs.

The user can choose the functions of XNOR(TC7SP57), XOR(TC7SP58), AND, OR, NAND, NOR, Schmitt Inverter, and Schmitt Buffer.

All inputs are equipped with protection circuits against static discharge.

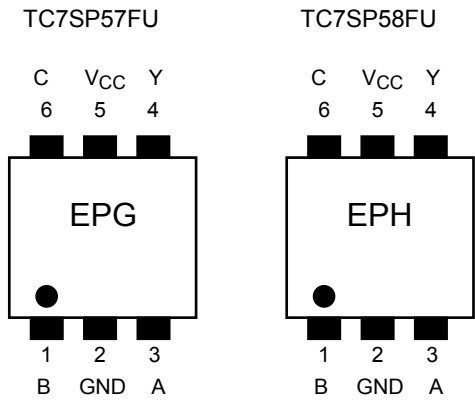


Weight: 0.0068 g (typ)

Features

- Low-voltage operation: $V_{CC} = 1.2$ to 3.6 V
- High-speed operation: $t_{pd} = 8.5$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
 $t_{pd} = 12.0$ ns (max) ($V_{CC} = 2.3$ to 2.7 V)
- Output current: $|I_{OH}| / I_{OL} = 8$ mA (min) ($V_{CC} = 3.0$ V)
 $|I_{OH}| / I_{OL} = 4$ mA (min) ($V_{CC} = 2.3$ V)
 $|I_{OH}| / I_{OL} = 1.5$ mA (min) ($V_{CC} = 1.65$ V)
- Latch-up performance: -300 mA
- ESD performance: Machine model $> \pm 200$ V
Human body model $> \pm 2000$ V
- Package: US6
- Power-down protection is provided on all inputs and outputs

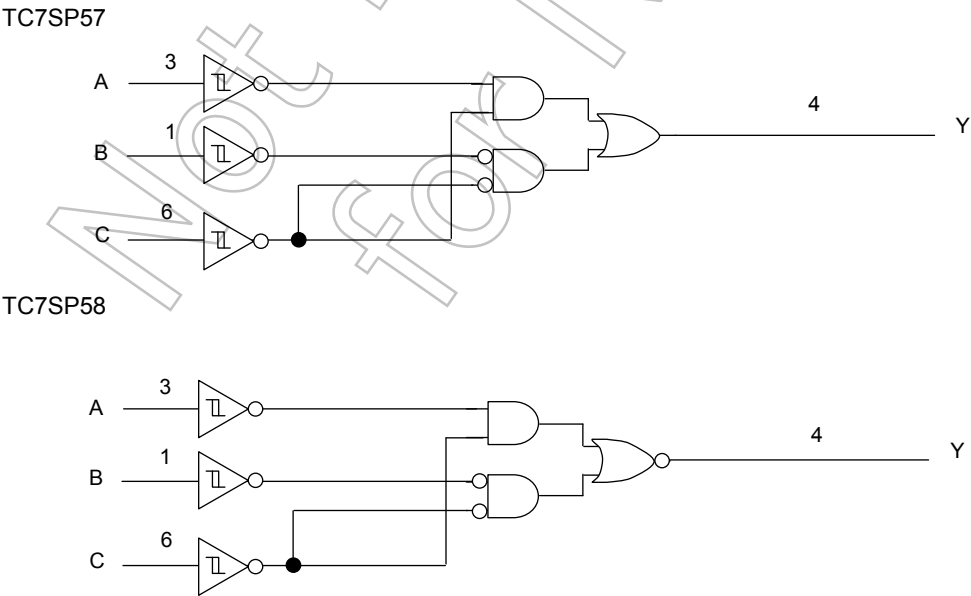
Pin Assignment (top view)



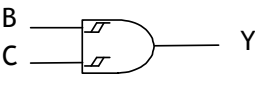
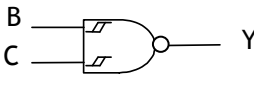
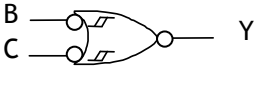
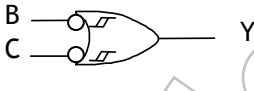
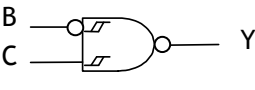
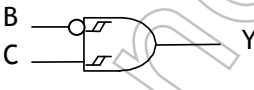
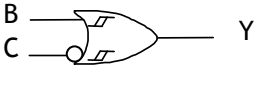
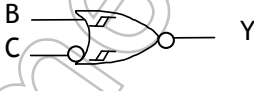
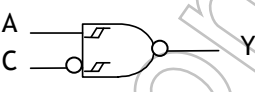
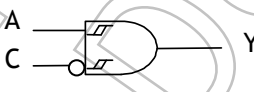
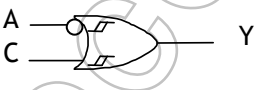
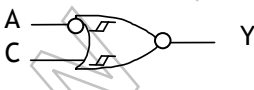
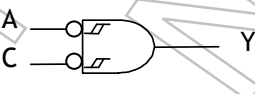
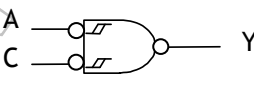
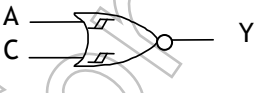
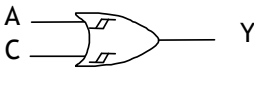
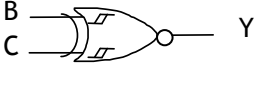
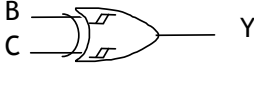
Truth Table

INPUTS			OUTPUT	
			TC7SP57	TC7SP58
A	B	C	Y	Y
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	H	L
H	L	L	L	H
H	L	H	L	H
H	H	L	L	H
H	H	H	H	L

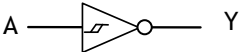

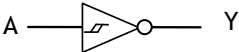


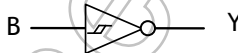

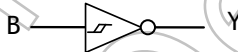
System Diagram



Logic configurations(1/2)

Function	Input Condition	TC7SP57 Logic symbol	TC7SP58 Logic symbol	Function Table																											
SP57 Schmitt AND or Schmitt INV + NOR	A=H-Level B=INPUT C=INPUT Y=OUTPUT	 OR	 OR	<table><tr><th rowspan="2">A</th><th rowspan="2">B</th><th rowspan="2">C</th><th colspan="2">Y</th></tr><tr><th>57</th><th>58</th></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr></table>	A	B	C	Y		57	58	H	L	L	L	H	H	L	H	L	H	H	H	L	L	H	H	H	H	H	L
A		B	C					Y																							
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H	L	L	L	H																											
H	L	H	L	H																											
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SP58 Schmitt NAND or Schmitt INV + OR		 OR	 OR																												
SP57 Schmitt INV +NAND or Schmitt INV +OR	A=L-Level B=INPUT C=INPUT Y=OUTPUT	 OR	 OR	<table><tr><th rowspan="2">A</th><th rowspan="2">B</th><th rowspan="2">C</th><th colspan="2">Y</th></tr><tr><th>57</th><th>58</th></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td></tr></table>	A	B	C	Y		57	58	L	L	L	H	L	L	L	H	L	H	L	H	L	H	L	L	H	H	H	L
A		B	C					Y																							
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L	H	H	H	L																											
SP58 Schmitt INV +AND or Schmitt INV + NOR		 OR	 OR																												
SP57 Schmitt INV +NAND or Schmitt INV + OR	A= INPUT B= H-Level C=INPUT Y=OUTPUT	 OR	 OR	<table><tr><th rowspan="2">A</th><th rowspan="2">B</th><th rowspan="2">C</th><th colspan="2">Y</th></tr><tr><th>57</th><th>58</th></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>h</td><td>H</td><td>H</td><td>L</td></tr></table>	A	B	C	Y		57	58	L	H	L	H	L	L	H	H	H	L	H	H	L	L	H	H	h	H	H	L
A		B	C					Y																							
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SP58 Schmitt INV +AND or Schmitt INV + NOR		 OR	 OR																												
SP57 Schmitt INV +AND or Schmitt INV +NOR	A=INPUT B=L-Level C=INPUT Y=OUTPUT	 OR	 OR	<table><tr><th rowspan="2">A</th><th rowspan="2">B</th><th rowspan="2">C</th><th colspan="2">Y</th></tr><tr><th>57</th><th>58</th></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr></table>	A	B	C	Y		57	58	L	L	L	H	L	L	L	H	L	H	H	L	L	L	H	H	L	H	L	H
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SP58 Schmitt INV + NAND or Schmitt INV + OR		 OR	 OR																												
SP57 Schmitt XNOR	A=B B=INPUT C=INPUT Y=OUTPUT	 OR	 OR	<table><tr><th rowspan="2">A</th><th rowspan="2">B</th><th rowspan="2">C</th><th colspan="2">Y</th></tr><tr><th>57</th><th>58</th></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td></tr></table>	A	B	C	Y		57	58	L	L	L	H	L	L	L	H	L	H	H	H	L	L	H	H	H	H	H	L
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L	L	H	L	H																											
H	H	L	L	H																											
H	H	H	H	L																											
SP58 Schmitt XOR																															

Logic configurations(2/2)

Function	Input Condition	TC7SP57 Logic symbol	TC7SP58 Logic symbol	Function Table																				
SP57 Schmitt INV	A= INPUT B=L-Level			<table><tr><th>A</th><th>B</th><th>C</th><th colspan="2">Y</th></tr><tr><td></td><td></td><td></td><td>57</td><td>58</td></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>L</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td><td>H</td></tr></table>	A	B	C	Y					57	58	L	L	L	H	L	H	L	L	L	H
A	B			C	Y																			
			57	58																				
L	L	L	H	L																				
H	L	L	L	H																				
SP58 Schmitt Buffer	C=L-Level Y=OUTPUT																							
SP57 Schmitt INV	A= INPUT B=H-Level			<table><tr><th>A</th><th>B</th><th>C</th><th colspan="2">Y</th></tr><tr><td></td><td></td><td></td><td>57</td><td>58</td></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td></tr></table>	A	B	C	Y					57	58	L	H	L	H	L	H	H	L	L	H
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SP58 Schmitt Buffer	C=L-Level Y=OUTPUT																							
SP57 Schmitt Buffer	A=L-Level B= INPUT			<table><tr><th>A</th><th>B</th><th>C</th><th colspan="2">Y</th></tr><tr><td></td><td></td><td></td><td>57</td><td>58</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td><td>L</td></tr></table>	A	B	C	Y					57	58	L	L	H	L	H	L	H	H	H	L
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SP58 Schmitt INV	C=H-Level Y=OUTPUT																							
SP57 Schmitt Buffer	A=H-Level B=INPUT			<table><tr><th>A</th><th>B</th><th>C</th><th colspan="2">Y</th></tr><tr><td></td><td></td><td></td><td>57</td><td>58</td></tr><tr><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr></table>	A	B	C	Y					57	58	H	L	H	L	H	H	H	H	H	H
A	B			C	Y																			
			57	58																				
H	L	H	L	H																				
H	H	H	H	H																				
SP58 Schmitt INV	C=H-Level Y=OUTPUT																							

Absolute Maximum Rating (Note1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage	V_{IN}	-0.5 to 4.6	V
DC output voltage	V_{OUT}	-0.5 to 4.6 (Note2)	V
		-0.5 to $V_{CC} \square + 0.5$ (Note3)	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20 (Note4)	mA
DC output current	I_{OUT}	± 25	mA
Power dissipation	P_D	180	mW
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 25	mA
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: $V_{CC} = 0\text{ V}$

Note 3: High or Low state. I_{OUT} absolute rating must be observed.

Note 4: $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

Operating Ranges (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	1.2 to 3.6	V
Input voltage	V_{IN}	-0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note2)	V
		0 to V_{CC} (Note3)	
Output current	I_{OH}/I_{OL}	± 8.0 (Note4)	mA
		± 4.0 (Note5)	
		± 1.5 (Note6)	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$

Note 1: The operating range is required to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: $V_{CC} = 0\text{ V}$

Note 3: High or low state

Note 4: $V_{CC} = 3.0\text{ to }3.6\text{ V}$

Note 5: $V_{CC} = 2.3\text{ to }2.7\text{ V}$

Note 6: $V_{CC} = 1.65\text{ to }1.8\text{ V}$

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	H-level	V _P	—		1.2	—	1.10	V
					1.4	—	1.20	
					1.65	—	1.35	
					2.3	—	1.70	
					3.0	—	2.00	
					3.6	—	2.20	
	L-level	V _N	—		1.2	0.10	—	V
					1.4	0.20	—	
					1.65	0.30	—	
					2.3	0.50	—	
					3.0	0.70	—	
					3.6	0.80	—	
Hysteresis voltage		V _H	—		1.2	0.2	0.9	V
					1.4	0.2	0.9	
					1.65	0.2	0.95	
					2.3	0.3	1.0	
					3.0	0.3	1.2	
					3.6	0.3	1.2	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	1.2 to 1.3	V _{CC} - 0.1	—	V
				I _{OH} = -500 μA	1.4 to 1.6	V _{CC} - 0.2	—	
				I _{OH} = -1.5 mA	1.65 to 1.95	V _{CC} - 0.3	—	
				I _{OH} = -4.0 mA	2.3 to 2.7	V _{CC} - 0.4	—	
				I _{OH} = -8.0 mA	3.0 to 3.6	2.40	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.2 to 1.3	—	0.10	
				I _{OL} = 500 μA	1.4 to 1.6	—	0.20	
				I _{OL} = 3.0 mA	1.65 to 1.95	—	0.25	
				I _{OL} = 4.0 mA	2.3 to 2.7	—	0.40	
				I _{OL} = 8.0 mA	3.0 to 3.6	—	0.40	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V	1.2 to 3.6	—	±1.5	μA	
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V	0	—	1.5	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND	1.2 to 3.6	—	3.0	μA	
			V _{CC} ≤ V _{IN} ≤ 3.6 V	1.2 to 3.6	—	±3.0		
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V	2.7 to 3.6	—	100		

AC Characteristics (Ta = -40 to 85°C, Input: tr = tr = 3.0 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time (A, B, C-Y)	t _{pLH} t _{pHL}	Figure 1, Figure 2 CL = 10pF, R _L = 1 MΩ	1.8 ± 0.15	1.0	21.0	ns
			2.5 ± 0.2	0.8	10.0	
			3.3 ± 0.3	0.6	7.0	
	t _{pLH} t _{pHL}	Figure 1, Figure 2 CL = 15pF, R _L = 1 MΩ	1.8 ± 0.15	1.0	23.0	ns
			2.5 ± 0.2	0.8	11.0	
			3.3 ± 0.3	0.6	7.7	
	t _{pLH} t _{pHL}	Figure 1, Figure 2 CL = 30pF, R _L = 1 MΩ	1.8 ± 0.15	1.0	27.0	ns
			2.5 ± 0.2	0.8	12.0	
			3.3 ± 0.3	0.6	8.5	

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}	—	1.8, 2.5, 3.3	6	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note)	1.8, 2.5, 3.3	30	pF

Note : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

AC Test Circuit

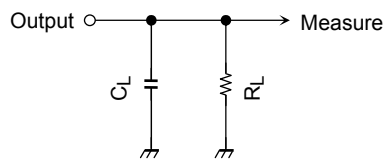
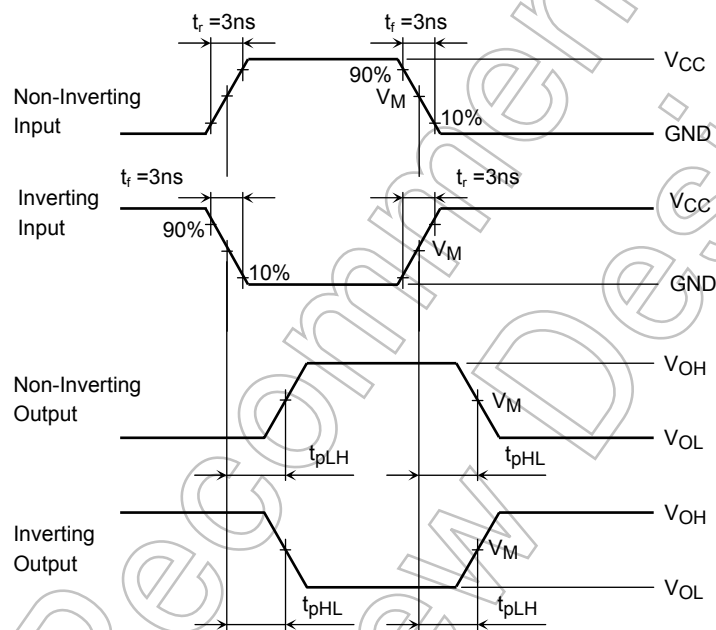


Figure 1

AC Waveform



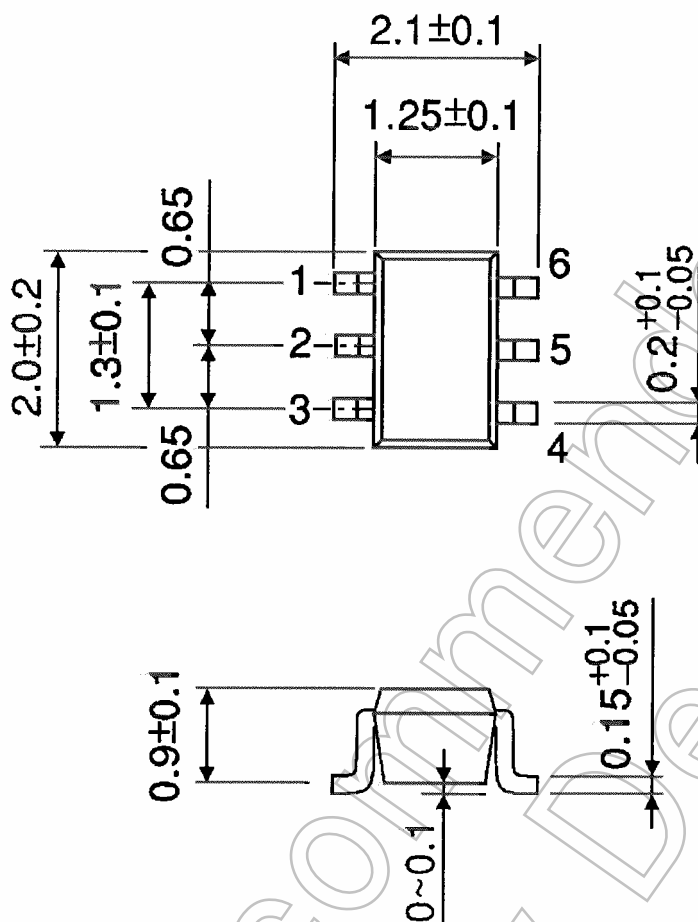
Symbol	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	$1.8 \text{ V} \pm 0.15 \text{ V}$
V_{IN}	V_{CC}	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$

Figure 2 t_{pLH} , t_{pHL}

Package Dimensions

SSOP6-P-0.65A

Unit: mm



Weight: 0.0068 g (typ)

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