

TOSHIBA CMOS LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC75W54FU, TC75W54FK****DUAL OPERATIONAL AMPLIFIER**

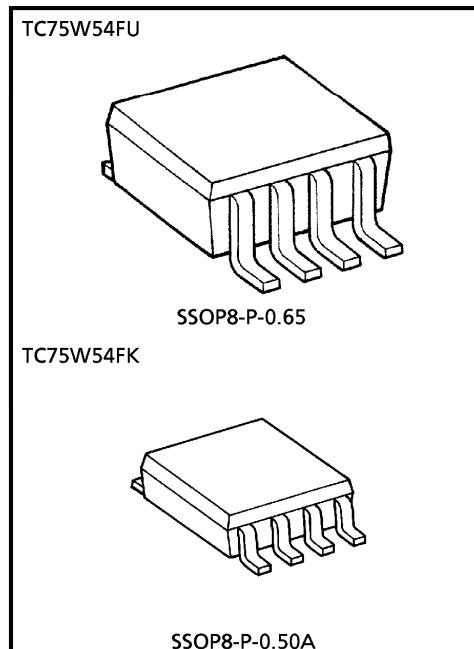
TC75W54 is a CMOS operational amplifier with low supply voltage, low supply current.

**FEATURES**

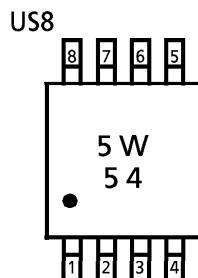
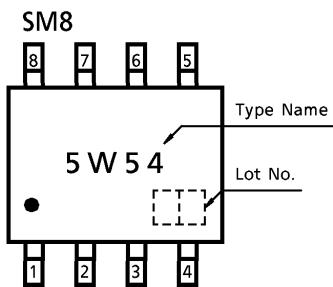
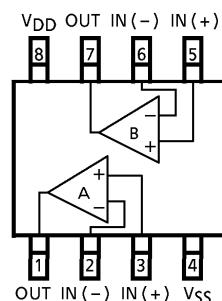
- Low supply voltage :  $V_{DD} = \pm 0.9\sim 3.5V$  or  $1.8\sim 7V$
- Low supply current :  $I_{DD} (V_{DD} = 3V) = 200\mu A$  (Typ.)
- The internally phase compensated operational amplifier.
- Small package

**MAXIMUM RATINGS ( $T_a = 25^\circ C$ )**

CHARACTERISTIC	SYMBOL	RATING	N
Supply Voltage	$V_{DD}, V_{SS}$	7	V
Differential Input Voltage	$DV_{IN}$	$\pm 7$	V
Input Voltage	$V_{IN}$	$V_{DD}\sim V_{SS}$	V
Power Dissipation	$P_D$	250 (SM8)	mW
		200 (US8)	
Operating Temperature	$T_{opr}$	$-40\sim 85$	$^\circ C$
Storage Temperature	$T_{stg}$	$-55\sim 125$	$^\circ C$



Weight  
 SSOP8-P-0.65 : 0.021g (Typ.)  
 SSOP8-P-0.50A : 0.01g (Typ.)

**MARKING (TOP VIEW)****PIN CONNECTION (TOP VIEW)**

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**ELECTRICAL CHARACTERISTICS**DC CHARACTERISTICS (V<sub>DD</sub> = 3.0V, V<sub>SS</sub> = GND, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V <sub>IO</sub>	1	R <sub>S</sub> = 1kΩ	—	2	10	mV
Input Offset Current	I <sub>IO</sub>	—	—	—	1	—	pA
Input Bias Current	I <sub>I</sub>	—	—	—	1	—	pA
Common Mode Input Voltage	CMV <sub>IN</sub>	2	—	0.0	—	2.1	V
Voltage Gain (Open Loop)	G <sub>V</sub>	—	—	60	70	—	dB
Maximum Output Voltage	V <sub>OH</sub>	3	R <sub>L</sub> ≥ 100kΩ	2.9	—	—	V
	V <sub>OL</sub>	4	R <sub>L</sub> ≥ 100kΩ	—	—	0.1	
Common Mode Input Signal Rejection Ratio	CMRR	2	V <sub>IN</sub> = 0.0~2.1V	60	70	—	dB
Supply Voltage Rejection Ratio	SVRR	1	V <sub>DD</sub> = 1.8~7.0V	60	70	—	dB
Supply Current	I <sub>DD</sub>	5	—	—	200	400	μA
Source Current	I <sub>source</sub>	6	—	100	200	—	μA
Sink Current	I <sub>sink</sub>	7	—	200	700	—	μA

DC CHARACTERISTICS (V<sub>DD</sub> = 1.8V, V<sub>SS</sub> = GND, Ta = 25°C)

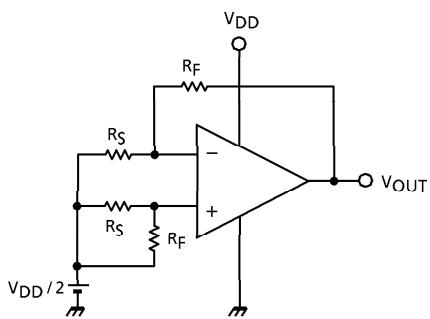
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V <sub>IO</sub>	1	R <sub>S</sub> = 10kΩ	—	2	10	mV
Input Offset Current	I <sub>IO</sub>	—	—	—	1	—	pA
Input Bias Current	I <sub>I</sub>	—	—	—	1	—	pA
Common Mode Input Voltage	CMV <sub>IN</sub>	2	—	0.2	—	0.9	V
Voltage Gain (Open Loop)	G <sub>V</sub>	—	—	60	70	—	dB
Maximum Output Voltage	V <sub>OH</sub>	3	R <sub>L</sub> ≥ 100kΩ	1.7	—	—	V
	V <sub>OL</sub>	4	R <sub>L</sub> ≥ 100kΩ	—	—	0.1	
Supply Current	I <sub>DD</sub>	5	—	—	160	320	μA
Source Current	I <sub>source</sub>	6	—	80	160	—	μA
Sink Current	I <sub>sink</sub>	7	—	200	600	—	μA

AC CHARACTERISTICS (V<sub>DD</sub> = 3.0V, V<sub>SS</sub> = GND, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	—	—	—	0.7	—	V/μs
Unity Gain Cross Frequency	f <sub>T</sub>	—	—	—	0.9	—	MHz

AC CHARACTERISTICS (V<sub>DD</sub> = 1.8V, V<sub>SS</sub> = GND, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	—	—	—	0.6	—	V/μs
Unity Gain Cross Frequency	f <sub>T</sub>	—	—	—	0.8	—	MHz

**TEST CIRCUIT****1. SVRR,  $V_{IO}$** 

- SVRR

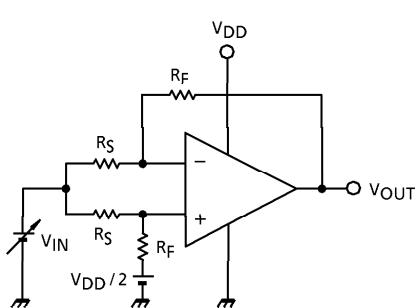
$$V_{DD} = 1.8V : V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}$$

$$V_{DD} = 7.0V : V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}$$

$$SVRR = 20\log\left(\left|\frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- $V_{IO}$

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

**2. CMRR,  $CMV_{IN}$** 

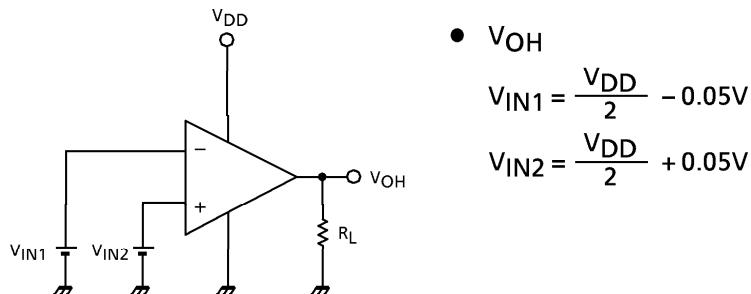
- CMRR

$$V_{IN} = 0.0V : V_{IN} = V_{IN1}, V_{OUT} = V_{OUT1}$$

$$V_{IN} = 2.1V : V_{IN} = V_{IN2}, V_{OUT} = V_{OUT2}$$

$$CMRR = 20\log\left(\left|\frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}}\right| \times \frac{R_S}{R_F + R_S}\right)$$

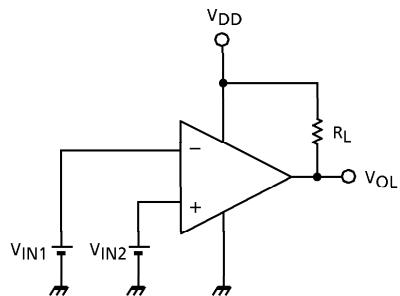
- $CMV_{IN}$

**3.  $V_{OH}$** 

- $V_{OH}$

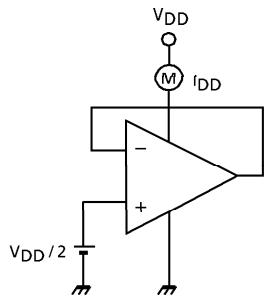
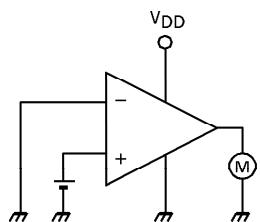
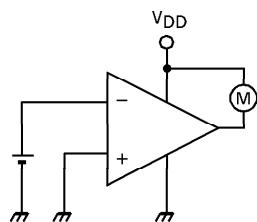
$$V_{IN1} = \frac{V_{DD}}{2} - 0.05V$$

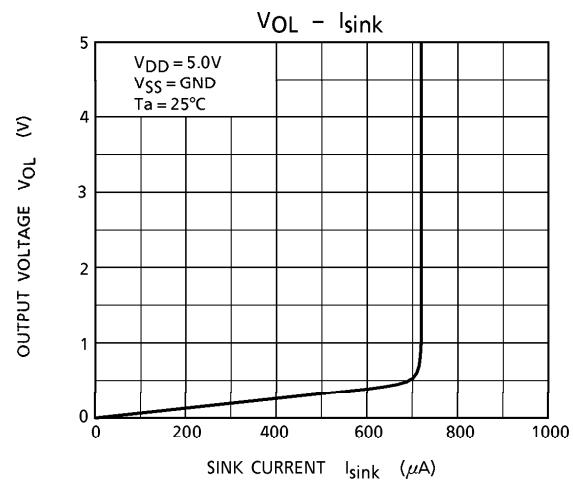
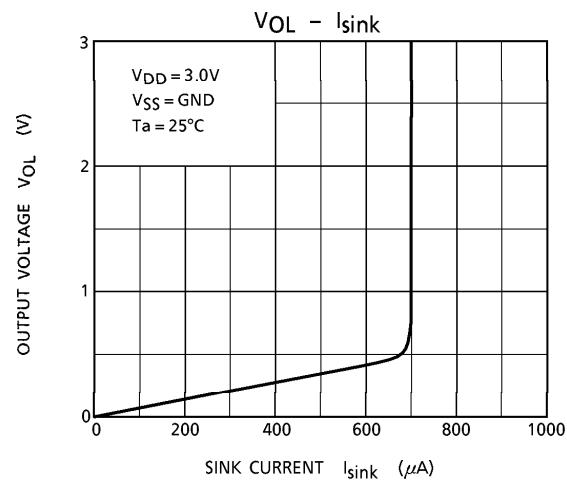
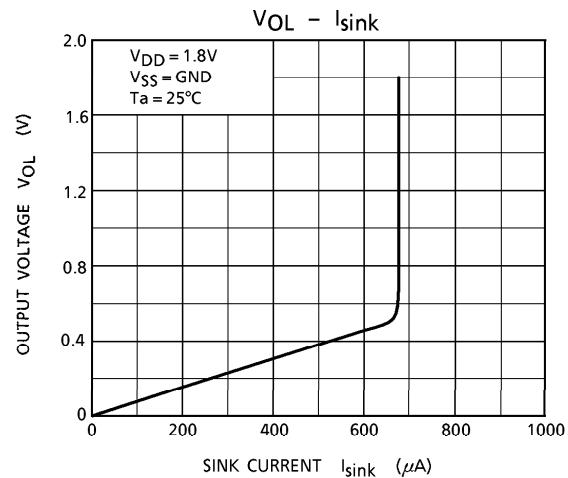
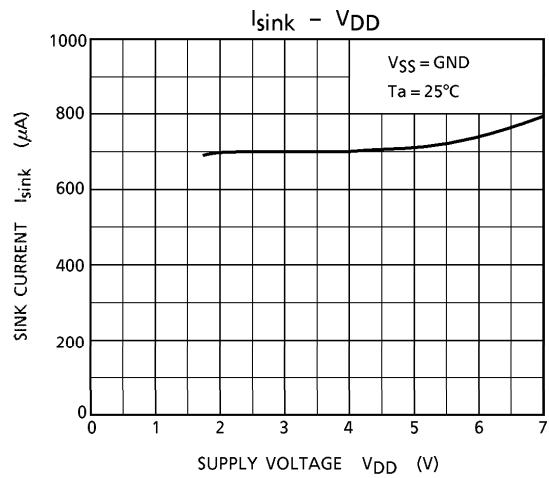
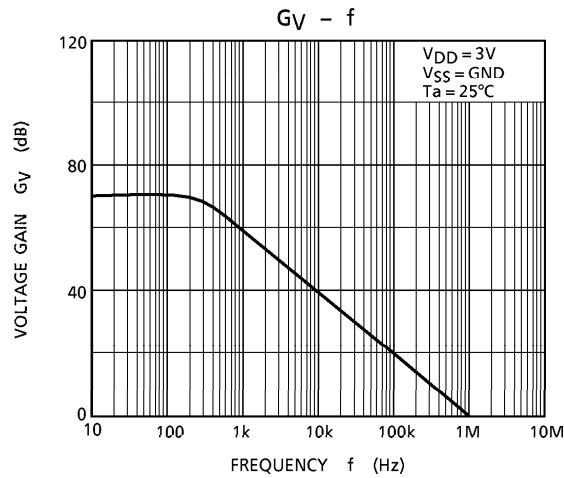
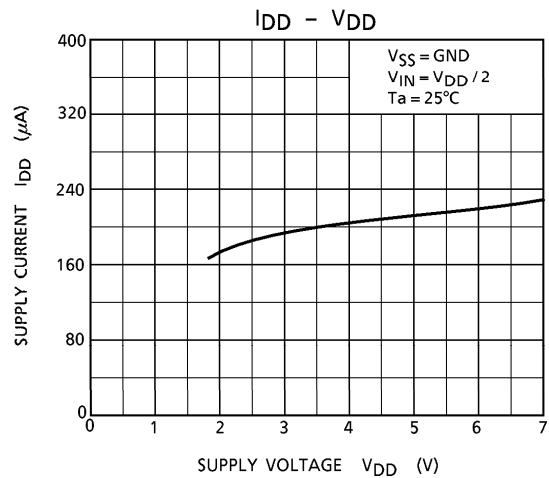
$$V_{IN2} = \frac{V_{DD}}{2} + 0.05V$$

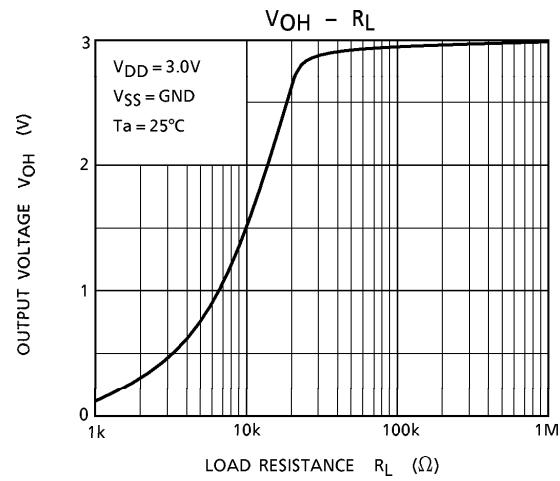
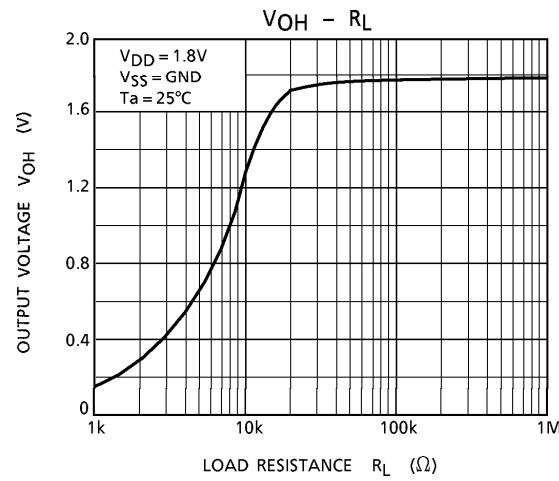
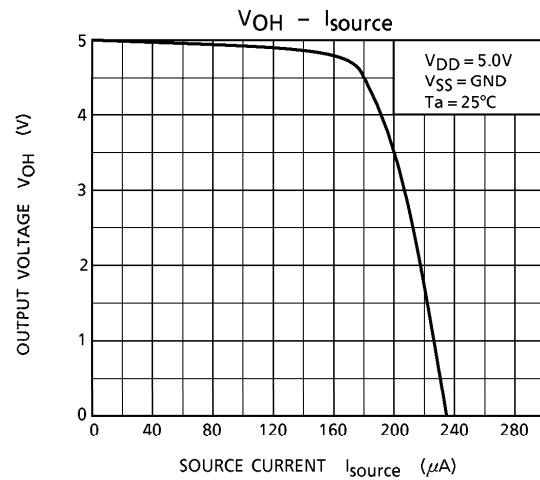
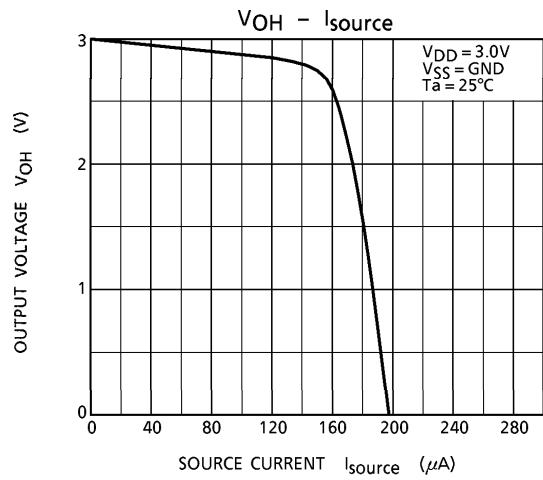
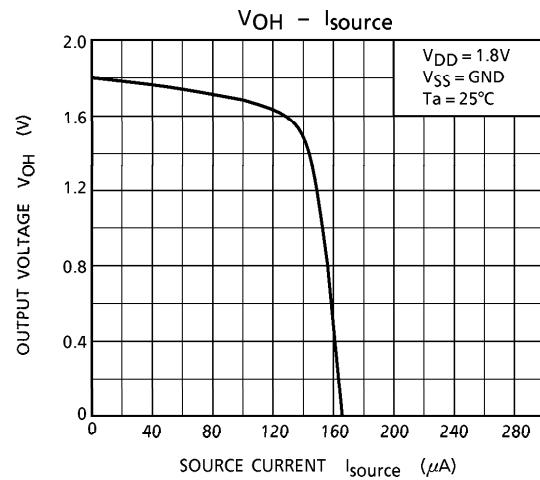
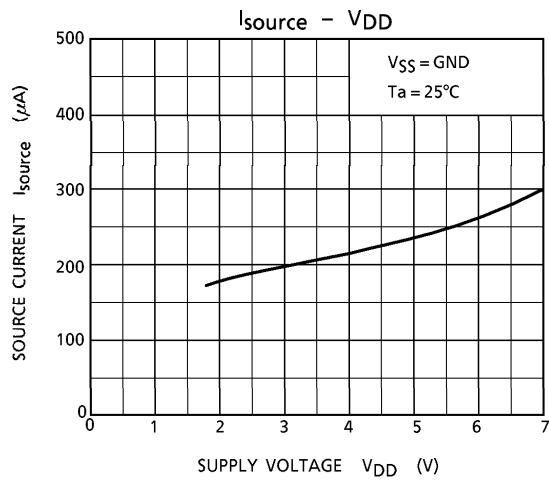
4.  $V_{OL}$ •  $V_{OL}$ 

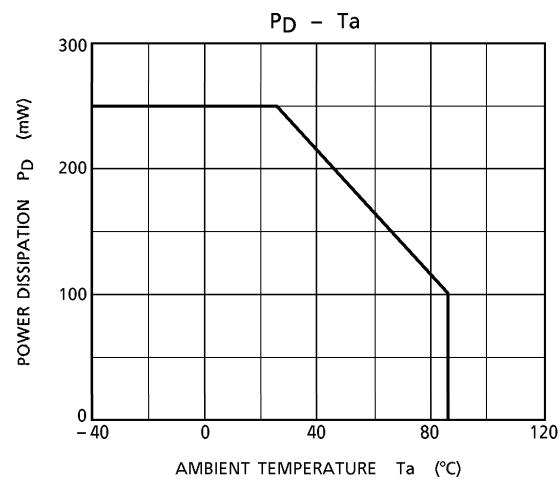
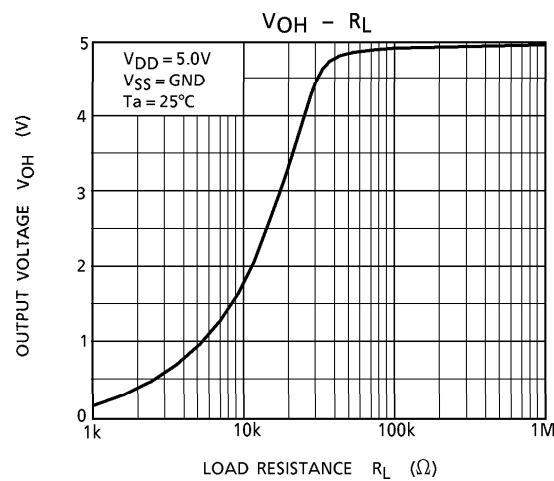
$$V_{IN1} = \frac{V_{DD}}{2} + 0.05V$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.05V$$

5.  $I_{DD}$ 6.  $I_{source}$ 7.  $I_{sink}$ 

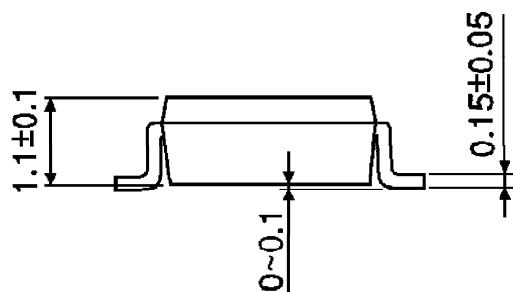
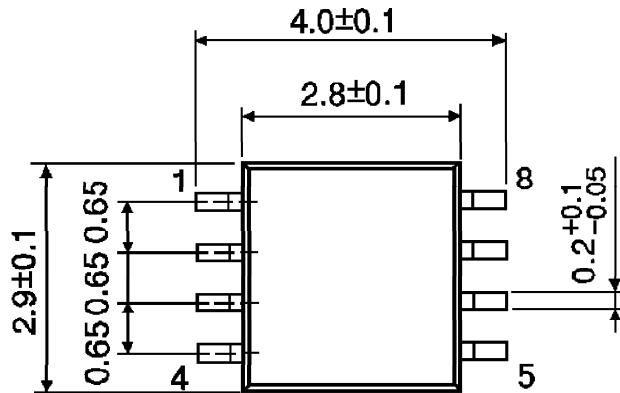






**OUTLINE DRAWING**  
SSOP8-P-0.65

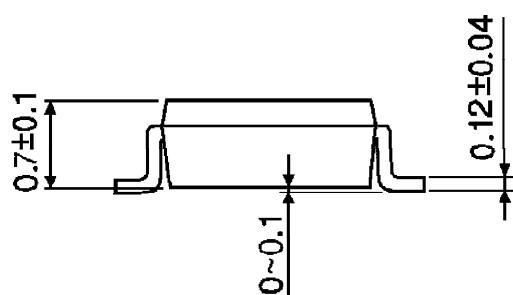
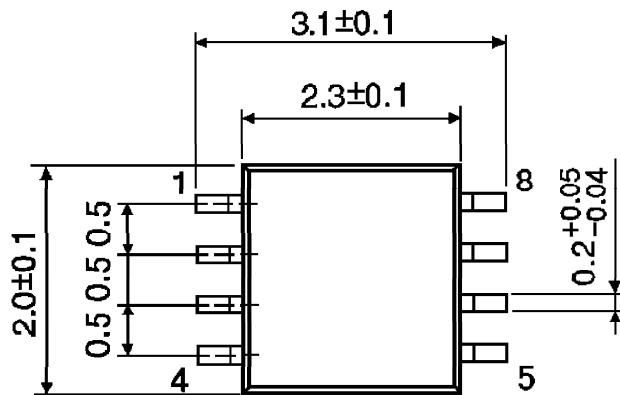
Unit : mm



Weight : 0.021g (Typ.)

**OUTLINE DRAWING**  
SSOP8-P-0.50A

Unit : mm



Weight : 0.01g (Typ.)