TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

# SSM3K15FU

## High Speed Switching Applications Analog Switch Applications

- · Small package
- Low on resistance
  - :  $R_{on} = 4.0 \Omega \text{ (max) } (@V_{GS} = 4 \text{ V})$
  - :  $R_{on} = 7.0 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$

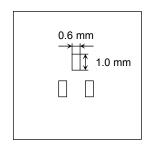
### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		$V_{DS}$	30	V	
Gate-source voltage		$V_{GSS}$	±20	V	
Drain current	DC	ΙD	100	mA	
	Pulse	$I_{DP}$	200		
Drain power dissipation (Ta = 25°C)		P <sub>D</sub> (Note 1)	150	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature		T <sub>stg</sub>	-55 to 150	°C	

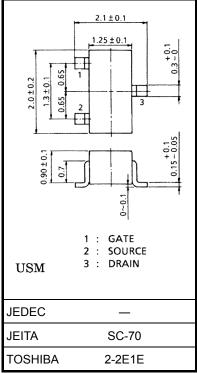
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu Pad: 0.6 mm<sup>2</sup>  $\times$  3)



# Unit: mm

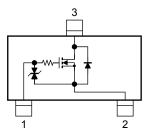


Weight: 0.006 g (typ.)

### Marking

# D P

# **Equivalent Circuit**



#### **Handling Precaution**

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production 2001-02

## **Electrical Characteristics (Ta = 25°C)**

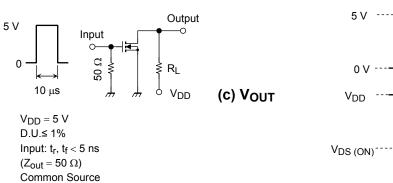
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Drain-source breakdown voltage		V (BR) DSS	$I_D = 0.1 \text{ mA}, V_{GS} = 0$	30	_	_	V
Drain cut-off curre	ent	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0$	_	_	1	μА
Gate threshold vo	oltage	V <sub>th</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 0.1 mA	0.8	_	1.5	V
Forward transfer	admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 3 V, I <sub>D</sub> = 10 mA	25	_	_	mS
Drain-source ON resistance		R <sub>DS (ON)</sub>	$I_D = 10$ mA, $V_{GS} = 4$ V	_	2.2	4.0	Ω
			I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 2.5 V	_	4.0	7.0	
Input capacitance	•	C <sub>iss</sub>	V <sub>DS</sub> = 3 V, V <sub>GS</sub> = 0, f = 1 MHz	_	7.8	_	pF
Reverse transfer	capacitance	C <sub>rss</sub>	V <sub>DS</sub> = 3 V, V <sub>GS</sub> = 0, f = 1 MHz	_	3.6	_	pF
Output capacitance		C <sub>oss</sub>	V <sub>DS</sub> = 3 V, V <sub>GS</sub> = 0, f = 1 MHz	_	8.8	_	pF
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = 5 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0 \text{ to } 5 \text{ V}$	_	50	_	ns
	Turn-off time	t <sub>off</sub>		_	180	_	

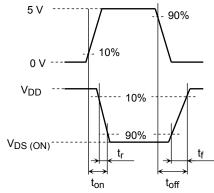
# **Switching Time Test Circuit**

Ta = 25°C







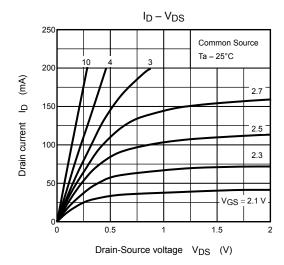


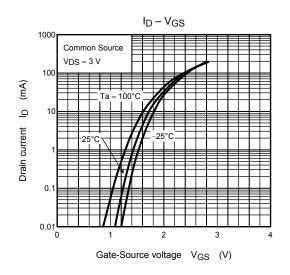
#### **Precaution**

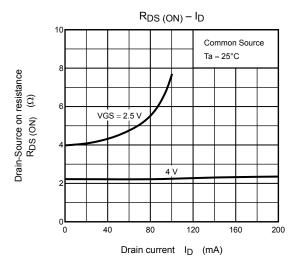
 $V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D$  = 100  $\mu A$  for this product. For normal switching operation,  $V_{GS}$  (on) requires higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires lower voltage than  $V_{th}$ .

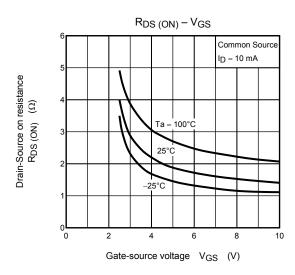
(relationship can be established as follows:  $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$ )

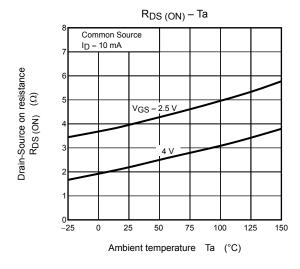
Please take this into consideration for using the device.

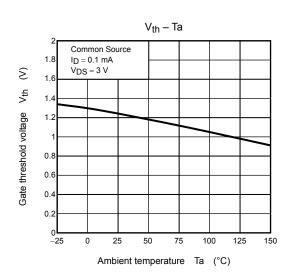


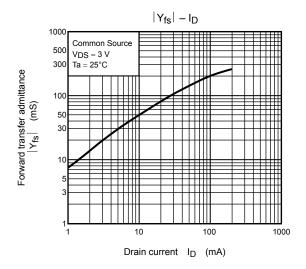


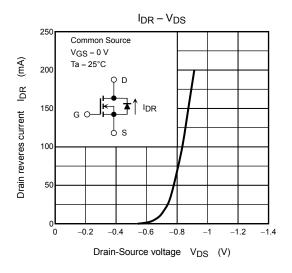


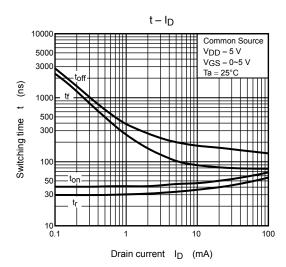


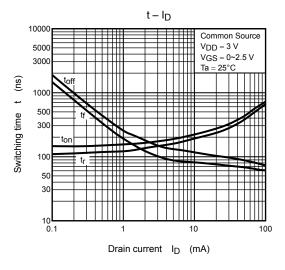


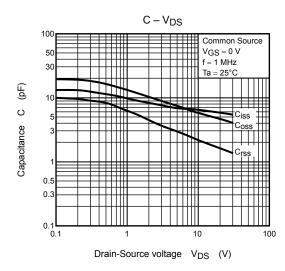


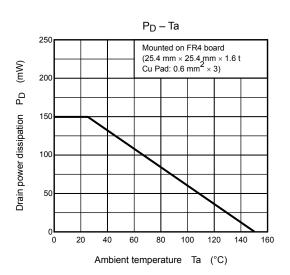












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