TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC574F, TC74VHC574FK

## Octal D-Type Flip Flop with 3-State Output

The TC74VHC574 is advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate $C^2MOS$ technology.

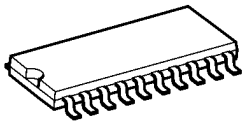
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

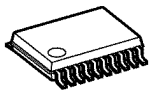
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC74VHC574F



SOP20-P-300-1.27A

TC74VHC574FK



VSSOP20-P-0030-0.50

Weight

SOP20-P-300-1.27A : 0.22 g (typ.)

VSSOP20-P-0030-0.50 : 0.03 g (typ.)

## Features

- High speed: $f_{max}$ = 180 MHz (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V
- Low noise: $V_{OLP}$ = 1.0 V (max)
- Pin and function compatible with 74ALS574

Start of commercial production

1991-11

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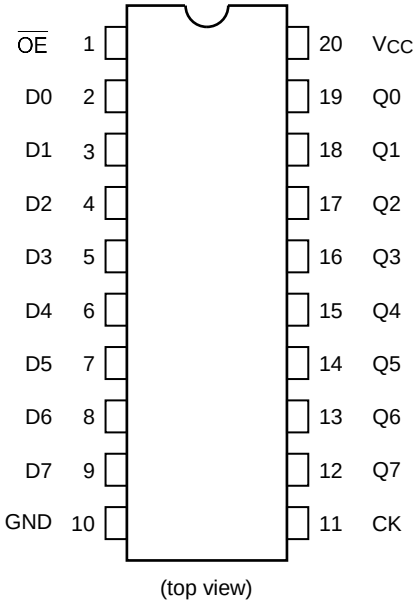
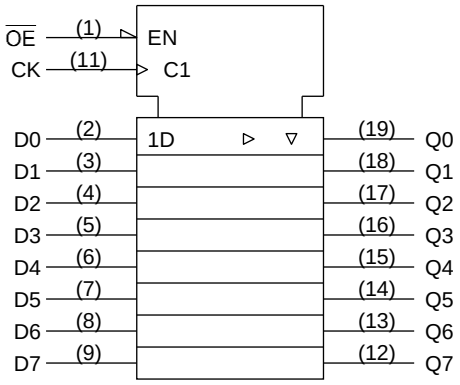
## Pin Assignment




(top view)

## IEC Logic Symbol




## Truth Table

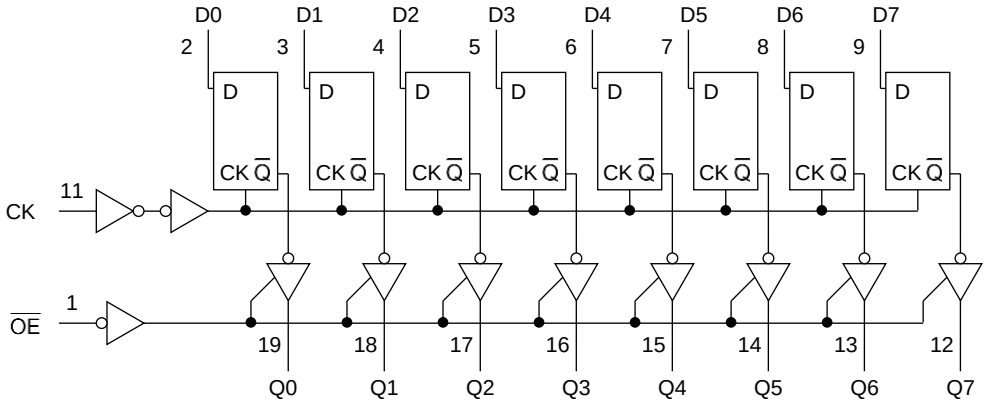
| Inputs | | | Output |
|---|---|---|---|
| $\overline{OE}$ | CK | D | |
| H | X | X | Z |
| L | ↓ | X | Qn |
| L | ↑ | L | L |
| L | ↑ | H | H |

X: Don't care

Z: High impedance

Qn: No change

## System Diagram

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## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to 7.0 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | −20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±75 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 ($V_{CC}$ = 3.3 ± 0.3 V)<br>0 to 20 ($V_{CC}$ = 5 ± 0.5 V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CC}$ or GND.

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## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| High-level input voltage | $V_{IH}$ | — | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | — | $V_{CC}$ × 0.7 | — | |
| Low-level input voltage | $V_{IL}$ | — | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | 3.0 to 5.5 | — | — | $V_{CC}$ × 0.3 | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −8 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| 3-state output off-state current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.25 | — | ±2.50 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |

### Timing Requirements (input: $t_r$ = $t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | Ta = −40 to 85°C | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Typ. | Limit | Limit | |
| Minimum pulse width (CK) | $t_{w\ (H)}$ | — | 3.3 ± 0.3 | — | 5.0 | 5.0 | ns |
| | $t_{w\ (L)}$ | | 5.0 ± 0.5 | — | 5.0 | 5.0 | |
| Minimum set-up time | $t_s$ | — | 3.3 ± 0.3 | — | 3.5 | 3.5 | ns |
| | | | 5.0 ± 0.5 | — | 3.5 | 3.5 | |
| Minimum hold time | $t_h$ | — | 3.3 ± 0.3 | — | 1.5 | 1.5 | ns |
| | | | 5.0 ± 0.5 | — | 1.5 | 1.5 | |

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## AC Characteristics (input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (CK-Q) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 8.5 | 13.2 | 1.0 | 15.5 | ns |
| | | | | 50 | — | 11.0 | 16.7 | 1.0 | 19.0 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.6 | 8.6 | 1.0 | 10.0 | |
| | | | | 50 | — | 7.1 | 10.6 | 1.0 | 12.0 | |
| 3-state output enable time | $t_{pZL}$ $t_{pZH}$ | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 15 | — | 8.2 | 12.8 | 1.0 | 15.0 | ns |
| | | | | 50 | — | 10.7 | 16.3 | 1.0 | 18.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.9 | 9.0 | 1.0 | 10.5 | |
| | | | | 50 | — | 7.4 | 11.0 | 1.0 | 12.5 | |
| 3-state output disable time | $t_{pLZ}$ $t_{pHZ}$ | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 50 | — | 11.0 | 15.0 | 1.0 | 17.0 | ns |
| | | | 5.0 ± 0.5 | 50 | — | 7.1 | 10.1 | 1.0 | 11.5 | |
| Maximum clock frequency | $f_{max}$ | — | 3.3 ± 0.3 | 15 | 80 | 125 | — | 65 | — | MHz |
| | | | | 50 | 50 | 75 | — | 45 | — | |
| | | | 5.0 ± 0.5 | 15 | 130 | 180 | — | 110 | — | |
| | | | | 50 | 85 | 115 | — | 75 | — | |
| Output to output skew | $t_{osLH}$ $t_{osHL}$ | (Note 1) | 3.3 ± 0.3 | 50 | — | — | 1.5 | — | 1.5 | ns |
| | | | 5.0 ± 0.5 | 50 | — | — | 1.0 | — | 1.0 | |
| Input capacitance | $C_{IN}$ | — | | | — | 4 | 10 | — | 10 | pF |
| Output capacitance | $C_{OUT}$ | — | | | — | 6 | — | — | — | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note 2) | | | — | 28 | — | — | — | pF |

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|,\ t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total $C_{PD}$ when n pcs. of latch operate can be gained by the following equation:

$$C_{PD}\ (\text{total}) = 20 + 8 \cdot n$$

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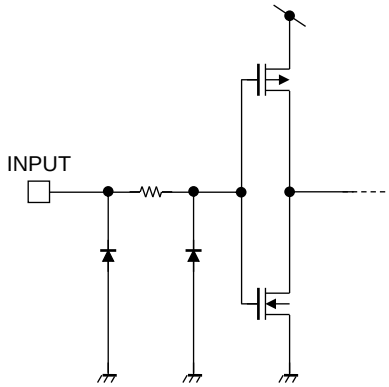
### Noise Characteristics (input: $t_r = t_f = 3$ ns)

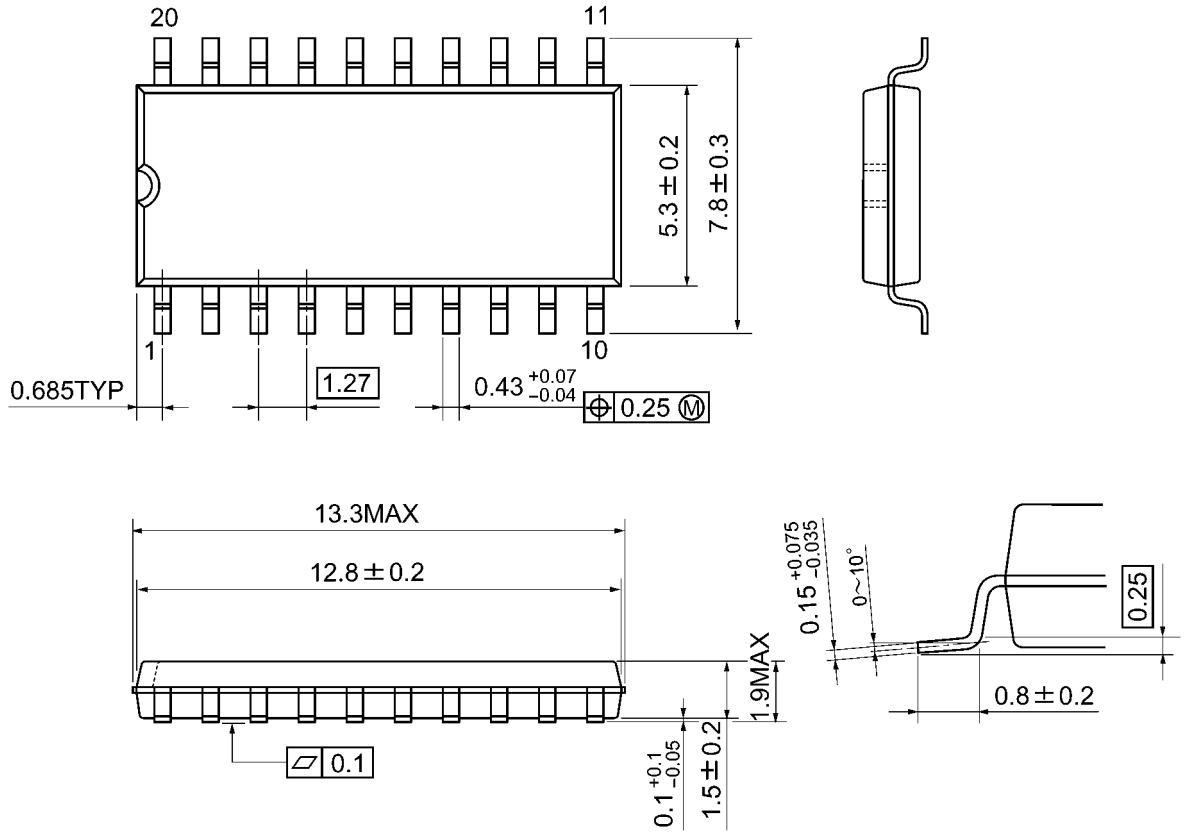
| Characteristics | Symbol | Test Condition | | Ta = 25°C | | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Typ. | Max | |
| Quiet output maximum dynamic $V_{OL}$ | $V_{OLP}$ | $C_L$ = 50 pF | 5.0 | 0.8 | 1.0 | V |
| Quiet output minimum dynamic $V_{OL}$ | $V_{OLV}$ | $C_L$ = 50 pF | 5.0 | −0.8 | −1.0 | V |
| Minimum high level dynamic input voltage | $V_{IHD}$ | $C_L$ = 50 pF | 5.0 | — | 3.5 | V |
| Maximum low level dynamic input voltage | $V_{ILD}$ | $C_L$ = 50 pF | 5.0 | — | 1.5 | V |

## Input Equivalent Circuit



## Package Dimensions

SOP20-P-300-1.27A Unit: mm




Weight: 0.22 g (typ.)

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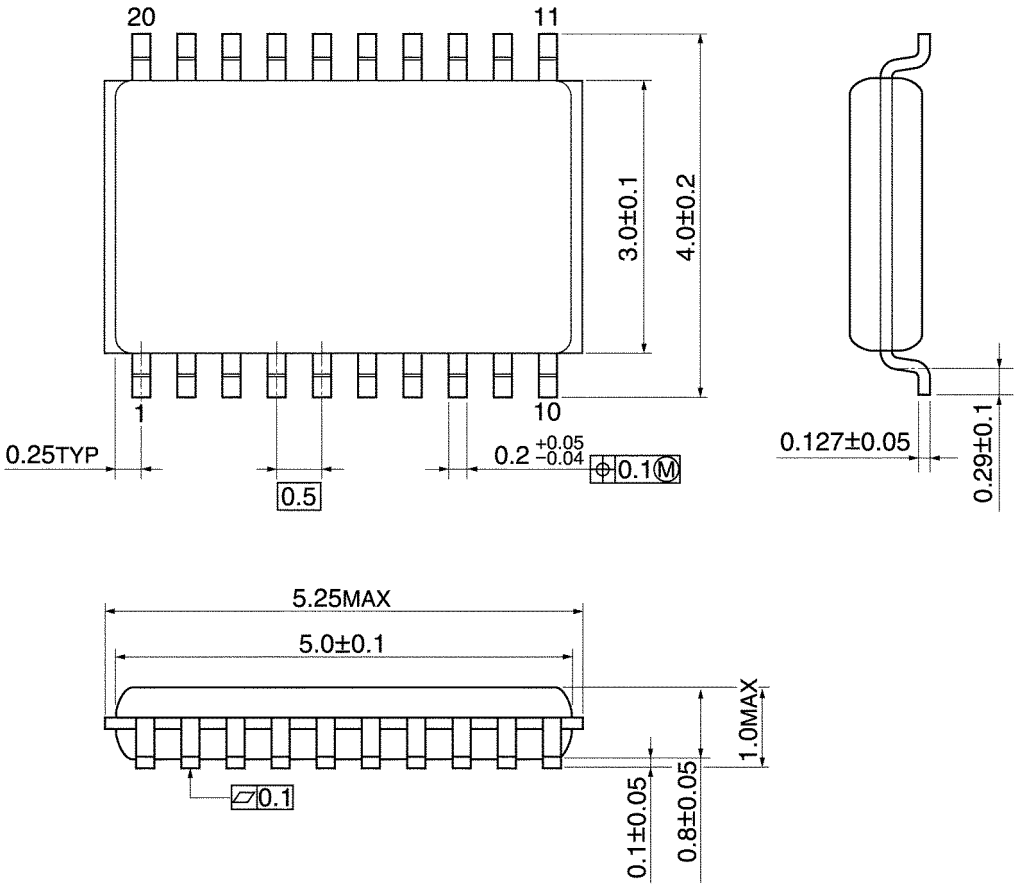
## Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm




Weight: 0.03 g (typ.)

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