

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC03F, TC74VHC03FK

Quad 2-Input NAND Gate (open drain)

The TC74VHC03 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

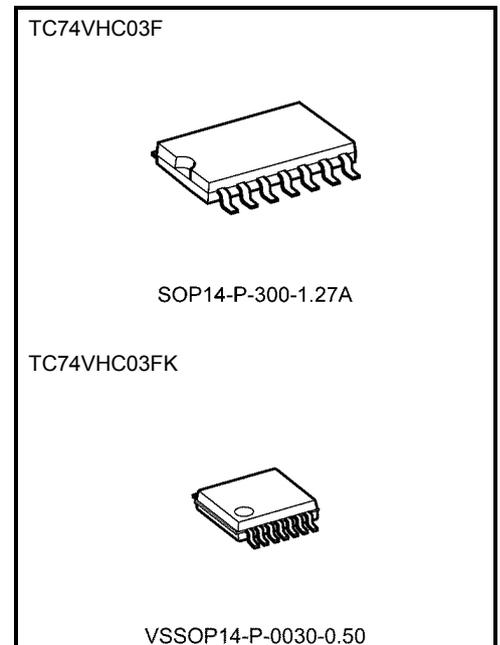
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74VHC00. But the TC74VHC03 has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therefore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: $t_{pZ} = 3.7 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Power down protection is provided on all inputs.
- Wide operating voltage range: $V_{CC (opr)} = 2 \text{ to } 5.5 \text{ V}$
- Low noise: $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS03

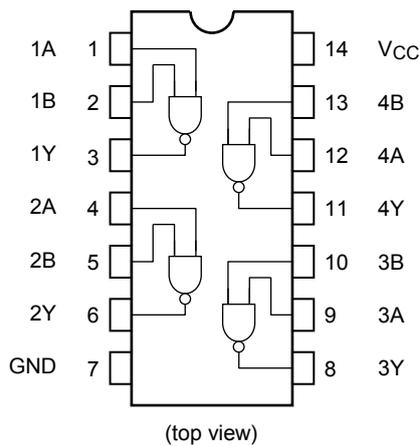


Weight

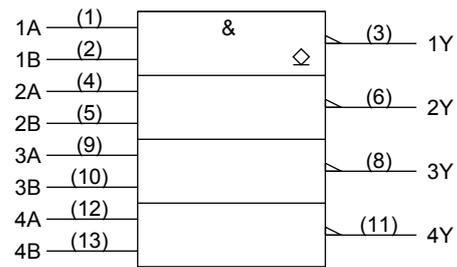
SOP14-P-300-1.27A	: 0.18 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

Start of commercial production
1995-04

Pin Assignment



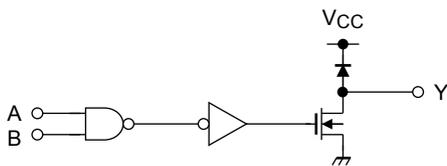
IEC Logic Symbol



Truth Table

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

System Diagram (per gate)



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	25	mA
DC V _{CC} /ground current	I _{CC}	±50	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit		
			V_{CC} (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	V_{IH}	—	2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V	
Low-level input voltage	V_{IL}	—	2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
Output off-state current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.25	—	± 2.50	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	μA	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time	t_{pZL}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	15	—	5.5	7.9	1.0	9.5	ns
				50	—	8.0	11.4	1.0	13.0	
			5.0 ± 0.5	15	—	3.7	5.5	1.0	6.5	
				50	—	5.2	7.5	1.0	8.5	
Propagation delay time	t_{pLZ}	$R_L = 1 \text{ k}\Omega$	3.3 ± 0.3	50	—	8.0	11.4	1.0	13.0	ns
			5.0 ± 0.5	50	—	5.2	7.5	1.0	8.5	
Input capacitance	C_{IN}	—	—	4	10	—	10	pF		
Output capacitance	C_{OUT}	—	—	5	—	—	—	pF		
Power dissipation capacitance	CPD	(Note)	—	6	—	—	—	pF		

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

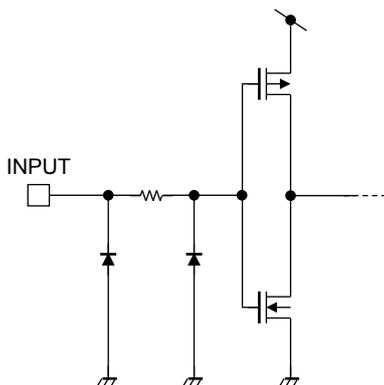
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50 \text{ pF}$	5.0	0.3	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50 \text{ pF}$	5.0	-0.3	-0.8	V
Minimum high level dynamic input voltage	V_{IHD}	$C_L = 50 \text{ pF}$	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	$C_L = 50 \text{ pF}$	5.0	—	1.5	V

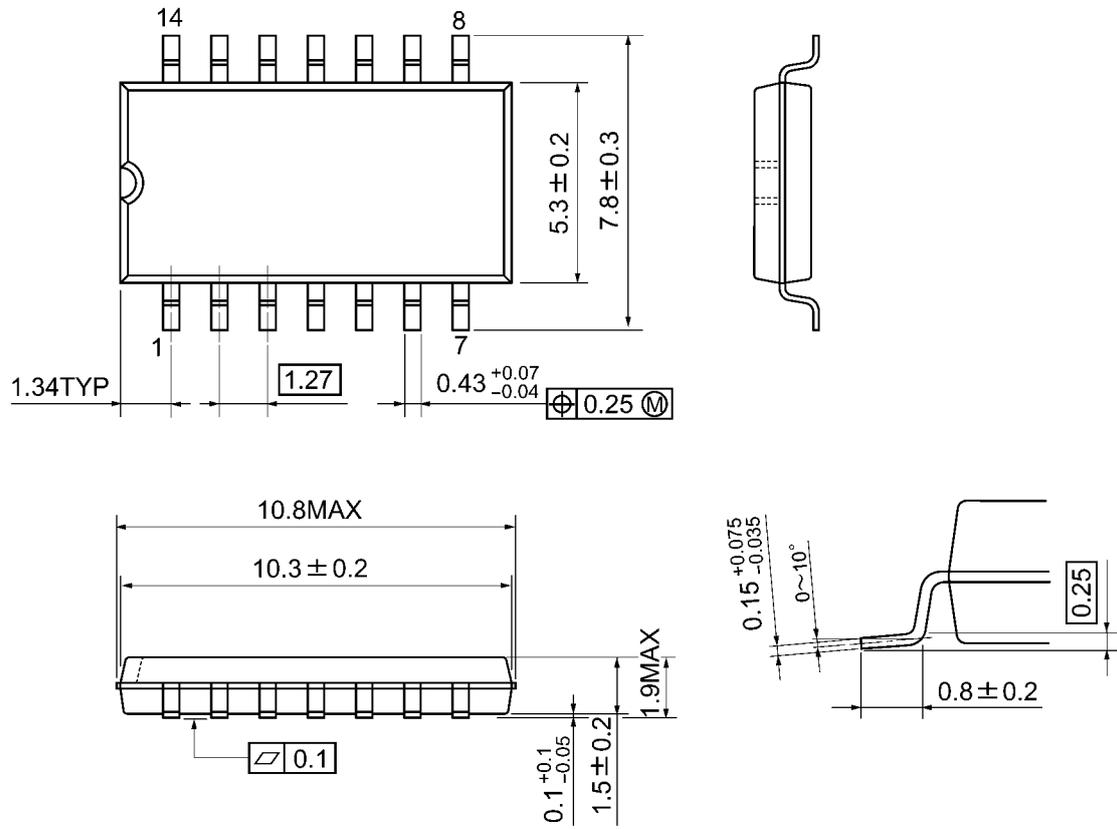
Input Equivalent Circuit



Package Dimensions

SOP14-P-300-1.27A

Unit: mm

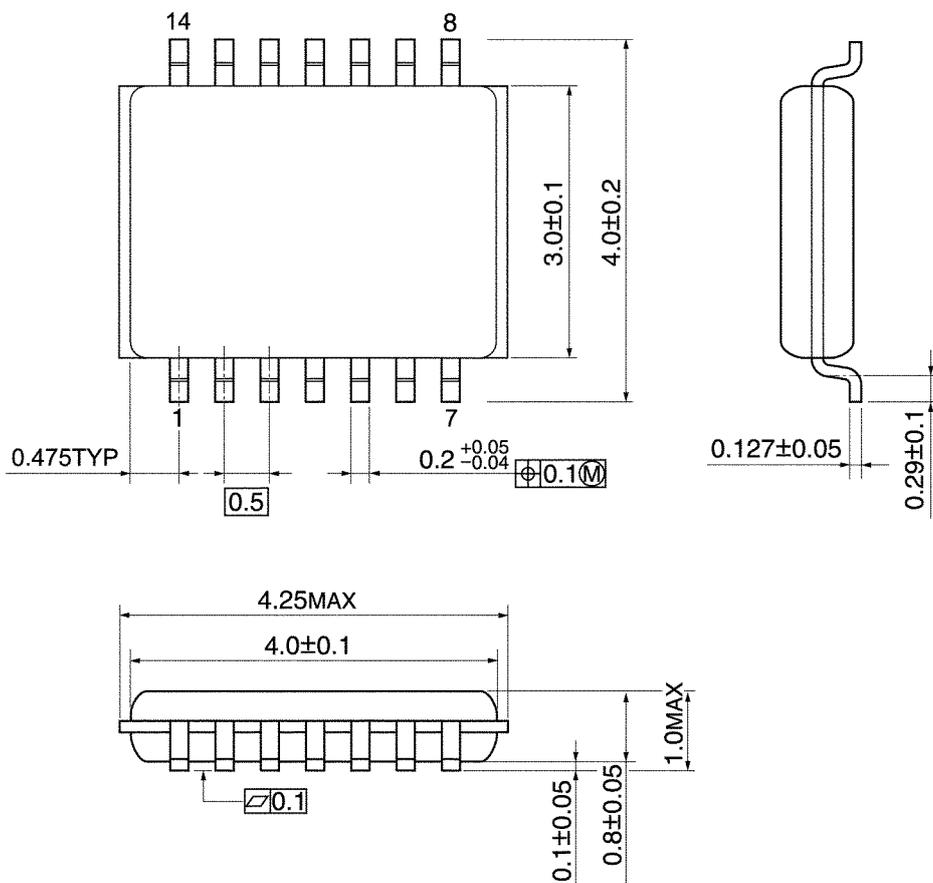


Weight: 0.18 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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