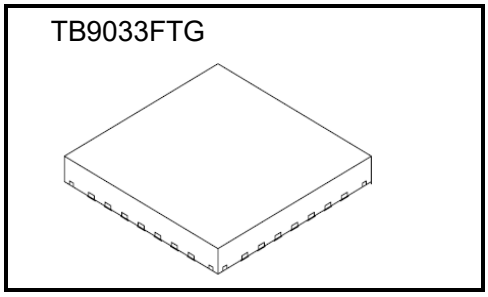
CDMOS Linear Integrated Circuit Silicon Monolithic

TB9033FTG

Automotive CXPI Responder Interface IC

1. Description

The TB9033FTG is an automotive CXPI responder interface IC.
The functions and operation of its 16 configurable I/O pins are controlled through CXPI (Clock Extension Peripheral Interface) communication. The pins support GPIO input/output, ADC input, and PWM output functions.



P-VQFN28-0606-0.65-003

2. Applications

Interfaces for control CXPI Responder Node for various automotive body applications (Door locks, Cluster switches, Steering switches, etc.)

3. Features

- CXPI (ISO 20794-2 to 4, ISO 14229-8) Compliant
- 16-channel GPIO I/O
- 6-channel, 10-bit A/D Converter
- 4-channel, 8-bit PWM
- Input specifications
  - Input ON/OFF detection (event transmission)
  - Chattering filter (configurable detection time and sample count)
  - Input monitoring in Sleep State
  - Switch matrix (up to 4x4)
  - Moving average for ADC (configurable by time and count)
- Output specifications
  - ON/OFF control (configurable by time and count)
  - Output control in the event of communication interruption.
  - PWM frequency configuration (200Hz to 22kHz)
- Built-in overheat, overvoltage and undervoltage detection circuits.
- Current in Deep Sleep Mode: 13μA (typ.)
- Operating Power Range 6 to 18V (Absolute Maximum Ratings: 40V)
- Operating temperature range: -40 to 125°C
- Junction temperature (T_J): 150 °C (max)
- AEC-Q100 / AEC-Q006 qualification.
- If the package label includes “[[G]]/RoHS COMPATIBLE,” “[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)]]”, “RoHS COMPATIBLE” or “RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV”, the product complies with the EU RoHS Directive (2011/65/EU) within the meaning indicated by the label description.

Start of commercial production
2026-10

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4. Block Diagram

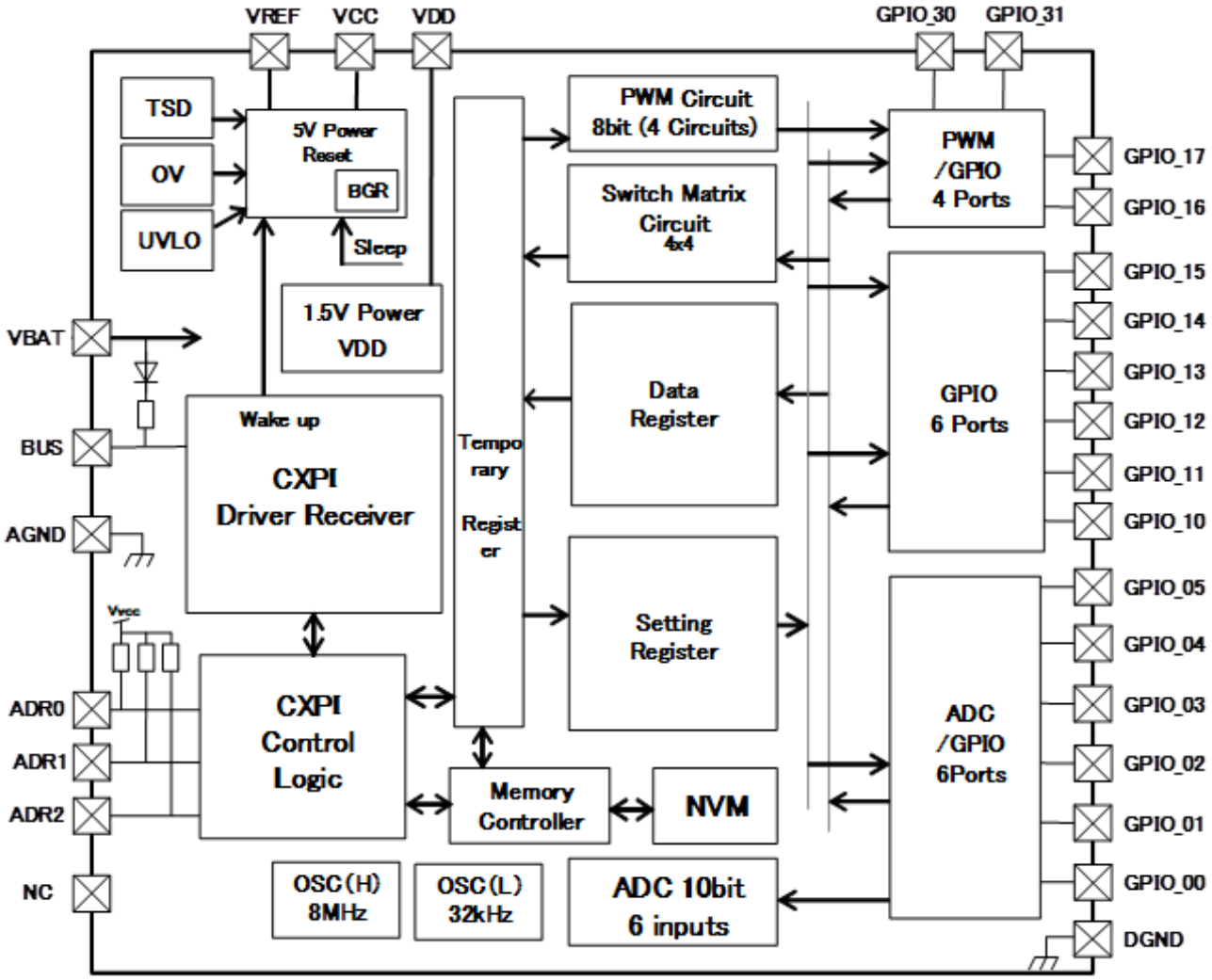


Figure 4.1 Block Diagram

5. Information on Pin

5.1. Pin Assignments

Top view

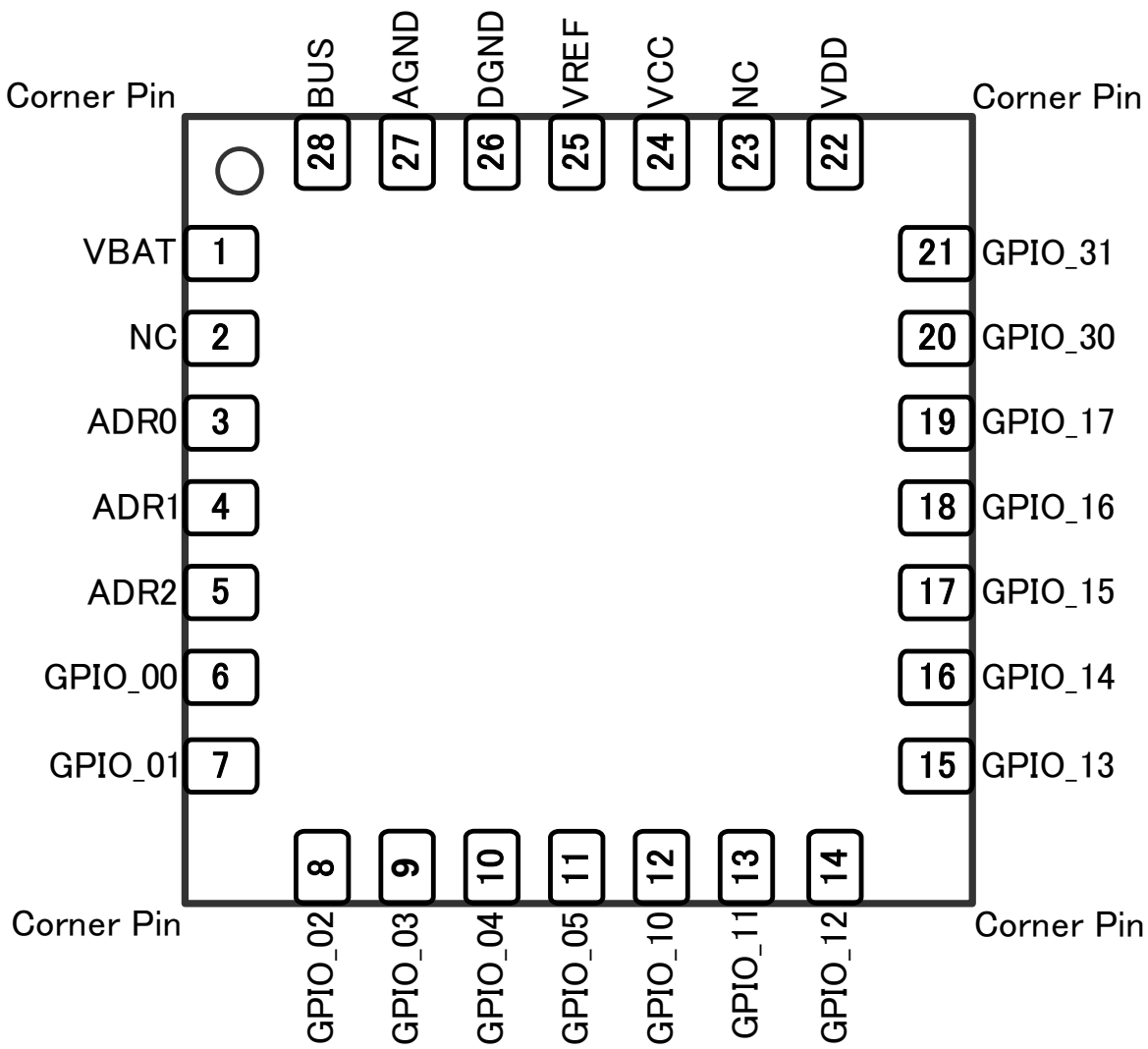


Figure 5.1 Pin Assignments

5.2. Pin Arrangement and Function Description

Table 5.2 Pin Arrangement and Function Description

No.	Name	Description	Withstand Voltage	IN, OUT	Remarks
1	VBAT	Power supply pin	40V	IN	+ 12V power supply
2	NC	Unused pin	—	—	Use in OPEN
3	ADR0	Node Address setting pin	6V	IN	50 kΩ pull-down resistor built-in (Note 1)
4	ADR1	Node Address setting pin	6V	IN	50 kΩ pull-down resistor built-in (Note 1)
5	ADR2	Node Address setting pin	6V	IN	50 kΩ pull-down resistor built-in (Note 1)
6	GPIO_00	IN/OUT, or ADC	6V	IN/OUT	—
7	GPIO_01	IN/OUT, or ADC	6V	IN/OUT	—
8	GPIO_02	IN/OUT, or ADC	6V	IN/OUT	—
9	GPIO_03	IN/OUT, or ADC	6V	IN/OUT	—
10	GPIO_04	IN/OUT, or ADC	6V	IN/OUT	—
11	GPIO_05	IN/OUT, or ADC	6V	IN/OUT	—
12	GPIO_10	IN/OUT, switch matrix	6V	IN/OUT	—
13	GPIO_11	IN/OUT, switch matrix	6V	IN/OUT	—
14	GPIO_12	IN/OUT, switch matrix	6V	IN/OUT	—
15	GPIO_13	IN/OUT, switch matrix	6V	IN/OUT	—
16	GPIO_14	IN/OUT, switch matrix	6V	IN/OUT	—
17	GPIO_15	IN/OUT, switch matrix	6V	IN/OUT	—
18	GPIO_16	IN/OUT, switch matrix, or PWM	6V	IN/OUT	—
19	GPIO_17	IN/OUT, switch matrix, or PWM	6V	IN/OUT	—
20	GPIO_30	IN/OUT, or PWM	6V	IN/OUT	—
21	GPIO_31	IN/OUT, or PWM	6V	IN/OUT	—
22	VDD	Power supply for 1.5V Reg output and 1.5V logic	2.1V	OUT	—
23	NC	Unused pin	—	—	Use in OPEN
24	VCC	Power supply for 5V Reg output and 5V logic (Note 2)	6V	OUT	—
25	VREF	5V input for ADC	6V	IN	—
26	DGND	Digital GND pin	—	—	—
27	AGND	Analogue GND pin	—	—	—
28	BUS	BUS pin for CXPI	40V	IN / OUT	Integrated 30 kΩ pull-up
-	Corner Pin	Connect the cable GND before use.	—	—	—
-	E-Pad	Connect the cable GND before use.	—	—	—

NC: Non-connect pin

Note 1: ADRx pin is pulled up only when it is read as the initial address at power-on. In other states, 50kΩ pull-down.

Note 2: If a resistive load of approximately 1 to 20Ω is connected to VCC pin (which provides a 5V output) for an extended period, it may lead to device damage. Please exercise caution.

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5.3. Equivalent Circuits around Pins

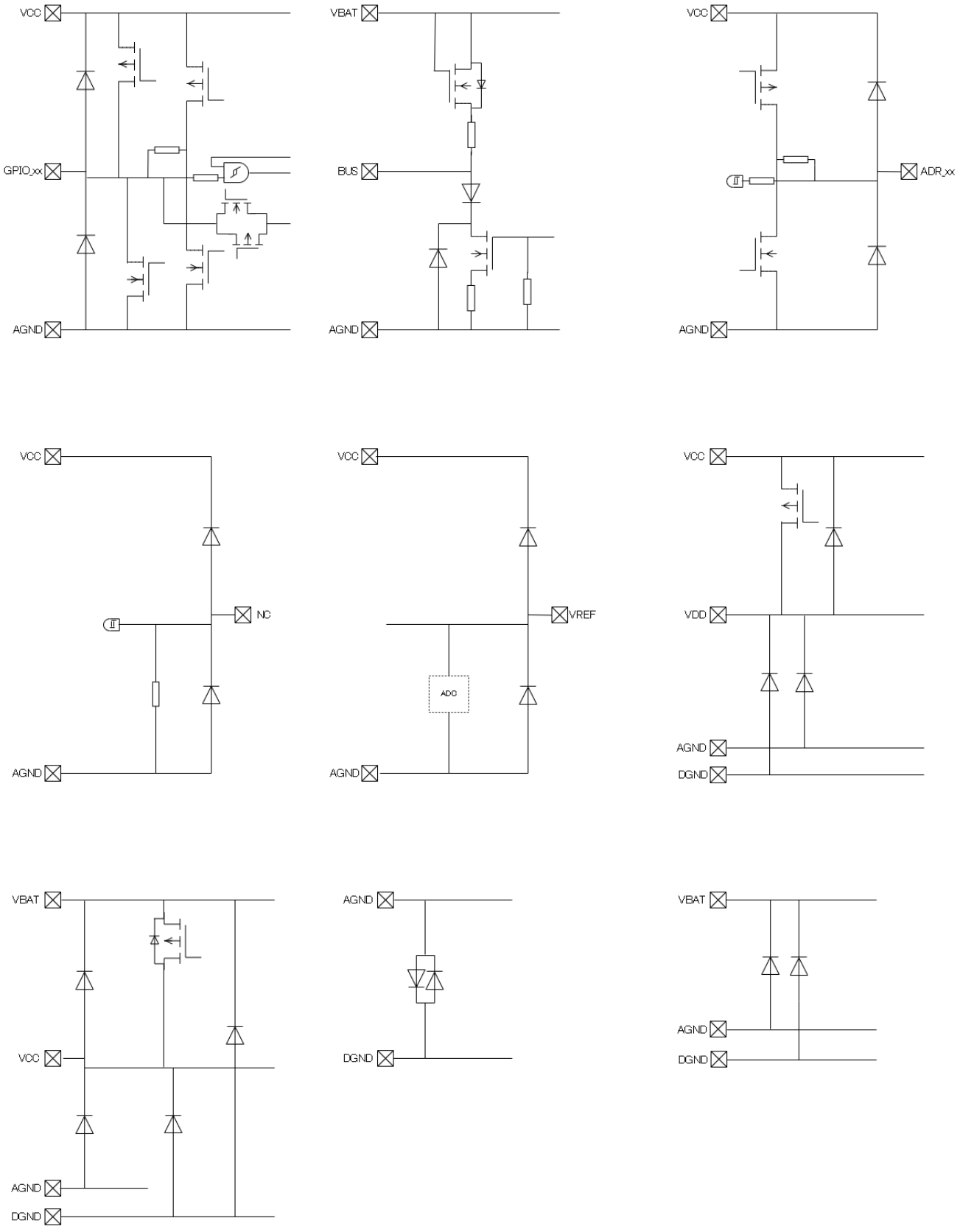
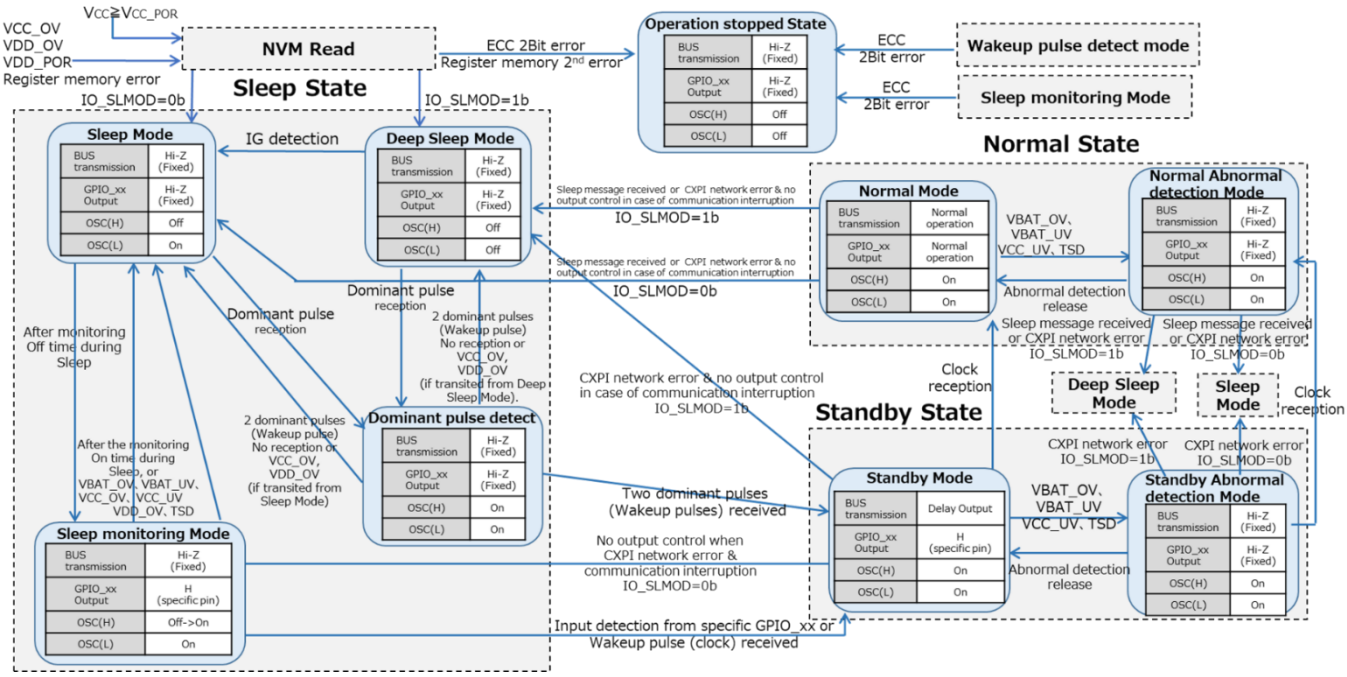


Fig. 5.2 Equivalent Circuits around Pins 1

6. State Transition

6.1. Normal operation

This is the state transition when there is no output specification at the time of communication interruption as the normal operation of this IC.



Note: IO_SLMOD: Mode selection during Sleep (0b: Sleep Mode, 1b: Deep Sleep Mode)

Figure 6.1 State Transition Diagram1

6.1.1. Sleep State

The state is that transmission/reception cannot be done via BUS.

6.1.1.1. Deep Sleep Mode

Deep Sleep Mode is the Mode of reducing the consumed current to the lowest level on the assumption that IG is Off. The internal low-speed clock is also stopped.

■ Transition conditions to Deep Sleep Mode:

(1) When I/O configuration data IO_SLMOD = 1 read from NVM after power ON.
(2) When a Sleep message is received in Normal Mode. (When IO_SLMOD=1)
(3) When a CXPI network errors in Normal Mode and there is no GPIO_xx to output when communication is interrupted. (When IO_SLMOD=1)
(4) When two dominant pulses (wake-up pulse) are not received within $T_{RX_Wakeup_Space_S}$ period in Dominant Pulse Detect Mode. (when transitioned from Deep Sleep Mode)
(5) When there is a CXPI network error in Standby Mode and there is no GPIO_xx output when communication is interrupted. (When IO_SLMOD=1)
(6) When a Sleep message is received in Normal Abnormality Detection Mode. (When IO_SLMOD=1)
(7) When a CXPI network error is detected in Normal Abnormality Detection Mode. (When IO_SLMOD=1)
(8) When a CXPI network error is detected in Standby Abnormality Detection Mode. (When IO_SLMOD=1)
(9) When VCC overvoltage or VDD overvoltage is detected in Dominant Pulse Detect Mode. (when transitioned from Deep Sleep Mode)

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■ Transition conditions from Deep Sleep Mode:
(1) Transition to Sleep Mode when the IG Detect pin input detects a High or Low level, depending on the IO configuration.
(2) Dominant pulse is received and transition to Dominant Pulse Detect Mode.

6.1.1.2. Sleep Mode

Sleep Mode indicates that transmission or reception has stopped. In this mode, the internal low-speed clock remains active, allowing the device to transition to Sleep Monitoring Mode.

■ Transition conditions to Sleep Mode:
(1) When I/O configuration data IO_SLMOD = 0 read from NVM after power ON.
(2) When a Sleep message is received in Normal Mode. (IO_SLMOD = 0 of I/O configuration)
(3) When IG detect pin signal is High or Low in Deep Sleep Mode.
(4) When two dominant pulses (wake-up pulse) are not received within $T_{RX_Wakeup_Space_S}$ period in Dominant Pulse Detect Mode. (When transitioned from Sleep Mode)
(5) If monitoring On/Off is set during Sleep, it transitions to Sleep Mode during the Off time.
(6) When there is a CXPI network error in Normal Mode and there is no GPIO_xx to output when communication is interrupted. (When IO_SLMOD=0)
(7) When there is a CXPI network error in Standby Mode and no GPIO_xx output when communication is interrupted. (When IO_SLMOD=0)
(8) When a Sleep message is received in Normal Abnormality Detection Mode. (When IO_SLMOD=0)
(9) When a CXPI network error is detected in Normal Abnormality Detection Mode. (When IO_SLMOD=0)
(10) When a CXPI network error is detected in Standby Abnormality Detection Mode. (When IO_SLMOD=0)
(11) When VCC overvoltage or VDD overvoltage is detected in Dominant Pulse Detect Mode. (When it is transitioned from Sleep Mode)
(12) When VBAT overvoltage, VBAT undervoltage, VCC overvoltage, VCC undervoltage, VDD overvoltage, or overheat is detected in Sleep Monitoring Mode.

■ Transition conditions from Sleep Mode:
(1) Receives a dominant pulse and transitions to Dominant Pulse Detect Mode.
(2) When monitoring On/Off is set for Sleep, transitions to Sleep Monitoring Mode during On time.

Note: In Sleep Mode/Sleep Monitoring Mode, if IG detection is disabled from the enabled level (H/L), it transitions to Deep Sleep Mode. (When IO_SLMOD=1)

6.1.1.3. Sleep monitoring Mode

If I/O configuration is set to a Sleep monitoring On/Off, it transitions to Sleep Monitoring Mode during On time. In Sleep Monitoring Mode, inputs on the configured pins are monitored, and High/Low outputs are driven on the designated output pins according to the I/O configuration.

■Transition conditions to Sleep monitoring Mode:
(1) Sleep monitoring On/Off is set to transition to Sleep Monitoring Mode during On time.

■Transition conditions from Sleep monitoring Mode:
(1) Sleep monitoring On/Off is set to transition to Sleep Mode during Off time.
(2) Transition to Standby Mode when input is detected from a specific pin determined by the I/O configuration.
(3) Transition to Standby Mode when Wake-up pulse is received.
(4) Transition to Sleep Mode when VBAT overvoltage, VBAT undervoltage, VCC overvoltage, VCC undervoltage, VDD overvoltage or overheat is detected.

Note: When a dominant pulse is received in Sleep Monitoring Mode, Dominant Pulse Detect Mode occurs simultaneously. It waits for receiving two dominant pulses (Wake-up pulse) during $T_{RX_Wakeup_Space_S}$ period. At the same time, stands by for inputting a particular pin, and transitions to Standby Mode by detecting one of them. This case is omitted on the 6.1. State Transition Diagram.

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6.1.1.4. Dominant Pulse Detect Mode

When a dominant pulse is received in any Mode of Sleep State, it transitions to Dominant Pulse Detect Mode. In Dominant Pulse Detect Mode, two dominant pulses (Wake-up pulse) are received or sampled during $T_{RX_Wakeup_Space_S}$ period.

■ Transition conditions to Dominant Pulse Detect Mode

(1) When a dominant pulse is received in Deep Sleep Mode
(2) When a dominant pulse is received in Sleep Mode

■Transition conditions from Dominant Pulse Detect Mode

(1) Transition to Standby Mode after receiving two dominant pulses (Wake-up pulse).
→Wake-up pulse (dominant twice) is recognized after $T_{RX_Wakeup_Detect_S}$ period from the dominant pulse reception. Wake-up pulse before $T_{RX_Wakeup_Detect_S}$ period are not recognized.
(2) Transition to Deep Sleep Mode when two dominant pulses (Wake-up pulse) are not received within $T_{RX_Wakeup_Space_S}$ period (when transitioned from Deep Sleep Mode)
(3) Transition to Sleep Mode when two dominant pulses (Wake-up pulse) are not received within $T_{RX_Wakeup_Space_S}$ period (when transitioned from Sleep Mode)
(4) Transition to Sleep Mode when VCC overvoltage or VDD overvoltage is detected (when transitioned from Sleep Mode)
(5) Transition to Deep Sleep Mode when VCC overvoltage or VDD overvoltage is detected (when transitioned from Deep Sleep Mode)

Note: When Dominant Pulse Detect Mode is the monitoring On period during Sleep, it will occur simultaneously with the Sleep monitoring Mode. It waits for receiving two dominant pulses (Wake-up pulse) during $T_{RX_Wakeup_Space_S}$ period. At the same time, stand by for inputting a particular pin, and transits to Standby Mode by detecting one of them. This case is omitted on the 6.1. State Transition Diagram.

Note: Upon detection of a VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overtemperature condition, the device remains in the current operating mode and does not transition to Sleep Mode or Deep Sleep Mode.

6.1.2. Standby State

In this state, wake-up pulses can be transmitted. However, message transmission and reception via the bus are not available.

6.1.2.1. Standby Mode

Wake-up pulse can be transmitted to the BUS. It also transitions to Normal Mode by receiving a clock signal.

■ Transition conditions to Standby Mode:

(1) When an input is detected from a specified pin determined by I/O configuration in Sleep monitoring Mode.
(2) When two dominant pulses (Wake-up pulse) are received in Sleep Monitoring Mode
(3) When two dominant pulses (Wake-up pulse) are received in Dominant Pulse Detect Mode
(4) When Abnormality detection is canceled by Standby Abnormality Detection Mode.

■ Transition conditions from Standby Mode:

(1) Transition to Normal Mode when a clock is received from the Commander Node.
(2) Transition to Standby Abnormality Detection Mode when VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected.
(3) Transition to Deep Sleep Mode when there is a CXPI network error and there is no GPIO_xx to output when communication is interrupted. (when IO_SLMOD=1).
(4) Transition to Sleep Mode when there is a CXPI network error and there is no GPIO_xx to output when communication is interrupted. (when IO_SLMOD=0).

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6.1.2.2. Standby Abnormality Detection Mode

When VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheating is detected in Standby Mode operation, BUS output and GPIO_xx output are stopped and standby.

■ Transition conditions to Standby Abnormality Detection Mode

(1) If VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected in Standby Mode.

■ Transition conditions from Standby Abnormality Detection Mode

(1) Transition to Standby Mode when The abnormal condition is cleared.
(2) Transition to Normal Abnormality Detection Mode when a clock is received from the Commander Node.
(3) Transition to Sleep Mode when a CXPI network error is detected. (When IO_SLMOD=0)
(4) Transition to Deep Sleep Mode when a CXPI network error is detected. (When IO_SLMOD=1)

6.1.3. Normal State

The Commander Node transmits the clock signal, and the Responder Nodes receive it. In this mode, messages can be transmitted and received via the bus.

6.1.3.1. Normal Mode

Normal Mode indicates that BUS transmission/reception and pin input/output are enabled. After Wake-up operation, it transitions to Normal Mode when it receives a clock from the Commander Node.

■ Transition conditions to Normal Mode:

(1) When a clock is received from Commander Node in Standby Mode.
(2) When an Abnormality detection is canceled in Normal Abnormality Detection Mode.

■ Transition conditions from Normal Mode:

(1) Transition to Deep Sleep Mode when there is a CXPI network error and there is no GPIO_xx output when communication is interrupted. (when IO_SLMOD=1) (Note 1)
(2) Transition to Sleep Mode when there is a CXPI network error and there is no GPIO_xx output when communication is interrupted. (when IO_SLMOD=0).
(3) Transition to Deep Sleep Mode when a Sleep message is received (when IO_SLMOD=1)
(4) Transition to Sleep Mode when a Sleep message is received (when IO_SLMOD=0)
(5) When VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected, transition to Normal Abnormality Detection Mode.

Note 1: When IG input is not detected, it transitions to Deep Sleep Mode, but when IG input is detected, it does not transition to Deep Sleep Mode but to Sleep Mode.

6.1.3.2. Normal Abnormality Detection Mode

When a VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheating is detected while Normal Mode is operating, BUS output and GPIO_xx output are stopped and standby. Refer to 7.6. for details.

■Transition conditions to Normal Abnormality Detection Mode

(1) If VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected in Normal Mode
(2) When a clock is received from Commander Node in Standby Abnormality Detection Mode

■Transition conditions from Normal Abnormality Detection Mode

(1) Transition to Normal Mode when Abnormality detected is canceled.
(2) Transition to Sleep Mode when a Sleep message is received. (When IO_SLMOD=0)
(3) Transition to Deep Sleep Mode when a Sleep message is received. (When IO_SLMOD=1)
(4) Transition to Sleep Mode when a CXPI network error is detected. (when IO_SLMOD=0)
(5) Transition to Deep Sleep Mode when a CXPI network error is detected. (When IO_SLMOD=1)

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6.1.4. Operation Stopped State

Normal operation is impossible and cannot be recovered to normal Mode. All internal clocks, BUS I/O, and IO I/O operations are stopped. This state is maintained until reset.

■Transition to Operation Stopped State

(1) When a 2bit error is detected in non-volatile memory immediately after reset.
(2) When a 2bit error of nonvolatile memory is detected in Dominant Pulse Detect Mode.
(3) When a 2bit error is detected in Sleep monitoring Mode.
(4) When a register memory error is detected for the second time

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6.2. Operation upon Communication interruption

The following state transitions apply when an output function is configured for communication loss conditions. The transitions start from Normal Mode.

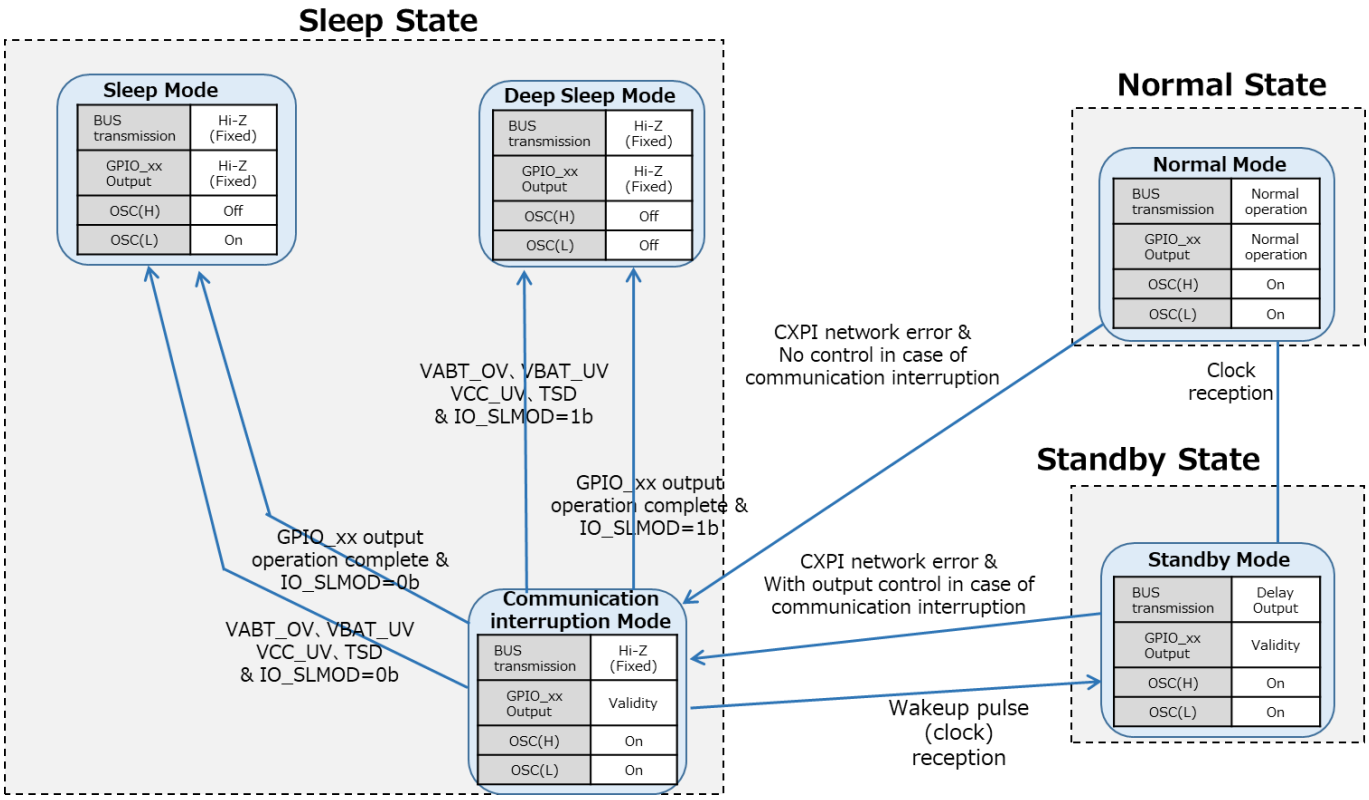


Figure 6.2 State Transition Diagram2

6.2.1. Sleep State

6.2.1.1. Communication interruption Mode

If I/O configuration is set for control when communication interruption, it can transition to the Communication interruption Mode. In the communication interruption Mode, when a CXPI networking error occurs, it is outputted from the specified pin determined by I/O configuration.

■Transition conditions to Communication Interruption Mode:

(1) When there is a CXPI network error in Normal Mode and GPIO_xx is output when communication is interrupted. (including the state where the clock from Commander Node is stopped)
(2) When there is a CXPI network error in Standby Mode and GPIO_xx is output when communication is interrupted.

■Transition conditions from Communication Interruption Mode:

(1) Transition to Standby Mode after receiving 2 times dominant pulses (Wake-up pulse) from BUS. (Note 1)
(2) Transition to Deep Sleep Mode when VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected. (when IO_SLMOD=1)
(3) Transition to Sleep Mode when VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected. (when IO_SLMOD=0)
(4) Transition to Deep Sleep Mode when the output operation is completed and all GPIO_xx have no output operation. (when IO_SLMOD=1)
(5) Transition to Sleep Mode when the output operation is completed and all GPIO_xx have no output operation. (when IO_SLMOD=0)

Note 1: In communication interruption Mode, the reception wait time ($T_{RX_Wakeup_Space_S}$) of Wake-up pulse is disabled, and Wake-up pulse is accepted even after the reception wait time has elapsed.

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6.2.1.2. Deep Sleep Mode

After transition from the communication interruption Mode, the IC operates as described in 6.1. Normal operation.

■Transition conditions to Deep Sleep Mode:

(1) When VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected in communication interruption Mode (when IO_SLMOD=1)

(2) When the output operation is completed in communication interruption Mode and all GPIO_xx do not perform output operation (when IO_SLMOD=1)

6.2.1.3. Sleep Mode

After transition from the communication interruption Mode, the IC operates as described in 6.1. Normal operation.

■Transition conditions to Sleep Mode:

(1) When VBAT overvoltage, VBAT undervoltage, VCC undervoltage, or overheat is detected in the communication interruption Mode (when IO_SLMOD=0)

(2) When the output operation is completed in communication interruption Mode and all GPIO_xx do not perform output operation (when IO_SLMOD=0)

6.2.2. Standby State

6.2.2.1. Standby Mode

After transition from the communication interruption Mode, the IC operates as described in 6.1. Normal operation.

■ Transition conditions to Standby Mode:

(1) When two dominant pulses (Wake-up pulse) are received in the communication interruption Mode

■ Transition conditions from Standby Mode:

(1) Transition to the communication interruption Mode when there is a CXPI network error and GPIO_xx to be output at the time of communication interruption.

Note: If an error is detected during a transition from Communication Interruption Mode to Standby Mode, the GPIO output stops, resulting in a CXPI network error as specified in 6.1.2.1, Standby Mode and no output during communication interruption, and transition to Sleep/Deep Sleep.

6.2.3. Normal State

6.2.3.1. Normal Mode

During Normal operation, a communication interruption (CXPI network error) is detected and the device transitions to the communication interruption Mode.

■ Transition conditions to Normal Mode:

(1) When receives a clock from Commander Node in Standby Mode. (Return from communication interruption Mode)

■ Transition conditions from Normal Mode:

(1) Transition to the communication interruption Mode when there is a CXPI network error and GPIO_xx to be output at the time of communication interruption.

Note: When returning from Communication interruption Mode to Normal Mode, the device immediately starts receiving CXPI frames without waiting for IFS detection. If the Commander Node or another Responder Node is already transmitted on the bus when Normal Mode is re-entered, the received data is treated as an erroneous packet, and a communication error is detected.

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7. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

(T_a = -40 to 125°C unless otherwise specified)

Characteristics	Symbol	Applicable pin	Conditions	Rating	Unit
Supply voltage	V_{VBAT}	VBAT	-	-0.3 to 40	V
	V_{VCC}	VCC	5V power supply for logic	-0.3 to 6	
	V_{VDD}	VDD	1.5V power supply for logic	-0.3 to 2.1	V
5V for ADC	V_{REF}	VREF	VREF≤6V	-0.3 to (V_{VCC} +0.3)	V
Input withstands voltage	V_{GIH} V_{AH}	GPIO_xx ADRx	V_{GIH}≤6V V_{AH}≤6V	-0.3 to (V_{VCC} +0.3)	V
Output withstands voltage	V_{GOH}	GPIO_xx	V_{GOH}≤6V	-0.3 to (V_{VCC} +0.3)	V
I/O withstand voltage	V_{BUS}	BUS	6V≤V_{VBAT}≤18V	-27 to +40	V
Output current	I_{VCC}	VCC	VCC≥4V	-850	mA
Output current	I_{BUS}	BUS	-	200	mA
Storage temperature range	T_{stg}	-	-	-55 to 150	°C
Junction Temperature (Max)	T_J	-	-	150	
Allowable Power Dissipation	PD	-	JEDEC Four-Layer Board Ta = 125°C Thermal Resistance 30.8°C/W	0.81	W

Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.
If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.
Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

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8. Electrical Characteristics

8.1. IC Overall

Table 8.1 IC Overall

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
VBAT						
VBAT normal operating area	V_{VBAT}	VBAT	6	12	18	V
Current Consumption (Dark Current)	I_{VBAT_DSLP}	BUS=V_{VBAT} Deep Sleep Mode ADRx: Internal pull-down	-	13	-	μA
Current Consumption (Sleep Mode)	I_{VBAT_SLPMOD}	BUS=V_{VBAT} Sleep Mode ADRx: Internal pull-down	-	18	-	μA
Current consumption (Normal Mode)	I_{VBAT_NORM}	Normal Mode	-	-	8	mA
Undervoltage protection	V_{VBAT_UV}		4.5	-	5.9	V
Filter time for low voltage detection	T_{VBAT_UV}	Same as detection/release Low-voltage pre-detection is also similar	5	9	18	μs
Undervoltage detect Hysteresis	V_{VBAT_UVHYS}		-	0.4	-	V
Overvoltage detection voltage	V_{VBAT_OV}		25	-	28	V
Filter time for overvoltage detection	T_{VBAT_OV}	Same as detection/release The same applies to the prior detection of overvoltage.	5	10	18	μs
Overvoltage detects Hysteresis	V_{VBAT_OVHYS}			1		V
Pre-detection of VBAT overvoltage	$V_{VBATFNH}$	Function operation only Design warranty	20.5	-	23.5	V
Hysteresis of overvoltage pre-detection	$V_{VBAT_PREOVHYS}$		-	1	-	V
Pre-detection of VBAT undervoltage	$V_{VBATFNL}$	Function operation only Design warranty	5	-	6	V
Hysteresis of low-voltage pre-detection	$V_{VBAT_PREUVHYS}$		-	0.4	-	V
Slew rate at VBAT power up	T_{VBAT_SLOPE}		0.01	-	2	V/μs
Time-to-transition to Sleep/Deep Sleep after VBAT power-on	T_{MODE_START}		-	-	5	ms
VCC(5V)						
VCC output-voltage	V_{VCC}		4.8	-	5.2	V
Current limit 1	I_{VCC_LIM1}	Normal Mode (VCC≥4V)	220	-	850	mA
Current limit 2	I_{VCC_LIM2}	Normal Mode (VCC≤3V) or Standby Mode	10	-	220	mA
VCC Drop	$V_{VCCDROP}$	Drop between VBAT-VCC V_{VBAT}= 4.5 V、 I_{OUT}= -50mA			0.5	V
Undervoltage protection	V_{VCC_UV}		4.0	-	4.5	V
Filter time for low voltage detection	T_{VCC_UV}	Same as detection/release	5	15	20	μs
Undervoltage detect Hysteresis	V_{VCC_UVHYS}		-	0.3	-	V

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POR detected	V_{VCC_POR}		3.0		3.9	V
POR detecting Hysteresis	V_{VCC_PORHYS}		-	0.15	-	V
Overvoltage detection voltage	V_{VCC_OV}		5.2		5.8	V
Filter time for overvoltage detection	T_{VCC_OV}	Same as detection/release	5	14	19	µs
Overvoltage detects Hysteresis	V_{VCC_OVHYS}		-	0.1	-	V
VDD (1.5V)						
VDD output-voltage	V_{VDD}		1.45	1.5	1.55	V
Current consumption (Normal)	I_{VDD}	VDD=1.5V	-	-	5	mA
POR detected	V_{VDD_POR}		1.25	-	1.4	V
POR detecting Hysteresis	V_{VDD_PORHYS}		-	50	-	mV
Overvoltage detection voltage	V_{VDD_OV}		1.55	-	1.65	V
Filter time for overvoltage detection	T_{VDD_OV}	Same as detection/release	2.5	10	35	µs
Overvoltage detect Hysteresis	V_{VDD_OVHYS}		-	10	-	mV

8.2. Temperature characteristics

Table 8.2 Temperature characteristics

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
Operating temperature						
Operating temperature	T_A		-40	-	125	°C
Overheat detection (TSD)						
Overheat detection	T_{TSD}		150	170	190	°C
Cancel Detection	T_{TSD_REL}		135	-	175	°C
Overheat Detect Hysteresis	T_{TSD_HYS}		-	10	-	°C
Filter time for overheat detection	T_{TSD_TIME}	Same as detection/release The same applies to the prior detection of overheating.	5	13	20	µs
Pre-detection of overheating	T_{TSDFN}		125	-	175	°C
Overheat pre-detection Hysteresis	T_{TSD_PREHYS}		-	10	-	°C

8.3. Oscillator

Table 8.3 Oscillator

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
Oscillator						
High-speed oscillator	HOSC	With trimming	7.2	8	8.8	MHz
Low-speed oscillator	LOSC	With trimming	28.8	32	35.2	kHz

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8.4. Nonvolatile memories

Table 8.4 Nonvolatile memories

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
Memory controller						
Data retention				15		Year
Waiting time for writing data to memories when setting IO	T_{Write}	Time from the Save Configuration response until completion of memory writing (1 erase operation + 4 write operations)	-	-	100	ms
Number of writes		Number of writes after deletion	-	-	15	times

8.5. Sleep monitoring duration

Table 8.5 Sleep monitoring duration

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
Sleep monitoring						
Monitoring On times	T_{WAON}	Set time of IO_WAON [1:0]	281.25	-	653.125	µs
Incoming MASK times during the monitoring On times	T_{MASK}	T_{WAON} - T_{SAMPLE}	84.375	-	412.5	µs
Input-Sample Judgment and Result-Processing Time during Monitoring On Time	T_{SAMPLE}	32 kHz OSC × (7 clocks)	-	218.75	-	µs

8.6. I/O pin

Table 8.6 I/O pin

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
GPIO_xx: Digital Input						
Line High	V_{GIH}		0.8xV_{VCC}	-	-	V
Input LOW voltage	V_{GIL}		-	-	0.2xV_{VCC}	V
Pull-up resistor 1	R_{GPU1}		50	100	200	kΩ
Pull-up resistor 2	R_{GPU2}		1.7	3.4	6.8	kΩ
Pull-Down resistor 1	R_{GPD1}		50	100	200	kΩ
Pull-Down resistor 2	R_{GPD2}		1.7	3.4	6.8	kΩ
GPIO_xx: Digital Output						
High voltage	V_{GOH}	Load current =-2 mA	0.8xV_{VCC}	-	-	V
Low voltage	V_{GOL}	Load current =2 mA	-	-	0.2xV_{VCC}	V

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GPIO_xx: Switch Matrix						
High Side MOS setting	R_{SMH}	Load current = -1 mA	100	200	500	Ω
Pull-up resistor	R_{SMPU}	-	1.7	3.4	6.8	kΩ
Low Side MOS setting	R_{SML}	Load current = 20 mA	5	30	70	Ω
GPIO_00, GPIO_01: IG Input						
Transitional times from IG to Sleep Mode	T_{IG}	IG detected from Deep Sleep Mode and transitioned to Sleep Mode	-	-	2	ms
ADRx						
Line High voltage	V_{AH}		0.8xV_{VCC}	-	-	V
Input LOW voltage	V_{AL}		-	-	0.2xV_{VCC}	V
Pull-Down resistor	R_{APD}		-	50	-	kΩ

8.7. AD circuit

Table 8.7 AD converter circuit

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
AD converter						
Operating voltage	V_{ADC}		4.8	5	5.2	V
Overall error	ADerr	VREF=VCC =5V	-3.5	-	3.5	LSB

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8.8. BUS (DC Characteristics)

Table 8.8 BUS(DC Characteristics)

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
BUS Dominant output voltage	V_{OL_BUS}	V_{TXD} = 0V, R_L(Note 1) = 500Ω 6V ≤ V_{BAT} < 7.3V	-	-	1.2	V
		V_{TxD}= 0V, R_L = 500Ω 7.3V ≤V_{VBAT} ≤ 10V	-	-	0.2x V_{VBAT}	V
		V_{TxD} = 0V, R_L = 500Ω 10V ≤V_{VBAT} ≤ 18V	-	-	2.0	V
Current (DC) when BUS shorting	I_{BUS_LIM}	V_{BUS} = V_{VBAT} = 18V	40	-	200	mA
Leak current when BUS dominant	$I_{BUS_PAS_dom}$	V_{BUS} = 0V, V_{VBAT} = 12V	-1	-	-	mA
Leak current when BUS recessive	$I_{BUS_PAS_rec}$	8V<V_{VBAT} < 18V, 8V<V_{BUS} < 18V, V_{BUS} > V_{VBAT}	-	-	20	µA
Leak current at ground disconnection	$I_{BUS_NO_GND}$	GND= V_{VBAT}、0 V < VBUS < 18 V V_{VBAT} = 12 V	-1	–	1	mA
Leak current when power is OFF	$I_{BUS_NO_VBAT}$	V_{VBAT} = 0V, 0 V < V_{BUS} < 18 V	–	–	100	µA
Dominant threshold voltage when receiving	V_{BUSdom}	Voltage judged by the receiving Node to be Low	–	-	0.423× V_{VBAT}	V
Recessive threshold voltage when receiving	V_{BUSrec}	Voltage judged by the receiving Node to be High	0.556× V_{VBAT}	-	-	V
Center voltage when receiving	V_{BUSCNT}	V_{BUSCNT}= (V_{th_dom} +V_{th_rec})/2 V_{th_dom} = measured Dominant thresholds during reception V_{th_rec} = measured Recessive thresholds during reception	0.475×V_{VBAT}	0.5× V_{VBAT}	0.525 ×V_{VBAT}	V
Hysteresis	V_{BUShys}	V_{BUShys}= V_{th_rec} - V_{th_dom}	-	-	0.133 ×V_{VBAT}	V

Note1: R_L is a pull-up resistance between VBAT and BUS externally connected to the IC.

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8.9. BUS (AC Characteristics)

8.9.1. Wakeup Pulse Transmission/Reception

Table 8.9 Wakeup Pulse Transmission/Reception

(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, 1Tbit=50μs, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
Dominant detection time when receiving Wake-up	T_{rx_wakeup}	TH_{rx_dom} = 0.423 × V_{VBAT} (Fig. 8.1.)	0.5	2.75	5	μs
BUS dominant time when transmitting Wake-up	T_{tx_wakeup}	TH_{tx_dom} = 0.3 × V_{VBAT} TH_{tx_rec} = 0.7 × V_{VBAT}	400	800	2500	μs
Interval times for Wake-up transmission	$T_{tx_wakeup_space}$	Time to transmit the second dominant pulse of Wake-up pulse	5	7.5	10	ms
Waiting time to receive Wakeup pulses	$T_{RX_Wakeup_Space_S}$	After Dominant pulse detect Mode transitions, wait time for reception of Wake-up pulsing (dominant twice)	70	120	170	ms
Waiting time for second dominant reception of Wakeup pulses	$T_{RX_Wakeup_Space}$	Second reception wait after the first dominant reception of Wake-up pulse Time	15	-	32	ms
Recognition time for receiving Wakeup pulses (twice dominant)	$T_{RX_Wakeup_Detect_S}$	When Wake-up signal (dominant twice) is received after Dominant pulse detect Mode transitions.	-	-	1.6	ms
Waiting time to transmit Wakeup pulse again	$T_{TX_Wakeup_Recovery_S}$	The delay between transmitting Wake-up pulse and transmitting it again	60	120	250	ms
Transition time to Sleep Mode	$T_{RX_Sleep_S}$	Transitions to Sleep Mode after Sleep message received	25	35	50	ms
Transition time to Normal Mode	$T_{RX_Normal_S}$	Duration from clock-reception to Normal Mode transitions in Standby Mode	-	-	20	ms

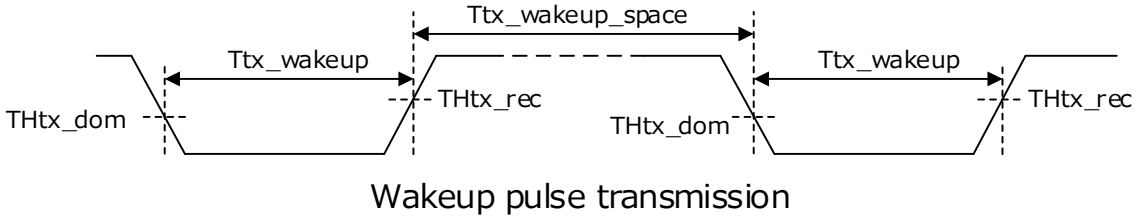


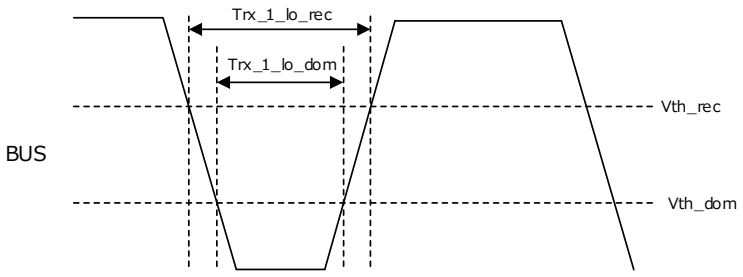
Figure 8.1 Wake-up pulsed

8.9.2. Transmission/Reception in Normal Mode

Table 8.10 Transmission/Reception in Normal Mode

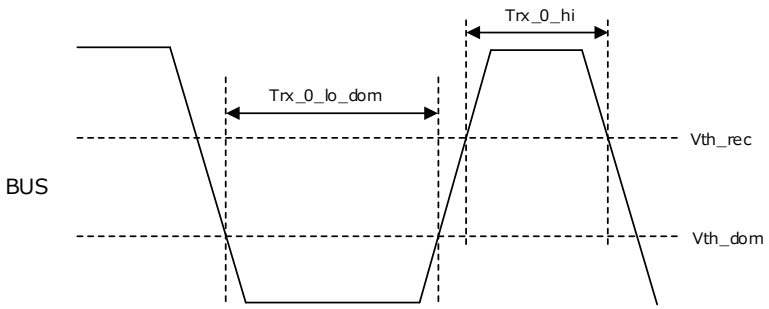
(V_{VCC} = 4.8 to 5.2V, V_{VBAT} = 6 to 18 V, Ta =-40 to 125 °C, 1Tbit=50μs, unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ.	Max	
When receiving Normal Mode						
BUS dominant time of logical 1 at reception	$T_{rx_1_lo_dom}$	C_{BUS}=1 nF、R_{BUS}=1kΩ V_{th_dom}=0.423 × V_{VBAT}	5.5	-	-	μs
BUS recessive time of logical 1 at reception	$T_{rx_1_lo_rec}$	C_{BUS}=10 nF、R_{BUS}=500 Ω V_{th_rec}=0.556 × V_{VBAT}	-	-	22.5	μs
BUS dominant time of logical 0 in reception	$T_{rx_0_lo_dom}$	C_{BUS}=1 nF、R_{BUS}=1kΩ V_{th_dom}=0.423 × V_{VBAT}	8.5	-	-	μs
BUS recessive time of logical 0 at reception	$T_{rx_0_hi}$	C_{BUS}=1 nF、R_{BUS}=1kΩ V_{th_rec}=0.556 × V_{VBAT}	3	-	-	μs
When transmitting Normal Mode						
BUS dominant time of logic 0 at transmit	$T_{tx_0_lo_dom}$	C_{BUS}=1 nF、R_{BUS}=1kΩ TH_{tx_dom} = 0.3 × V_{VBAT}	8.5	-	-	μs
BUS recessive duration of logic 0 at transmit	$T_{tx_0_hi}$	C_{BUS}=10 nF、R_{BUS}=500 Ω TH_{tx_rec} = 0.7 × V_{VBAT}	1	-	-	μs
CXPI networking error	T_{NETERR}	7.5.3.2. Reference	4	7	10	s
Response times of UDSonCXPI	$T_{RESPONSE}$	Time until Response after Request reception of UDSonCXPI	0	-	500	ms



On reception: BUS width of logic 1

Fig. 8.2 BUS time in logical 1 reception



On reception: BUS width of logic 0

Fig. 8.3 BUS time in logical 0 reception

8.10. Others

Table 8.11 Others

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min	Typ.	Max	
Chattering filter						
Input decision time of the chattering filter	T_{IN_FIX}	Chattering filter sampling period (ms) = T_{IN} Number of sampling times of chattering filter (times) = N	T_{IN} × N	T_{IN} × (N+0.5)	T_{IN} × (N+1)	ms
Others						
BUS internal resistance	$R_{Responder}$	VBAT to BUS Resistance	20	30	60	kΩ
BUS inner diode voltage drop	V_F	Diode between VBAT and BUS	0.25	0.5	1.0	V
Allowable capacitance of Responder Node	$C_{Responder}$	Design warranty	-	220	250	pF
BUS allowable capacitance 1	C_{BUS}	R_L=1kΩ	-	-	1	nF
BUS allowable capacitance 2	C_{BUS}	R_L=660Ω	-	-	4	nF
BUS allowable capacitance 3	C_{BUS}	R_L=500Ω	-	-	10	nF

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9. Application Circuit Example

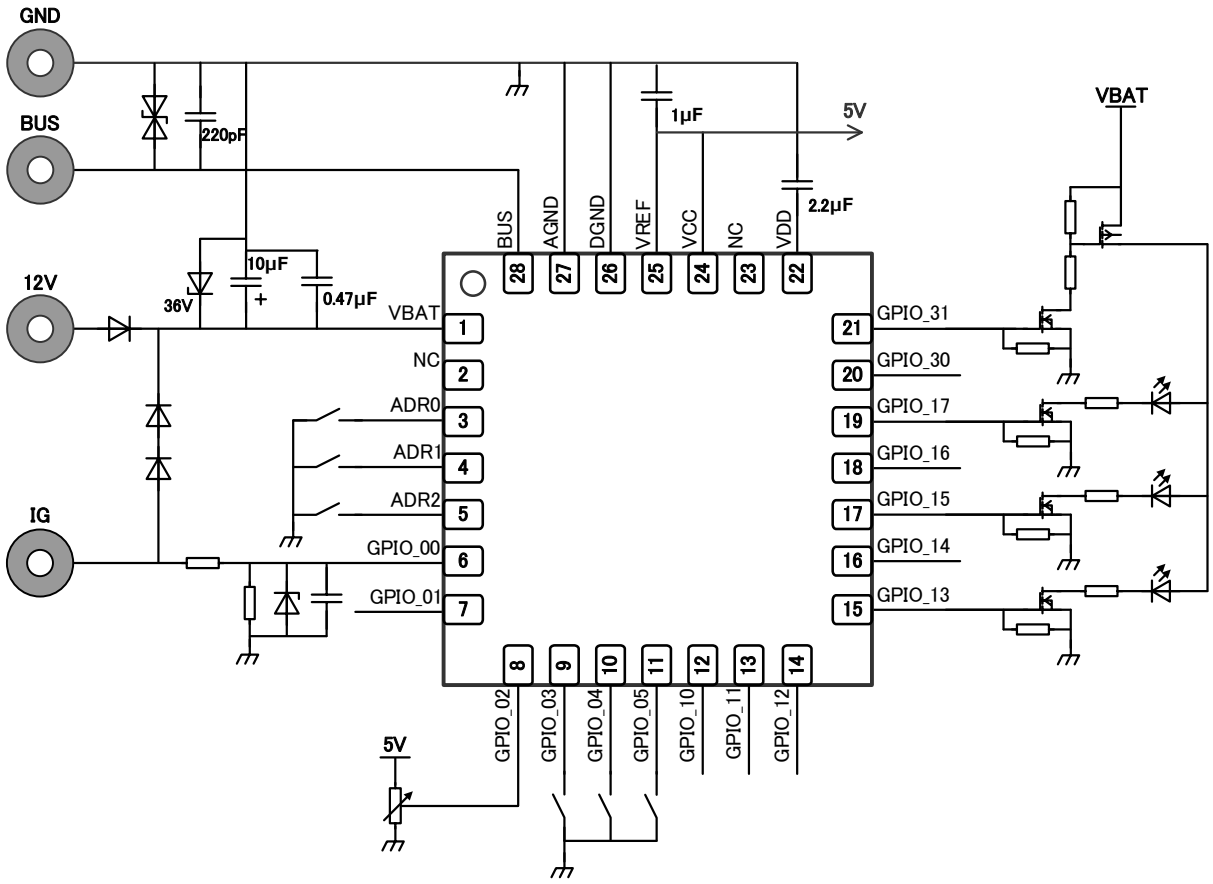


Figure 9.1 Application circuit diagram1

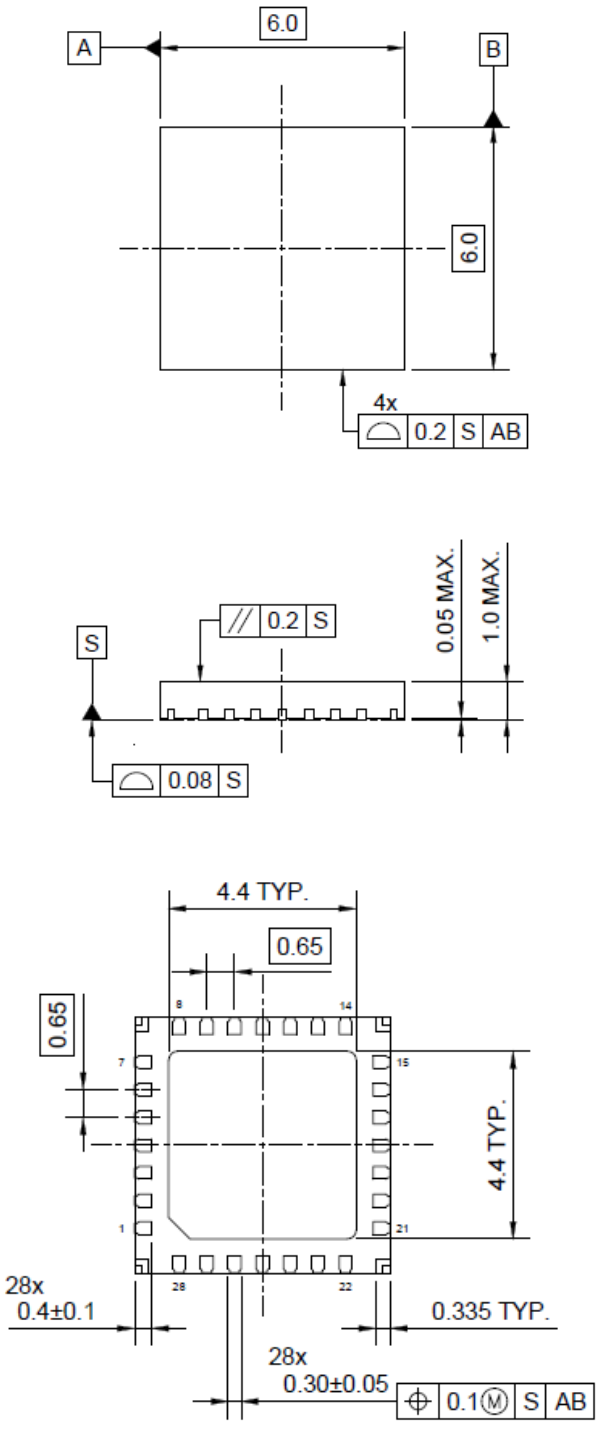
Note: Unless otherwise specified, Typ. values are assumed. (Characteristic tolerances consider resistor tolerances of ±5% ±200 ppm/°C, electrolytic capacitor tolerances of ±20%, and ceramic capacitor tolerances of ±5%.)

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10. Package Dimensions

● P-VQFN28-0606-0.65-003

Unit: mm



Mass: 0.1 g (typ.)

Figure 10.1 Package Dimensions

11. Change History

Ver	Specification items	Specification changes	Issue Date
1.0	-	Create New	2026/10/30

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12. Notes On Handing of ICs

(1) The block diagrams used in this specification are for explaining the functions and operations, and some may be omitted or simplified.

(2) The equivalent circuit diagrams used in this specification are for explaining the functions and operations, and some may be omitted or simplified.

(3) The timing charts used in this specification are for explaining the functions and operations and may be partially omitted or simplified.

(4) The maximum rating is a standard that must not be exceeded instantaneously. Exceeding the max. rating may result in breakage, degradation or damage of IC, and may cause damage other than IC. Design the product so that the maximum rating is not exceeded under any operating conditions.
Use the product within the operating range described in the manual.

(5) The components in the application circuit examples are not guaranteed to be free from malfunctions or malfunctions of applied devices.
When selecting parts, perform an application evaluation sufficiently and confirm that there is no problem before use.

(6) Avoid incorrect mounting. Doing so may damage IC or the equipment.

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