Automotive CXPI Communication Application Circuit

Design Guide

RD254-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This design guide (hereinafter referred to as “this guide”) describes the reference design (hereinafter referred to as “this design”) for automotive CXPI (Clock Extension Peripheral Interface) communication application circuits using the TB9032FNG (driver/receiver IC) and TB9033FTG (CXPI interface IC).

CXPI is a next-generation Automotive communication protocol established by the Society of Automotive Engineers of Japan and standardized by the International Organization for Standardization (ISO) as ISO 20794:2020. The protocol was developed to reduce the increase in wiring harnesses associated with communication between HMI (Human Machine Interface) devices and to contribute to overall vehicle weight reduction.

Traditionally, automotive networks have widely adopted LIN (Local Interconnect Network) communication for controlling components such as door mirrors and LED lighting. In contrast, next-generation CXPI communication offers both low cost and high responsiveness, contributing to efficient control of automotive functions. This design is created with these application scenarios in mind.

This design consists of a CXPI commander node and multiple CXPI responder nodes. The commander node connects to a host controller and performs communication transmission and reception using a CXPI driver/receiver board equipped with the TB9032FNG, the CXPI physical-layer IC. Commands from the host controller are delivered to each responder node through the CXPI bus via the CXPI driver/receiver board.

For responder nodes, this design provides the following two types of control boards:

- Door mirror drive board for door mirror applications
- LED ambient light drive board for ambient lighting applications

Both boards incorporate the TB9033FTG as the CXPI responder interface IC.

The door mirror board includes an MCD (motor control driver) and MOSFETs to perform door mirror opening/closing operations, mirror angle adjustment, and Blinker control. The LED ambient light board uses the GPIO output pins of the TB9033FTG, enabling dimming control by adjusting the PWM duty cycle.

This design can be used as a reference for verifying CXPI communication operation and evaluating the functions of each responder node. It can be used as a reference example in the development and evaluation of automotive endpoint control systems utilizing CXPI communication.

2. Next-Generation Automotive Communication Protocol: CXPI

This section provides an overview of CXPI, the next-generation Automotive communication standard used in this design.

CXPI (Clock Extension Peripheral Interface) is a next-generation automotive communication protocol developed by the Society of Automotive Engineers of Japan and internationally standardized in 2020 as ISO 20794. It was designed to support communication between devices in the HMI (Human Machine Interface) domain, such as switches and sensors where high responsiveness is required.

Traditionally, input/output devices inside vehicles were connected in a one-to-one configuration, leading to an increase in wiring harnesses and consequently greater vehicle weight. CXPI adopts a single-wire bus architecture, achieving lower cost compared with CAN (Controller Area Network) while providing responsiveness that cannot be achieved with LIN (Local Interconnect Network). This enables both weight reduction through harness minimization and improved efficiency through multiplex communication.

The main features of CXPI are as follows:

- Communication method: PWM modulation + clock synchronization
- Access method: CSMA/CR (event-triggered) + commander/responder schedule (polling)
- Physical layer: Single-wire bus, maximum communication speed of 20kbps
- Data transfer: 12byte normal frame, up to 255byte burst frame
- Reliability: Error detection using CRC
- Scalability: Up to 16 nodes; easy node addition and removal

With these features, CXPI is well suited for body-control applications that require both high responsiveness and low cost, such as steering switches, wipers, lighting systems, door mirrors, and seat control.

Details of CXPI are available on the website *"Automotive Network Communication"*; please refer to it for more information.

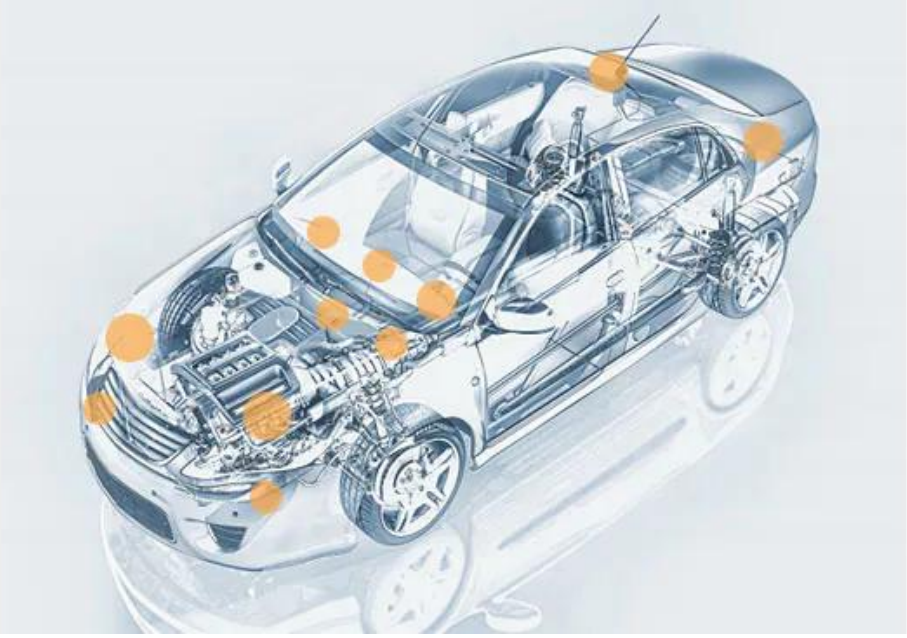


Fig 2.1 Application Overview

3. Reference Design Configuration

This design explains the configuration of an automotive control system that adopts CXPI (Clock Extension Peripheral Interface), as well as the roles of each node using Toshiba ICs.

CXPI is a communication standard optimized for body-control functions such as door mirrors and LED lighting, featuring low cost through a single-wire bus and high responsiveness.

This design consists of the following three main blocks. A block diagram is shown in Figure 3.1.

- **CXPI Commander Node (A) — CXPI Driver/Receiver Board**

  The RD254A board incorporates the CXPI driver/receiver IC TB9032FNG. When combined with a host controller equipped with a CXPI controller, it functions as the CXPI commander node. This configuration enables reliable communication with the CXPI bus.

- **CXPI Responder Node (B) — Door Mirror Drive Board**

  The RD254B board adopts the TB9033FTG as a CXPI interface IC. In combination with an MCD (Motor Control Driver) and MOSFETs, it enables control of multiple motors and the Blinker integrated in the door mirror.

- **CXPI Responder Node (C) — LED Ambient Light Drive Board**

  The RD254C board also uses the TB9033FTG and is responsible for controlling the LED ambient lighting. It drives multiple LED ambient lights through MOSFETs, contributing to improved comfort inside the vehicle.

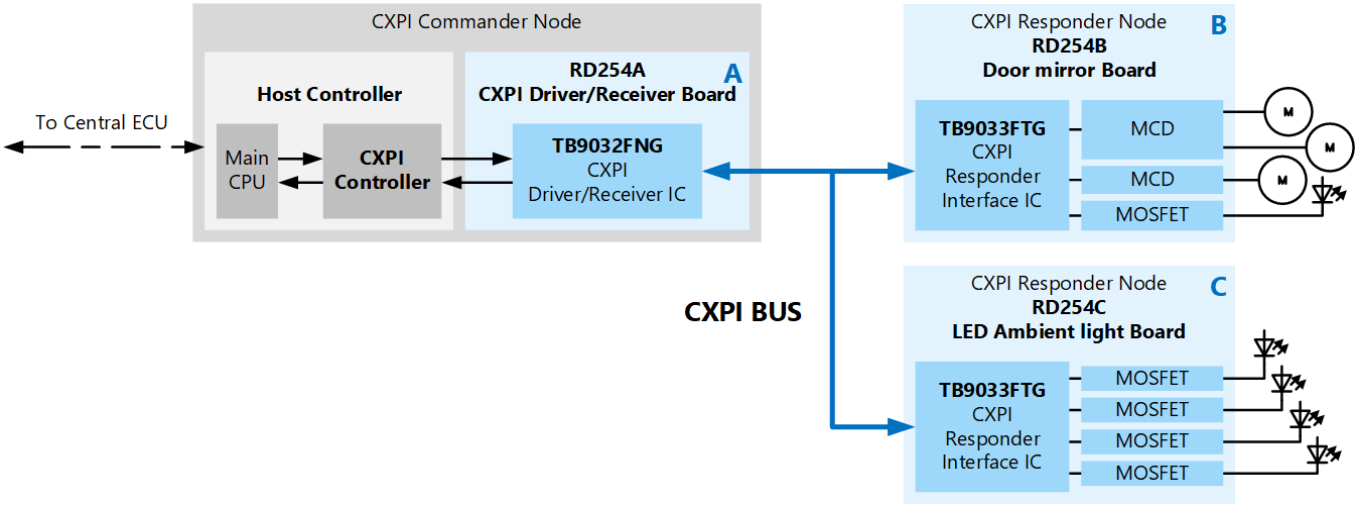


Fig 3.1 Block Diagram

4. A CXPI Driver/Receiver Board (Commander Node)

4.1. Specifications and Block Diagram

Table 4.1 shows the main specifications of the RD254A board used in this design.

Table 4.1 RD254A Board Specifications

Item	Condition	Min	Typ.	Max	Unit
Power					
VBAT Voltage		6	12	16	V
VIO		4.5	5	5.5	V
RXD					
Output HIGH Voltage	Load current -1mA, V_{VIO} = 5V	4.5	-	-	V
Output LOW Voltage	Load current 1mA	-	-	0.5	V
TXD					
Input HIGH Voltage	VVIO = 5V	4.0	-	-	V
Input LOW Voltage	VVIO = 5V	-	-	1.0	V
Hysteresis	VVIO = 5V	0.16	0.325	0.65	V
Bus (DC Characteristics)					
Dominant Output Voltage	V_{TXD}=0V, R_L*= 500Ω 10V ≤ VBAT ≤ 18V	-	-	2.0	V
Recessive Output Voltage	TXD=H	0.8 x VBAT	-	VBAT	V
Dominant Voltage at Reception	Voltage at which the receiving node determines Low level	-	-	0.423 x VBAT	V
Recessive Voltage at Reception	Voltage at which the receiving node determines High level	0.556 x VBAT	-	-	
Hysteresis		-	-	0.133 x VBAT	V
Other Settings					
Board Layer Structure	FR-4, 2 layers (through-hole via), PCB thickness 1.6mm, Cu thickness 35µm (surface layer)				
Board Size	65mm x 55mm				

* R_L is the external pull-up resistor between the BAT and BUS lines.

Fig 4.1 presents the main block diagram of the RD254A board in the proposed design.

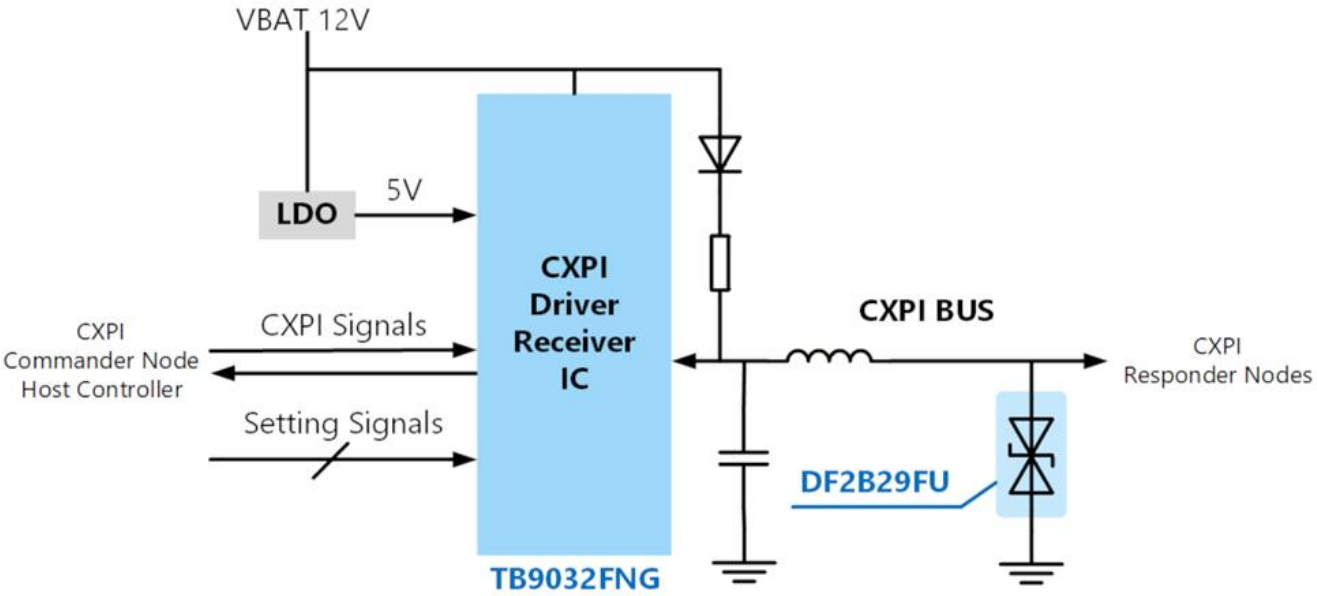


Fig 4.1 RD254A Block Diagram

4.2. Main Components Used

This section describes the main components used on the RD254A board in this design.

4.2.1. CXPI Driver/Receiver IC TB9032FNG

In this design, the CXPI communication driver/receiver IC TB9032FNG is used in the bus circuit on the commander side. This device complies with ISO 20794-4 and allows switching between commander node and responder node operation by means of external pins.

The main features of the TB9032FNG are as follows:

- CXPI communication driver/receiver IC
- Operating voltage (VBAT): 6 to 18V
- Microcontroller interface voltage: 4.5 to 5.5V
- Operating temperature (Ta): −40 to 125 °C
- Junction temperature (Tj): 150 °C (max)
- Sleep mode and wake-up transmission mode
- Dominant timeout detection function
- Overtemperature detection and undervoltage detection functions (BAT, VIO)
- Communication speed: up to 20kbps

Appearance and Pin Layout

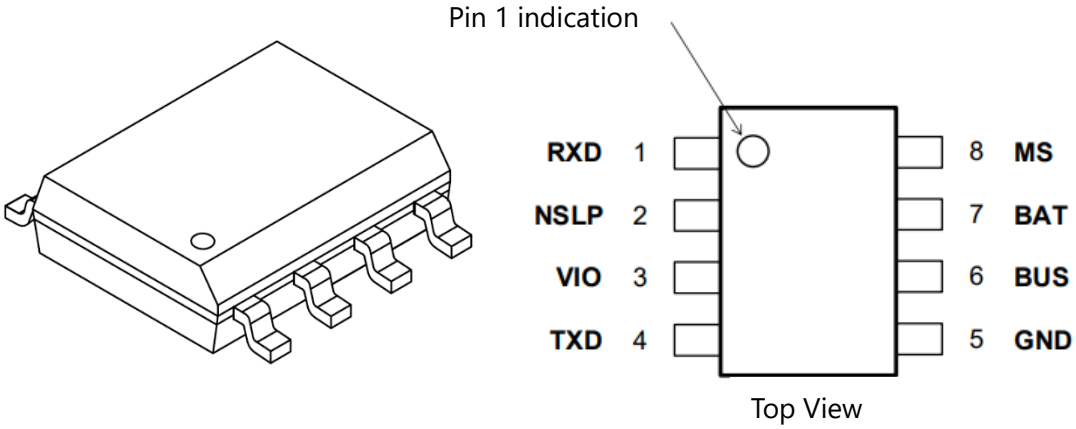


Fig 4.2 TB9032FNG Appearance and Pin Layout

Pins Specifications

Table 4.2 TB9032FNG Pin Specifications

No.	Pin	Withstand Voltage (V)	I/O	Pull Up/Down	Description
1	RXD	6	O	-	Output pin for CXPI signals received from the bus
2	NSLP	6	I	Pull down	Normal mode: Input High Sleep mode or wake-up transmission mode: Input Low
3	VIO	6	I	-	5V interface supply
4	TXD	6	I	Pull up	Input pin for CXPI signals transmitted to the bus
5	GND	-	-	-	GND
6	BUS	40	I/O	-	CXPI communication bus pin
7	BAT	40	I	-	Connected to battery
8	MS	40	I	-	Commander node: Input High Responder node: Input Low

Block Diagram

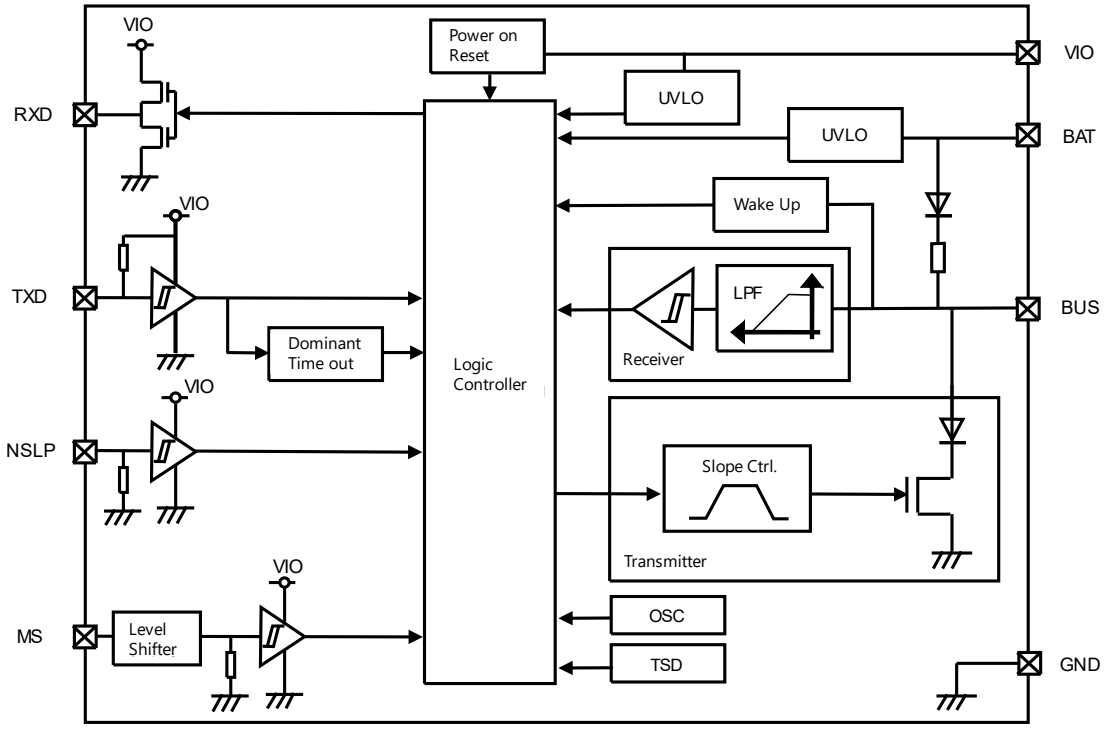


Fig 4.3 TB9032FNG Block Diagram

4.2.2. TVS Diode DF2B29FU

In the CXPI bus circuit, the bidirectional ESD protection diode DF2B29FU is used to protect against electrostatic discharge (ESD).

The main features of the DF2B29FU are as follows:

- Reverse breakdown voltage: VBR = 26V (min) (Measurement condition: IBR = 1 mA)
- Suitable for CAN/LIN interfaces and power supply applications
- AEC-Q101 compliant

Appearance and Pin Layout

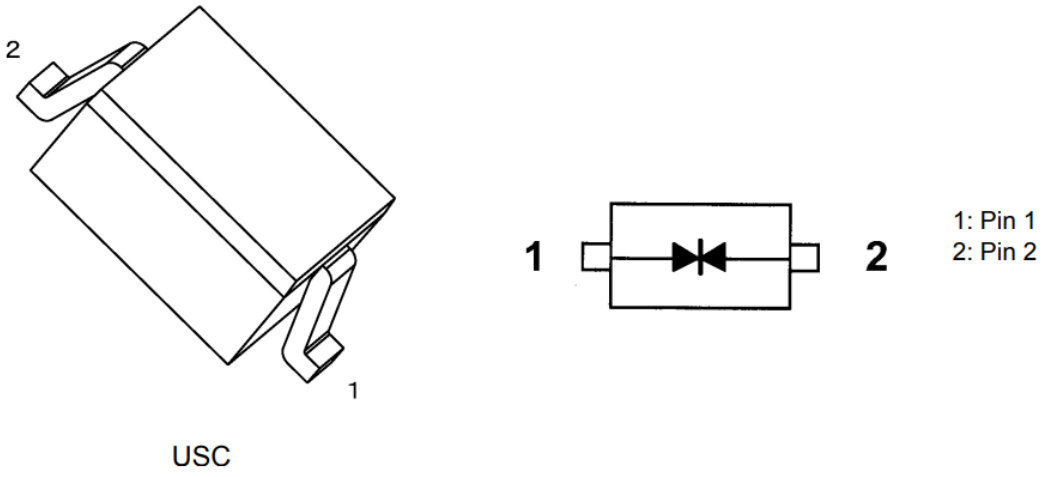


Fig 4.4 DF2B29FU Appearance and Pin Layout

4.3. Circuit Design

This section describes the key points of the circuit design for each part of the RD254A board used in this design.

4.3.1. Power Supply Circuit

The power supply circuit is designed to withstand transient noise and meet EMC requirements in automotive environments, while providing a stable power supply to the CXPI communication module. The automotive power supply VBAT is used, and a filtering configuration is adopted to reduce transient noise and ripple before supplying power to the internal circuits of the module. A two-stage filtering configuration consisting of capacitors and an inductor is employed to reduce noise over a wide frequency range and ensure high reliability. In addition, an LED indicator is provided to allow easy visual confirmation of the power status.

The output power is divided into two supply lines: BUS/MS and VIO generated by the regulator, which are supplied to communication and control circuits.

Connector Section (CON1)

Pin 1 is GND and pin 2 is VBAT, assuming connection to the vehicle power supply.

EMC-Compliant Filtering Section (C1, C2, C3, C4, L1)

Capacitors C1 (0.1μF) and C2 (100μF / 50V) are decoupling capacitors placed immediately after VBAT.

C1 is used to remove high-frequency noise, while C2 absorbs low-frequency ripples. This combination reduces noise over a wide frequency range.

Inductor L1 (2mH) is inserted in series with the power supply line to suppress noise.

Capacitors C3 (0.1μF) and C4 (100μF / 50V) are placed downstream of L1 to form the second-stage filtering.

C3 bypasses high-frequency components to GND, and C4 absorbs residual ripple to ensure a stable DC voltage.

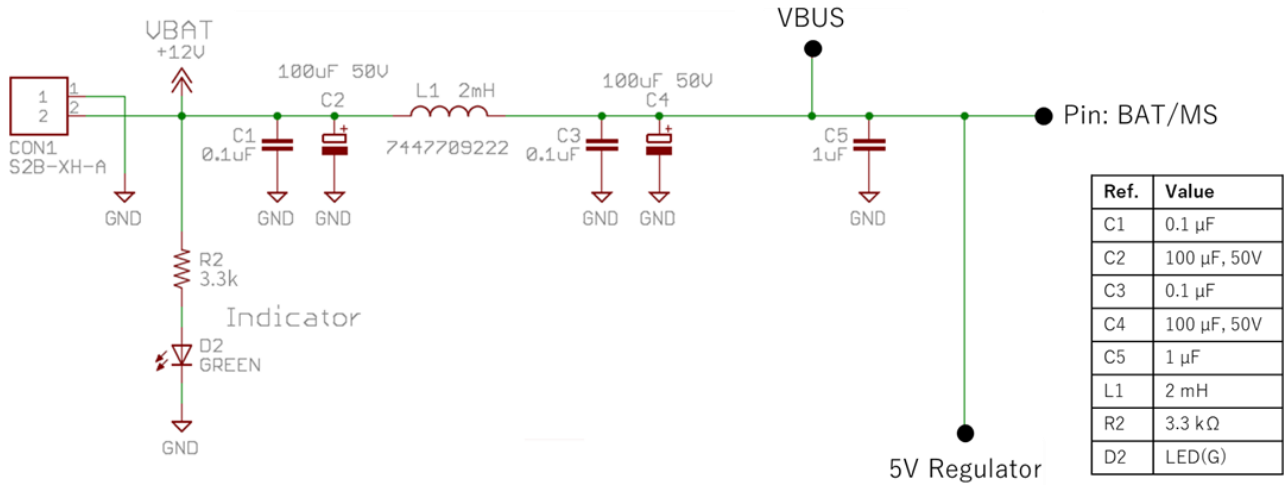
Regulator Power Supply Section (C5)

Capacitor C5 (1μF) absorbs high-frequency noise and stabilizes the power supply line.

Placing C5 close to the input side of the regulator ensures stable regulator operation.

Indicator Section (R2, D2)

When the power is turned on, the green LED D2 lights up, allowing the VBAT supply status to be visually confirmed.



Ref.	Value
C1	0.1 μF
C2	100 μF, 50V
C3	0.1 μF
C4	100 μF, 50V
C5	1 μF
L1	2 mH
R2	3.3 kΩ
D2	LED(G)

Fig 4.5 Power Supply Circuit Diagram

4.3.2. CXPI BUS Signal Circuit

This circuit is a signal circuit for configuring the BUS line in accordance with the CXPI standard.

In this design, the circuit provides the basic functions required for CXPI communication bus bias generation, protection, and EMC countermeasures to ensure reliable operation in an automotive environment. Key design points include ESD protection, noise reduction using ferrite beads and capacitors, and stabilization of the recessive bus level using a pull-up resistor. In addition, a spare pad for C6 is provided to allow flexible tuning during EMC optimization.

Connector Section (CON2)

BUS signals (transmit/receive) are connected via the 2-pin connector CON2 from an external harness.
Pin 1 is GND and pin 2 is the signal line, assuming connection to the vehicle side.

Circuit Protection Section (ZD1: DF2B29FU)

ZD1 is an ESD protection diode placed adjacent to the connector section. It protects the circuit against air discharge. The DF2B29FU TVS diode manufactured by Toshiba is used to minimize the impact on communication signals.

EMC Countermeasure Section (L2, C7, C6)

L2 is a ferrite bead that attenuates high-frequency noise. It is designed to maintain low impedance in the communication frequency band so as not to degrade signal quality.

Capacitor C7 (220pF) provides BUS capacitance and works in combination with L2 to bypass high-frequency noise to GND.

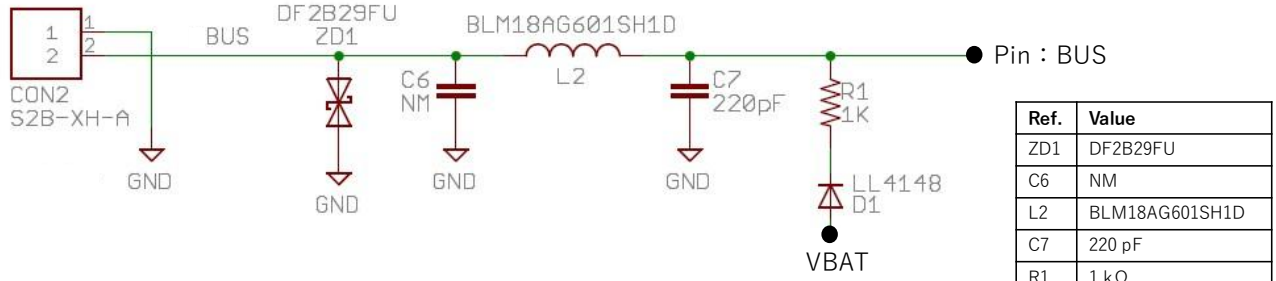
C6 (NM: Not Mounted) is provided as a spare pad for EMC performance adjustment. Depending on the EMC requirements, either a 220pF capacitor may be mounted on C6 or C7, or capacitors may be placed on both so that the combined capacitance of C6 and C7 totals 220pF.

Bus Bias Generation Section (R1, D1) *Commander node only

Resistor R1 (1kΩ) is used as an external BUS resistor to pull up the BUS line to VBAT, maintaining the recessive state (high level). It also limits the current flowing into the CXPI bus, preventing damage due to overcurrent or short-circuit conditions.

Diode D1 is inserted between the BUS and VBAT. When the ECU loses the battery supply (loss of battery), current may flow back from the CXPI bus into the ECU, potentially causing an uncontrolled power-up. D1 prevents this reverse current and blocks the ECU from being powered via the CXPI bus.

* This design is intended for use with a commander node, and these components are not required when used in a responder node configuration.



Ref.	Value
ZD1	DF2B29FU
C6	NM
L2	BLM18AG601SH1D
C7	220 pF
R1	1 kΩ
D1	LL4148

Fig 4.6 CXPI BUS Signal Circuit Diagram (Commander node)

4.3.3. Control Signal Circuit

This circuit is configured to process signals related to CXPI communication and is intended for power stabilization, communication signal input/output, and generation of control signals.

The main components and design intent are described below. The circuit supports the PWM signals, NSLP control signal, and mode switching via the MS pin required for CXPI communication, while supplying a stable +5V power (VIO). Key features include power stabilization using a regulator, physical-layer communication via the IC, and flexible mode configuration using switches and jumpers.

Connector Section (CON3)

Connector CON3 is a 4-pin connector that provides RXD (receive data), TXD (transmit data), NSLP (sleep control), and GND to external devices.

It serves as an interface to an automotive ECU or an external control unit.

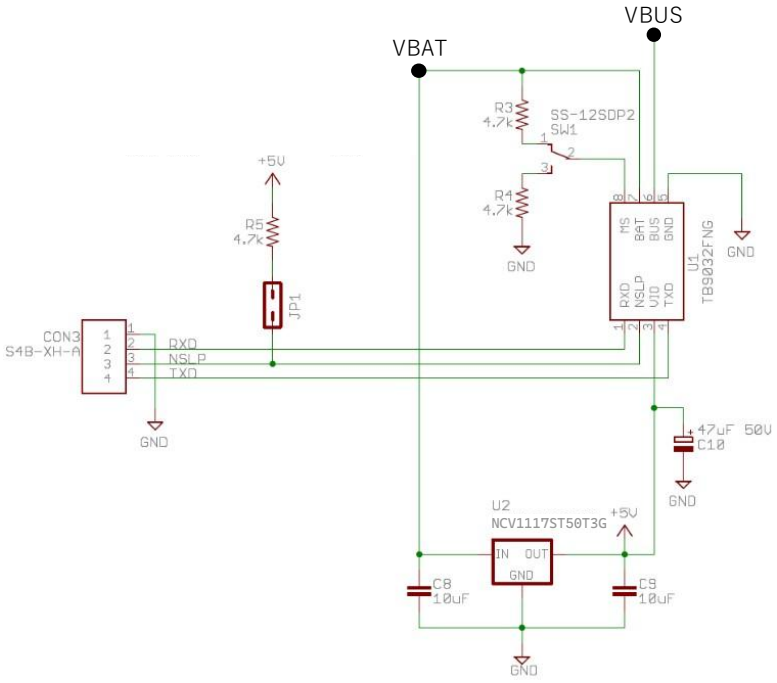
Power Stabilization Section

A linear regulator generates VIO (+5V) from VBAT. Capacitor C8 (10μF) is placed on the input side and C9 (10μF) on the output side to suppress ripple and ensure stable operation. In addition, C10 (47μF / 50V) is added to the +5V line to enhance voltage stability under load fluctuations.

Control Signal Generation Section (RXD/TXD, NSLP, MS)

These signals are used between the CXPI driver/receiver IC TB9032FNG and the host controller.

- **RXD**: Outputs the CXPI signal received from the CXPI BUS to the host controller.
- **TXD**: Inputs the CXPI signal to be transmitted onto the CXPI BUS from the host controller.
- **NSLP**: Controls the operating mode of the TB9032FNG. When High is applied, the IC enters Normal mode.When Low is applied, the IC enters Sleep mode or Wake-up transmission mode.
  In this design, the NSLP line can be pulled up to 5 V by shorting jumper JP1. When controlling the NSLP line using an open-drain output from the host controller, connect the output pin to the NSLP pin of connector CON3 and short JP1. Alternatively, if the NSLP line is fixed to High, leave the NSLP pin of CON3 open and short JP1.
- **MS**: Selects Commander node mode or Responder node mode. In this design, the mode can be switched using the manual switch SW1.



Ref.	Value
R3	4.7 kΩ
R4	4.7 kΩ
R5	4.7 kΩ
C8	10 μF
C9	10 μF
C10	47 μF, 50V
U1	TB9032FNG
U2	NCV1117ST50T3G

Fig 4.7 Control Signal Circuit Diagram

5. B Door Mirror Drive Board (Responder Node)

5.1. Specifications and Block Diagram

Table 5.1 shows the specifications of the RD254B board used in this design.

Table 5.1 RD254B Board Specifications

Item	Condition	Min.	Typ.	Max.	Unit
Power					
VBAT voltage		7	12	16	V
VCC		4.8	5	5.2	V
BUS					
Dominant Voltage at Reception	Voltage at which the receiving node determines Low level	-	-	0.423 x VBAT	V
Recessive Voltage at Reception	Voltage at which the receiving node determines High level	0.556 x VBAT	-	-	V
Hysteresis		-	-	0.133 x VBAT	V
GPIO_xx: Digital Input					
Input HIGH Voltage	VCC = 5V	4	-	-	V
Input LOW Voltage	VCC = 5V	-	-	1	V
GPIO_xx: Digital Output					
Output HIGH Voltage	Load current = -2mA, VCC = 5V	4	-	-	V
Output LOW Voltage	Load current = 2mA, VCC = 5V	-	-	1	V
AD converter					
Operating Voltage		4.8	5	5.2	V
Door Mirror Adjustment Motor Drive (Motor 1, Motor 2)					
Output Current		-	0.5	1	A
Output ON Resistance		-	1.2	2.4	Ω
Door Mirror Folding Motor drive (Motor 3)					
Output Current	2ch coupling mode	-	-	10	A
Output ON Resistance	2ch coupling mode	-	100	125	mΩ
Blinker LED Drive					
LED drive Voltage	Depends on VBAT	7	12	16	V
LED drive Current		-	-	200	mA
Other settings					
Board Layer Structure	FR-4, 2 layers (through-hole via), PCB thickness 1.6mm, Cu thickness 35µm (surface layer)				
Board Size	100mm x 100mm				

Fig 5.1 shows the block diagram of the RD254B board used in this design.

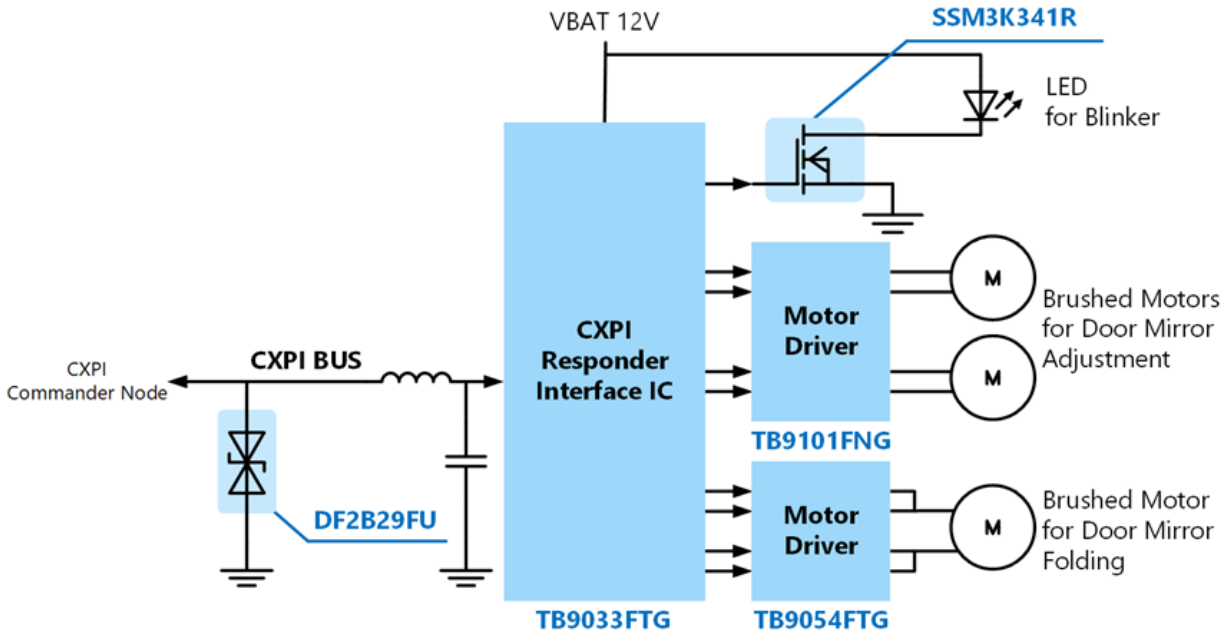


Fig 5.1 RD254B Block Diagram

Table 5.2 shows the control signal connection specifications of the RD254B board used in this design.

Table 5.2 RD254B Board Control Signal Connection Specifications

IC	Pins	GPIO (TB9033FTG)	Specifications
TB9054FTG	**ENB1/2**	**GPIO_00**	Digital Output
	EN1/2	**GPIO_01**	Digital Output
	SLEEPB	**GPIO_02**	Digital Output
	CM1	**GPIO_03**	ADC
	CM2	**GPIO_04**	ADC
-	**-**	**GPIO_05**	-
TB9101FNG	**DI1A**	**GPIO_10**	Digital Output
	DI1B	**GPIO_11**	Digital Output
	DG1	**GPIO_12**	Digital Input
	DI2A	**GPIO_13**	Digital Output
	DI2B	**GPIO_14**	Digital Output
	DG2	**GPIO_15**	Digital Input
Blinker	**-**	**GPIO_16**	PWM
-	**-**	**GPIO_17**	-
TB9054FTG	**PWM2**	**GPIO_30**	PWM
	PWM1	**GPIO_31**	PWM

5.2. Main Components Used

This section describes the main components used on the RD254B board in this design.

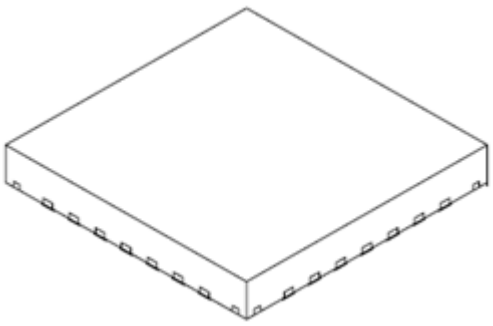
5.2.1. CXPI Interface IC TB9033FTG

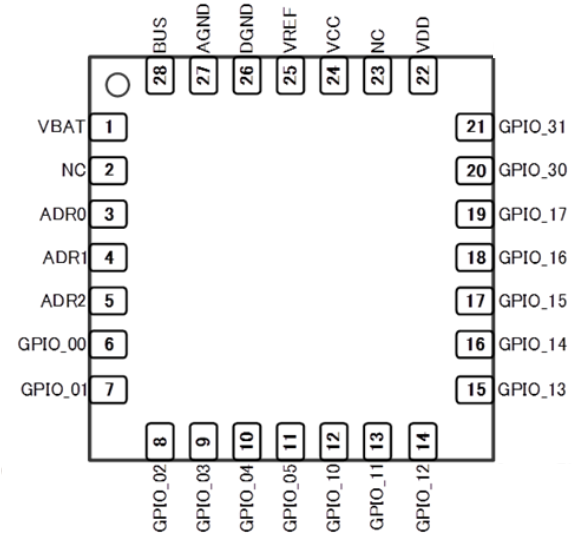
In this design, the automotive CXPI responder interface IC TB9033FTG, which incorporates hardware logic, is used in the bus circuit on the responder node. The TB9033FTG provides 16-channel GPIOs, of which 6 channels can be configured as A/D converter inputs and 4 channels can be configured as PWM outputs.

The main features of the TB9033FTG are as follows:

- CXPI communication interface IC compliant with CXPI (ISO20794-2 to -4, ISO14229-8)
- 16-channel GPIO I/O pins: 6 channels: A/D converter inputs (10-bit, 1 ADC Circuit),
  4 channels: PWM outputs (8-bit, 4 PWM Circuits)
- Input specifications
  - Input ON/OFF detection (event transmission)
  - Chattering filter (configurable time and count)
  - Input monitoring during Sleep mode
  - Switch matrix (up to 4 x 4)
  - Moving average processing for ADC (configurable time and count)
- Output specifications
  - Output ON/OFF control (configurable time and count)
  - Output control in the event of communication loss
  - PWM frequency setting (200Hz to 22kHz)
- Built-in overtemperature, overvoltage, and undervoltage detection circuits
- Current consumption in Deep Sleep mode: 10μA (Typ.)
- Operating supply voltage range: 6 to 18V(Absolute maximum rating: 40V)
- Operating temperature range: −40 to 125°C

Appearance and Pin Layout





Top View

Fig 5.2 TB9033FTG Appearance and Pin Layout

Pin Description

Table 5.3 TB9033FTG Pin Specifications

No.	Pin	Withstand Voltage (V)	I/O	Description
1	**VBAT**	40	I	Power supply pin
2	**NC**	-	-	Unused pin
3	**ADR0**	6	I	Node Address configuration pin
4	**ADR1**	6	I	Node Address configuration pin
5	**ADR2**	6	I	Node Address configuration pin
6	**GPIO_00**	6	I/O	IN/OUT or ADC
7	**GPIO_01**	6	I/O	IN/OUT or ADC
8	**GPIO_02**	6	I/O	IN/OUT or ADC
9	**GPIO_03**	6	I/O	IN/OUT or ADC
10	**GPIO_04**	6	I/O	IN/OUT or ADC
11	**GPIO_05**	6	I/O	IN/OUT or ADC
12	**GPIO_10**	6	I/O	IN/OUT or Switch matrix
13	**GPIO_11**	6	I/O	IN/OUT or Switch matrix
14	**GPIO_12**	6	I/O	IN/OUT or Switch matrix
15	**GPIO_13**	6	I/O	IN/OUT or Switch matrix
16	**GPIO_14**	6	I/O	IN/OUT or Switch matrix
17	**GPIO_15**	6	I/O	IN/OUT or Switch matrix
18	**GPIO_16**	6	I/O	IN/OUT, Switch matrix, or PWM
19	**GPIO_17**	6	I/O	IN/OUT, Switch matrix, or PWM
20	**GPIO_30**	6	I/O	IN/OUT or PWM
21	**GPIO_31**	6	I/O	IN/OUT or PWM
22	**VDD**	2.1	O	1.5V regulator output and power supply for 1.5V logic
23	**NC**	-	-	Unused pin
24	**VCC**	6V	O	5V regulator output and power supply for 5V logic
25	**VREF**	6V	I	5V input for ADC
26	**DGND**	-	-	Digital GND pin
27	**AGND**	-	-	Analog GND pin
28	**BUS**	40V	I/O	CXPI BUS pin

GPIO Description

Table 5.4 TB9033FTG GPIO Specifications

No.	Pin	Digital I/O	ADC	PWM	Chattering filter	Input monitoring in Sleep	Output monitoring in Sleep	IG det.	SW Matrix	Output control during communication loss
1	**GPIO_00**	✓	✓	-	✓	-	✓	✓	-	-
2	**GPIO_01**	✓	✓	-	✓	-	✓	✓	-	-
3	**GPIO_02**	✓	✓	-	✓	-	✓	-	-	-
4	**GPIO_03**	✓	✓	-	✓	-	✓	-	-	-
5	**GPIO_04**	✓	✓	-	✓	-	✓	-	-	-
6	**GPIO_05**	✓	✓	-	✓	-	✓	-	-	-
7	**GPIO_10**	✓	-	-	✓	✓	✓	-	✓	✓
8	**GPIO_11**	✓	-	-	✓	✓	✓	-	✓	✓
9	**GPIO_12**	✓	-	-	✓	✓	✓	-	✓	✓
10	**GPIO_13**	✓	-	-	✓	✓	✓	-	✓	✓
11	**GPIO_14**	✓	-	-	✓	✓	✓	-	✓	✓
12	**GPIO_15**	✓	-	-	✓	✓	✓	-	✓	✓
13	**GPIO_16**	✓	-	✓	✓	✓	✓	-	✓	✓
14	**GPIO_17**	✓	-	✓	✓	✓	✓	-	✓	✓
15	**GPIO_30**	✓	-	✓	✓	-	✓	-	-	✓
16	**GPIO_31**	✓	-	✓	✓	-	✓	-	-	✓

Block Diagram

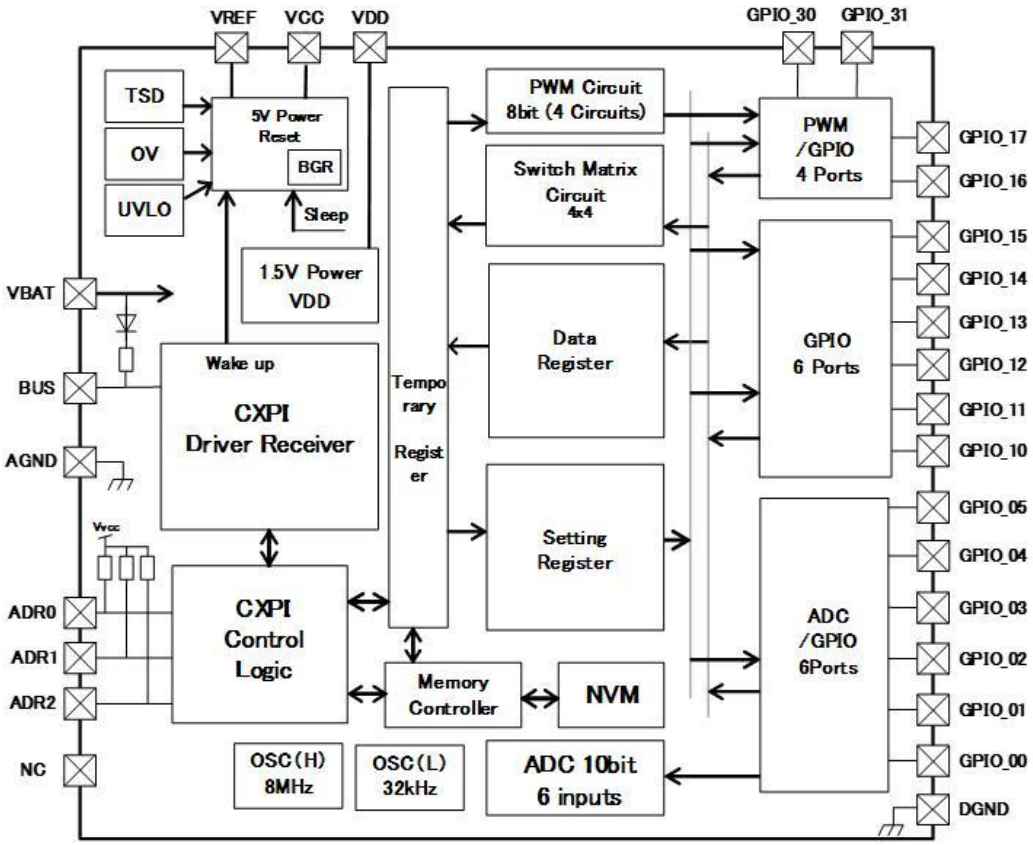


Fig 5.3 TB9033FTG Block Diagram

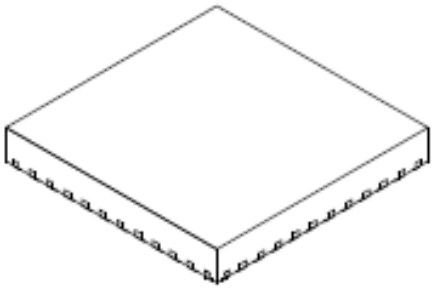
5.2.2. MCD Automotive H-Bridge Driver TB9054FTG

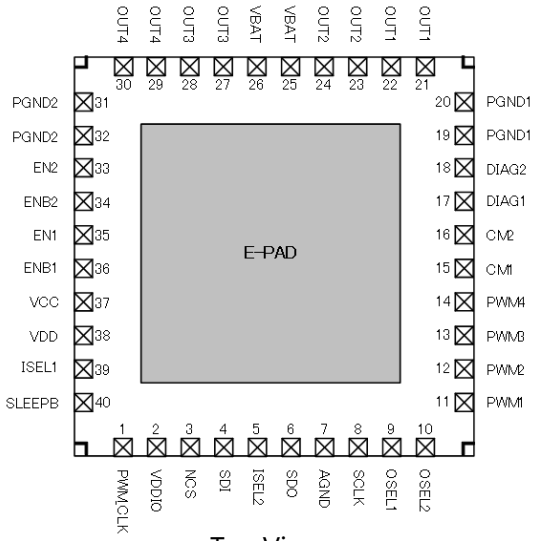
In this design, the automotive PWM-type 2-channel H-bridge DC brushed motor control driver (MCD) IC TB9054FTG is used in the motor control circuit for door mirror folding (open/close) on the responder side.

The main features of the TB9054FTG are as follows:

- 2-channel H-bridge driver
  - ON resistance: RON (Nch + Nch) < 350mΩ (max) (Measurement conditions: Tj = 150 °C, VBAT = 8V)
  - Selectable configurations: 2-channel mode / 2-channel combined mode, 1-channel H-bridge, or 4-channel half-bridge
- Fault detection functions: Overcurrent detection, Overtemperature detection, VBAT undervoltage detection, VCC undervoltage detection, Power supply fault detection (VBAT undervoltage, VCC undervoltage)
- Built-in diagnostic functions
- PWM-controlled output
- Forward / reverse / brake operation
- Current limit control using a chopper current limiting method
- High-side output current monitoring function (CM1 pin, CM2 pin)
- Load open detection function (during operation / non-operation)
- DIAG outputs (DIAG1 pin, DIAG2 pin)
- H-bridge / half-bridge mode selection function (OSEL1 pin, OSEL2 pin)
- Low-power Sleep mode
- Built-in shoot-through prevention circuit
- AEC-Q100 / AEC-Q006 compliant
- SPI communication: Notification of various fault detections, Configuration of operating modes, Motor drive control via SPI
- Operating voltage range: VBAT = 4.5 to 28V (Absolute maximum rating: 40V),
  VCC = 4.5 to 5.5V, VDDIO = 3.0 to 5.5V
- Operating temperature range: Ta = −40 to 125 °C

Appearance and Pin Layout





Top View

Fig 5.4 TB9054FTG Appearance and Pin Layout

5.2.3. MCD Automotive H-Bridge Driver TB9101FNG

In this design, the output-driver-integrated MCD (Motor Control Driver) IC TB9101FNG, which directly drives small automotive DC brushed motors, is used in the motor control circuit for door mirror adjustment on the responder side.

The main features of the TB9101FNG are as follows:

- Built-in 2-channel H-bridge driver
  - ON resistance: R_{HON} (Pch) = 0.6Ω (Typ.), R_{LON} (Nch) = 0.6Ω (Typ.)
- Standby current: 0 mA (Typ.)
- Operating voltage range: Supply voltage: 7 to 18V (Absolute maximum rating: 40V)
- Operating temperature (Ta): −40 to 125 °C
- Fault detection functions: Motor overcurrent detection, VCC overvoltage detection, VCC undervoltage detection, Internal IC overtemperature detection
- AEC-Q100 compliant

Appearance and Pin Layout

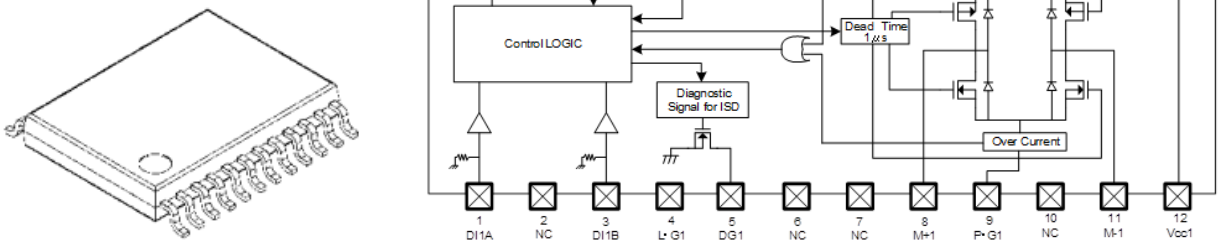


Fig 5.5 TB9101FNG Appearance and Pin Layout

5.2.4. N-Channel MOSFET SSM3K341R

In this design, the N-channel MOSFET SSM3K341R is used for Blinker control of the door mirror.
The main features of the SSM3K341R are as follows:

- AEC-Q101 compliant
- Low ON resistance
  - $R_{DS(on)}$ = 28mΩ (Typ.) @ V_{GS} = 10V
  - $R_{DS(on)}$ = 36mΩ (Typ.) @ V_{GS} = 5.0V
  - $R_{DS(on)}$ = 43mΩ (Typ.) @ V_{GS} = 4.5V

Appearance and Pin Layout

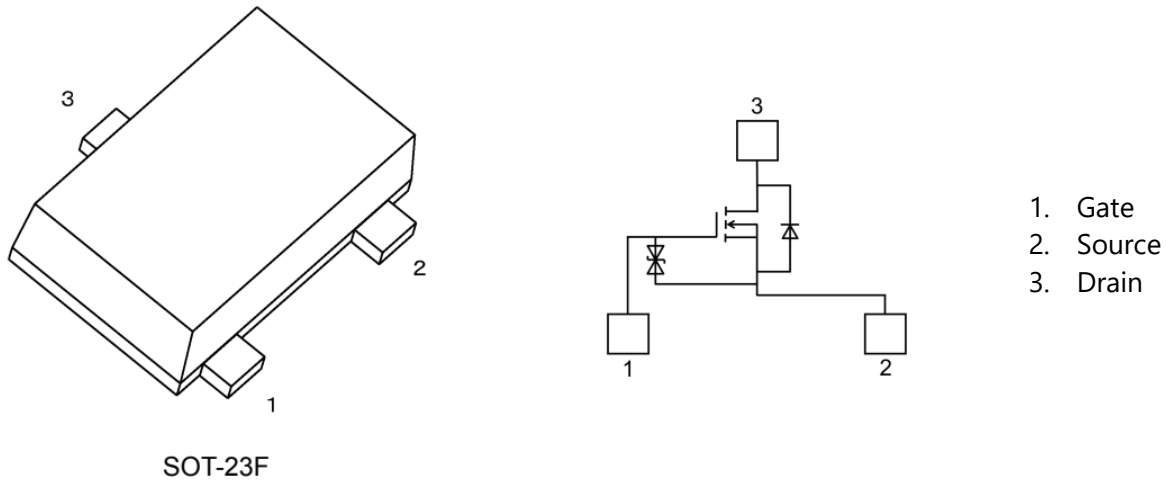


Fig 5.6 SSM3K341R Appearance and Pin Layout

5.2.5. TVS Diode DF2B29FU

In this design, the bidirectional ESD protection diode DF2B29FU is used to protect the CXPI BUS circuit against electrostatic discharge (ESD).

For details of this component, please refer to the previous section, *"4.2.2 TVS Diode DF2B29FU"*.

5.3. Circuit Design

This section describes the key points of the circuit design for each part of the RD254B board used in this design.

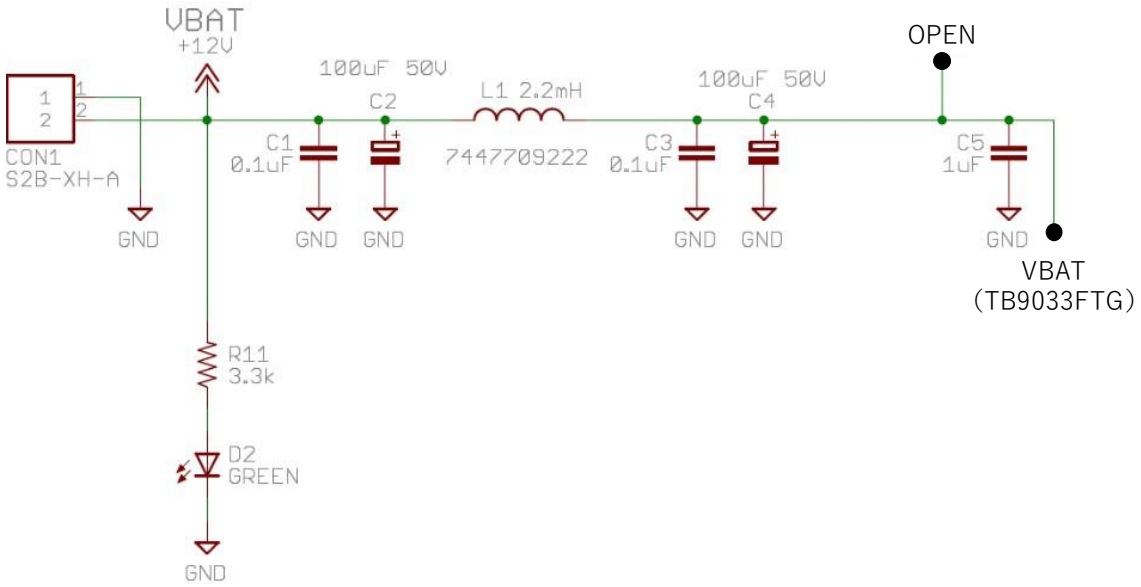
5.3.1. Power Supply Circuit

This circuit is designed to provide a stable power supply to the CXPI communication module, the motor control drivers (MCDs) for door mirror control, and the Blinker LED in automotive system.

Power Supply Circuit for the CXPI Communication Module (TB9033FTG)

This circuit supplies power to the CXPI communication module (TB9033FTG). The connector section, the EMC-compliant filtering circuit, and the indicator circuit are based on the same design as the power supply circuit used for the CXPI driver/receiver board.

For details, please refer to Section *"4.3.1. Power Supply Circuit"*.



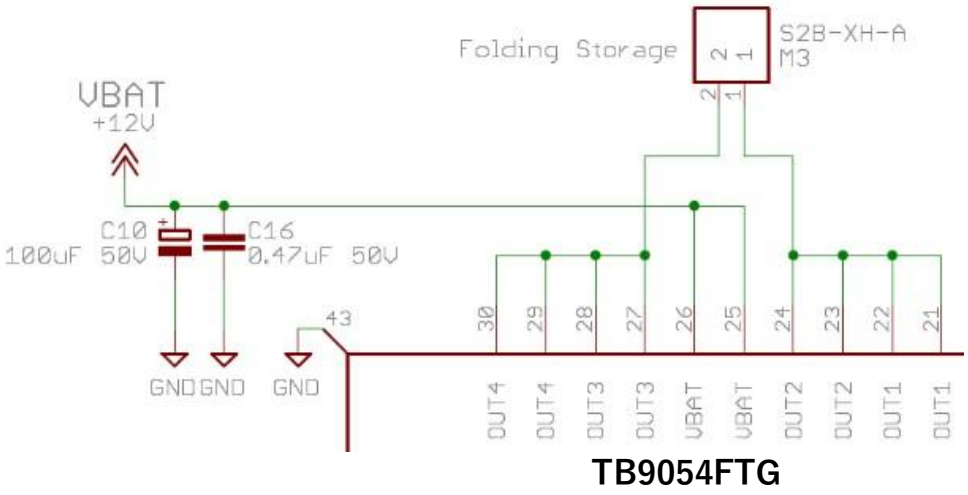
Ref.	Value
C1	0.1 µF
C2	100 µF, 50V
C3	0.1 µF
C4	100 µF, 50V
C5	1 µF
L1	2.2 mH
R11	3.3 kΩ
D2	LED(G)

Fig 5.7 VBAT Power Supply Circuit for TB9033FTG

Power Supply Circuit for the Door Mirror Folding Motor Control MCD (TB9054FTG)

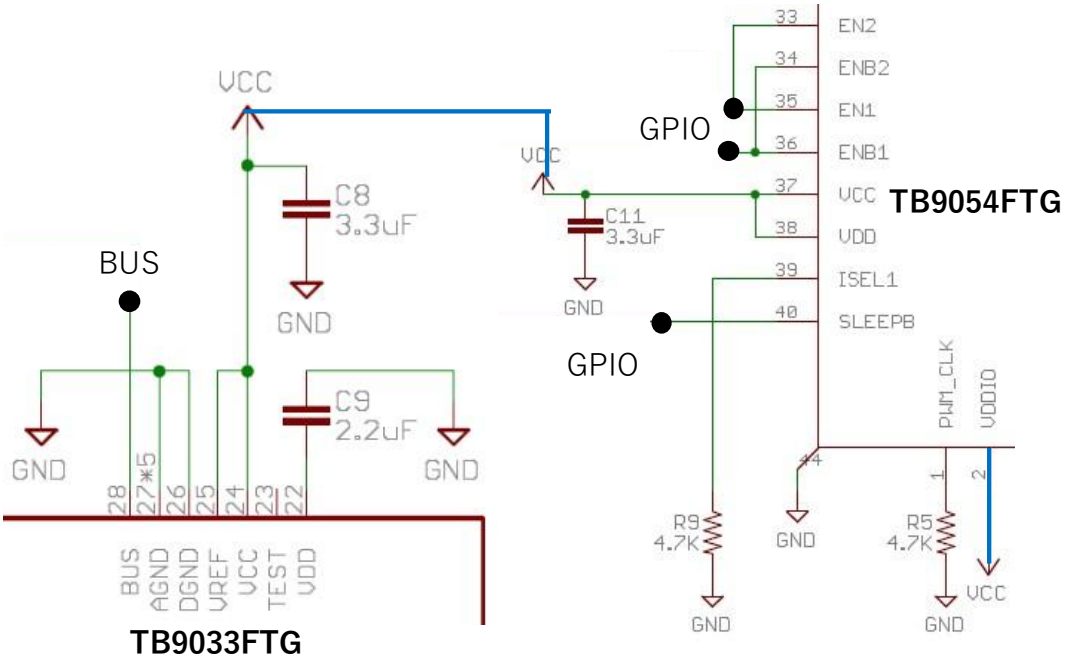
This circuit is configured to provide a stable automotive power supply VBAT to the system including the motor driver IC TB9054FTG. VBAT is supplied from the vehicle battery and provides power to the motor driver IC as well as to multiple output lines (OUT1 to OUT4), serving as the reference power source for motor drive and control signals. Capacitor C10 (100µF) is primarily used to absorb low-frequency fluctuations in the power supply and stabilize the voltage. Capacitor C16 (0.47µF) is a decoupling capacitor for removing high-frequency noise. By placing these two capacitors in parallel, noise and voltage fluctuations over a wide frequency range are suppressed, ensuring stable operation of downstream circuits and external loads.

In addition, to supply stable VCC and VDDIO power to the motor driver IC from the VCC output of the CXPI interface IC TB9033FTG module, decoupling capacitors C8 and C11 (3.3µF each) are placed on the VCC line. This configuration provides effective noise reduction and voltage stabilization.



Ref.	Value
C10	100 µF, 50V
C16	0.47 µF, 50V

Fig 5.8 VBAT Power Supply Circuit for TB9054FTG



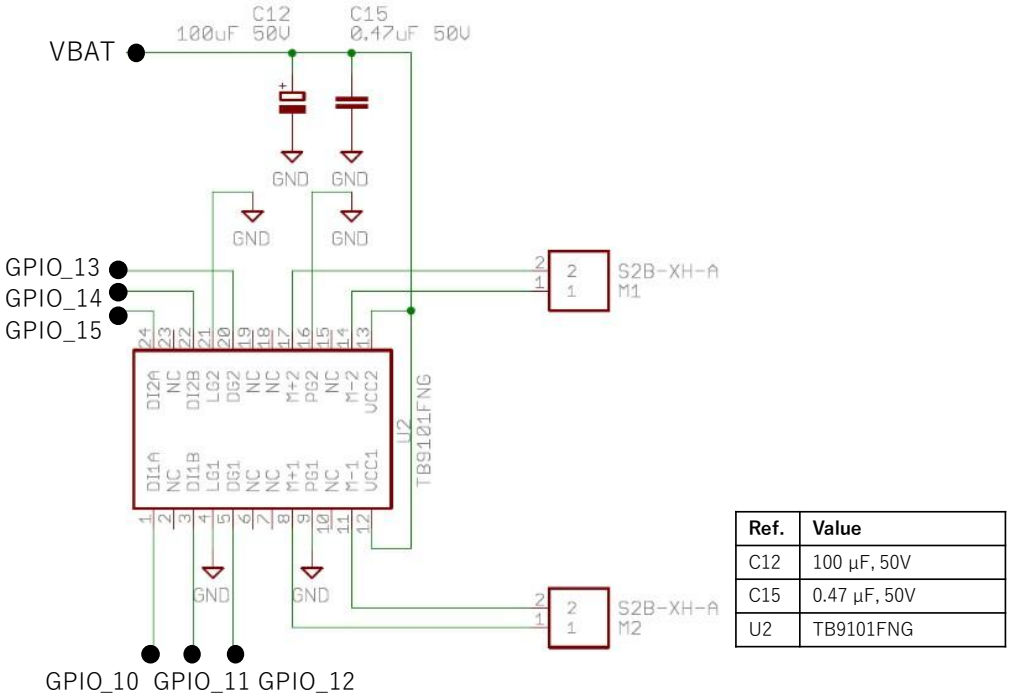
Ref.	Value
C8	3.3 µF
C9	2.2 µF
C11	3.3 µF
R5	4.7 kΩ
R9	4.7 kΩ

Fig 5.9 VCC and VDDIO Circuit for TB9054FTG

Power Supply Circuit for the Door Mirror Angle Adjustment Motor Control MCD (TB9101FNG)

This circuit, the automotive power supply VBAT is connected to VCC1/VCC2 of the TB9101FNG and functions as the primary power line for supplying power for motor drive. Capacitor C12 (100μF) is mainly used to absorb low-frequency fluctuations in the power supply and stabilize the voltage. Capacitor C15 (0.47μF) is a decoupling capacitor for removing high-frequency noise. By placing these two capacitors in parallel, noise and voltage fluctuations over a wide frequency range are suppressed, ensuring stable operation of downstream circuits and external loads.

In addition, this configuration accommodates rapid current fluctuations during motor operation and helps prevent voltage drops.

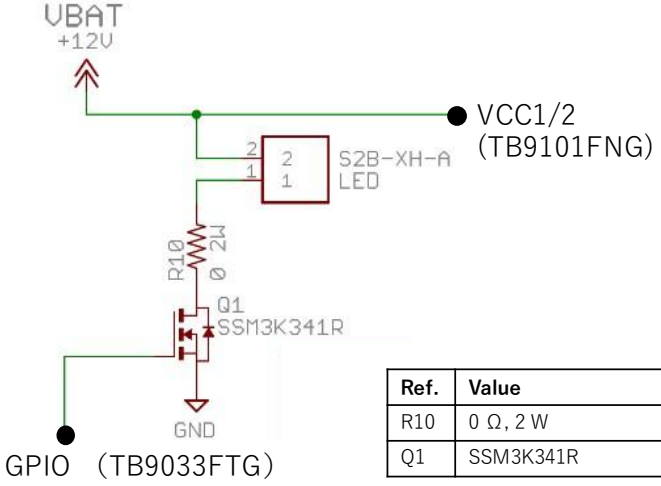


Ref.	Value
C12	100 μF, 50V
C15	0.47 μF, 50V
U2	TB9101FNG

Fig 5.10 VBAT Power Supply Circuit for TB9101FNG

Power Supply Circuit for Blinker Drive

This circuit operates based on the automotive power supply VBAT to provide power for the blinker drive. VBAT serves as the power source for blinker illumination.



Ref.	Value
R10	0 Ω, 2 W
Q1	SSM3K341R

Fig 5.11 Power Supply Circuit for Blinker Drive

5.3.2. CXPI BUS Signal Circuit

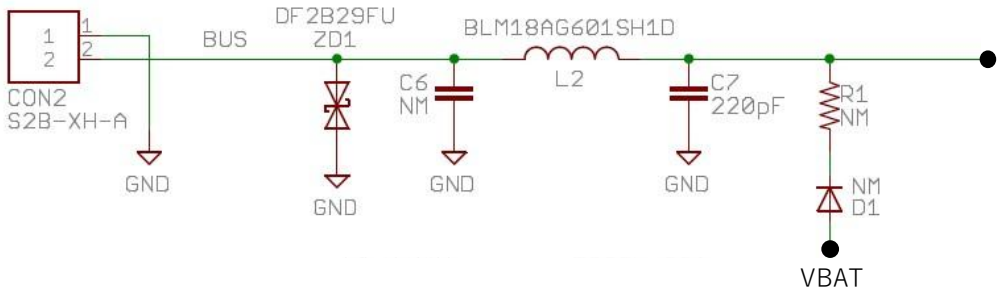
This circuit is a signal circuit for configuring the BUS line in accordance with the CXPI standard.

The design provides the fundamental functions required for CXPI communication and is intended to help ensure reliability in automotive environments.

Specifically, in addition to surge protection using an ESD protection diode, the circuit configuration combines a ferrite bead and capacitors to reduce the influence of high-frequency noise. Furthermore, C6 is provided as a spare pad that can be connected to GND, allowing adjustment flexible adjustment during EMC optimization.

It should be noted that the CXPI interface IC TB9033FTG (responder node) has an internal 30 kΩ pull-up resistor on the BUS pin. Therefore, in this configuration, the external components R1 and D1 are not mounted (NM: Not Mounted).

For other circuit configurations, the same design concept as the CXPI BUS signal circuit of the CXPI driver/receiver board is applied. For details, please refer to Section "4.3.2. CXPI BUS Signal Circuit."



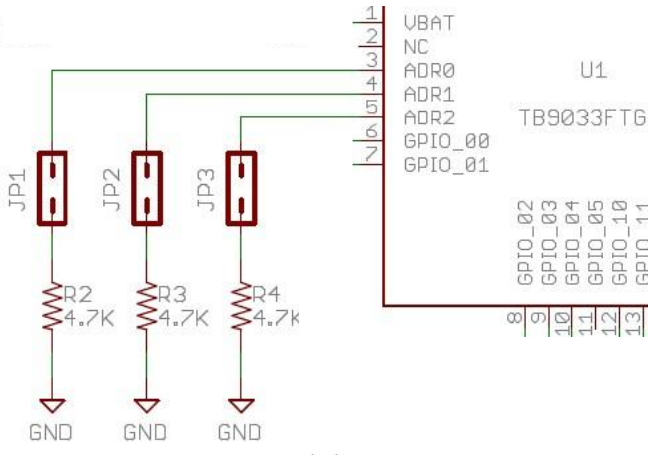
Ref.	Value
ZD1	DF2B29FU
C6	NM
L2	BLM18AG601SH1D
C7	220 pF
R1	NM
D1	NM

Fig 5.12 CXPI BUS Signal Circuit (Responder node)

5.3.3. TB9033FTG Node Address (NAD) Setting Circuit

This circuit, the initial NAD (Node Address) of the TB9033FTG is set during initial configuration via three pins (ADR0 to ADR2) using jumpers JP1 to JP3. The configuration method is as follows: Jumper shorted: connected to GND (ADRx = 0); Jumper open: pin open (ADRx = 1)

These pins are effective only when the NAD read from memory during the IC power-on sequence is 00h. Accordingly, the jumper-based setting is applied as the initial configuration at product shipment or when the NAD area in non-volatile memory is 00h. In addition, by using the Assign Node Address function, the NAD can be changed after communication has been established and written to memory, allowing operation independent of the jumper settings.



Ref.	Value
R2	4.7 kΩ
R3	4.7 kΩ
R4	4.7 kΩ

Fig 5.13 Initial Node Address (NAD) Setting Circuit

5.3.4. Motor Control Circuit for Door Mirror Folding (Open/Close Operation)

This control circuit is a brushed DC motor drive circuit for door mirror folding (open/close operation) centered on the motor driver IC TB9054FTG. The circuit is designed to reliably process control signals such as PWM input, mode control, and sleep control via the CXPI interface IC TB9033FTG. Signal line filtering and level stabilization using pull-up resistors are employed to ensure reliable operation in an automotive environment.

Motor Drive Mode Configuration

The motor driver IC TB9054FTG supports multiple drive modes.

This control circuit is designed based on the PWM-driven LARGE mode (2-channel combined mode, single motor). Accordingly, the related pins OSEL1/2 and ISEL1/2 are set to the Low level, and pull-down resistors R6 to R9 (4.7kΩ) are used to maintain the Low level.

Table 5.5 Motor Driver Signal Configuration of TB9054FTG

Pin	I/O	Description	Status	Circuit Configuration
PWM_CLK	I	Input from external MCU	Unused	Pulled down via R5 (4.7kΩ)
NCS	I	SPI input	Unused	OPEN
SDI	I	SPI input	Unused	OPEN
SDO	O	SPI output	Unused	OPEN
SCLK	I	SPI input	Unused	OPEN
OSEL1/2	I	Mode selection pins	L	Pulled down via R6, R9 (4.7kΩ)
ISEL1/2	I	Selection pins	L	Pulled down via R7, R8 (4.7kΩ)
PWM1	I	PWM input	H/L	PWM control from GPIO_30
PWM2	I	PWM input	H/L	PWM control from GPIO_31
PWM3	I	PWM input	Disabled	OPEN
PWM4	I	PWM input	Disabled	OPEN
CM1/2	O	Current monitor output	ADC	ADC input via GPIO_03, GPIO_04
DIAG1/2	O	DIAG output	Unused	
OUT1	O	Motor output 1	H/L	Output as 1 channel in LARGE mode
OUT2	O	Motor output 2	H/L	
OUT3	O	Motor output 3	H/L	Output as 1 channel in LARGE mode
OUT4	O	Motor output 4	H/L	
EN1/2	I	EN input	H/L	Controlled by GPIO_01
ENB1/2	I	ENB input	H/L	Controlled by GPIO_00
SLEEPB	I	Sleep input	H/L	Controlled by GPIO_02

Motor Drive Configuration

Control signals are input from the GPIO pins of the CXPI interface IC TB9033FTG to the motor driver IC TB9054FTG input pins PWM1/2, EN1/2, ENB1/2, and SLEEPB to control forward rotation, reverse rotation, and brake operation of the motor.

Table 5.6 shows the combinations of control signals. The duty cycle and frequency of the PWM signals applied to PWM1/2 can be configured in advance using the GPIO pin function settings. For EN1/2, ENB1/2, and SLEEPB, standard digital High/Low (H/L) levels are applied. Note that the functions shown in Table 5.6 represent only a subset of the available features. For detailed information, please refer to the product data sheet.

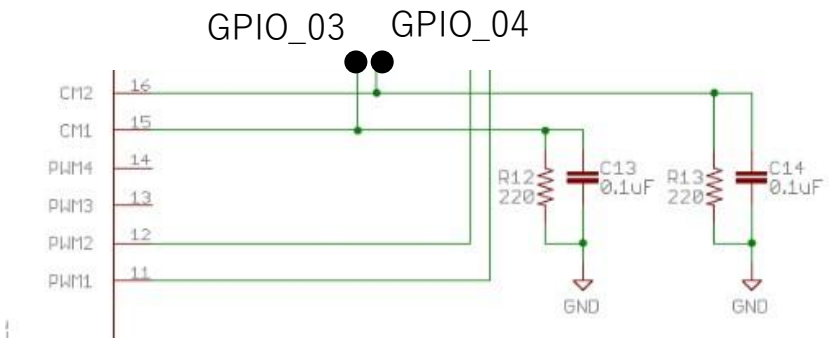
Table 5.6 Motor Function

Function	PWM1	PWM2	EN1/2	ENB1/2	SLEEPB	OUT1/2	OUT3/4
Forward	H	L	H	L	H	H	L
Short Brake	L	L	H	L	H	L	L
Reverse	L	H	H	L	H	L	H
Short Brake	H	H	H	L	H	H	H

Current Monitoring via CM1/CM2 Pins

The output pins CM1 and CM2 of the motor driver IC TB9054FTG allow real-time monitoring of the current (0 to 6A) flowing through the high-side switches (N-channel) of the H-bridge motor drive output. The current equivalent to 0.24% of the motor drive current is output from the CM pins. By connecting external resistors R12 and R13 (220Ω) between the CM1/CM2 pins and GND, this current can be detected as a voltage.

By capturing this voltage with the ADC inputs (GPIO_03/04) of the CXPI interface IC TB9033FTG, the motor status can be monitored, including conditions such as motor lock and load open detection during operation.



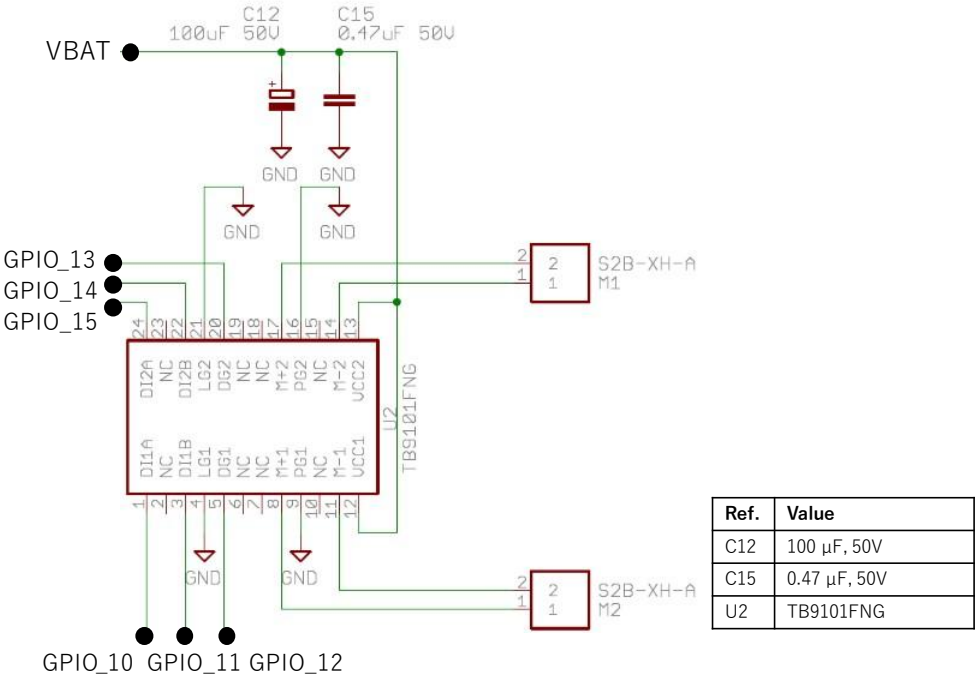
Ref.	Value
C13	0.1 µF
C14	0.1 µF
R12	220 Ω
R13	220 Ω

Fig 5.14 Current Monitoring Circuit

5.3.5. Door Mirror Angle Adjustment Motor Control Circuit

This control signal circuit is a drive circuit for a brushed DC motor used for mirror angle adjustment, configured around the motor driver IC TB9101FNG, as shown in Figure 5.14. As specified in Tables 5.7 and 5.8, the DI1A/DI2A and DI1B/DI2B pins of the TB9101FNG are connected to the GPIO pins of the CXPI interface IC TB9033FTG. Based on the signals output from the GPIOs, forward and reverse rotation of the motor corresponding to left/right and up/down mirror movement is controlled.

In addition, DG1/DG2 of the TB9101FNG are fault detection pins and are connected to GPIO_12 and GPIO_15 of the TB9033FTG. When a fault is detected, the status is reported by switching these pins to the Low level.



Ref.	Value
C12	100 µF, 50V
C15	0.47 µF, 50V
U2	TB9101FNG

Fig 5.15 Door Mirror Angle Adjustment Motor Control Circuit

Table 5.7 TB9101FNG Pin Configuration Table

Pin	I/O	Description	Status	Circuit configuration
DI1A/DI2A	IN	Motor 1/2 output control input pins	H/L	GPIO_10,13
DI1B/DI2B	IN		H/L	GPIO_11,14
LG1/2	IN	5V system GND pin	L	GND
DG1/2	OUT	Fault detection pins	H	Connected to GPIO_12, GPIO_15 (pull-up)
M+1/2	OUT	Motor 1/2 output pins	-	Mirror adjustment
M-1/2	OUT	Motor 1/2 output pins	-	Mirror adjustment
PG1/2	-	Motor output section GND	L	GND
NC	-	OPEN Pin	Unused	OPEN

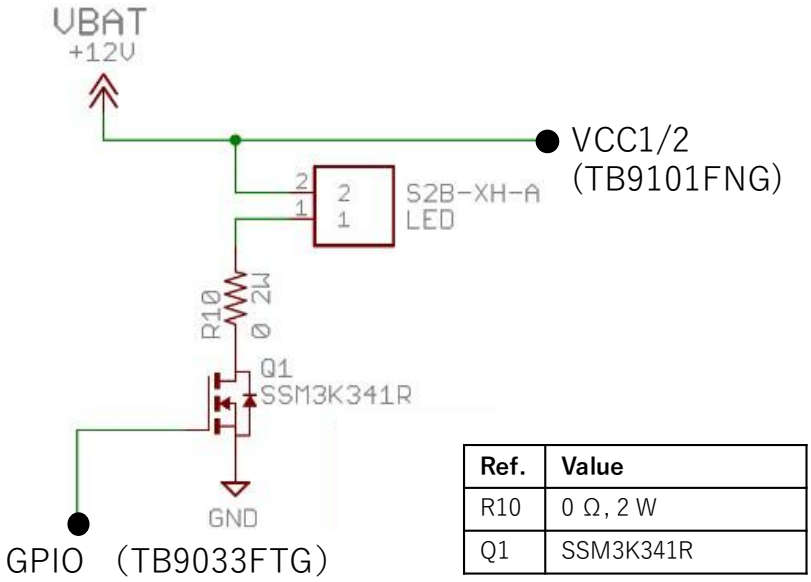
Table 5.8 TB9101FNG Motor Function

Function	DI1A/DI2A	DI1B/DI2B	M+1/2	M-1/2
Stop (Brake)	H	H	L	L
Forward	H	L	H	L
Reverse	L	H	L	H
Stop (Standby)	L	L	OFF (High Impedance)	

5.3.6. Blinker Drive Circuit

In this circuit, the blinker is driven using the automotive power supply VBAT. The N-channel MOSFET SSM3K341R is used as a switching device, and its gate is driven by a GPIO signal from the CXPI interface IC TB9033FTG, enabling LED ON/OFF control as well as PWM dimming.

The current-limiting resistor R10 limits the current flowing through the blinker and maintains the rated current. In this design, blinker with an internal current-limiting resistor is assumed; therefore, a zero-ohm resistor (0Ω / 2W) is used for R10. Depending on the specifications of the blinker to be driven, R10 should be replaced with an appropriate resistor value.



Ref.	Value
R10	0 Ω, 2 W
Q1	SSM3K341R

Fig 5.16 Blinker Drive Circuit

6. C LED Ambient Light Drive Board (Responder Node)

6.1. Specifications and Block Diagram

Table 6.1 shows the main specifications of the RD254C board used in this design.

Table 6.1 RD254C Board Specifications

Item	Condition	Min.	Typ.	Max.	Unit
Power					
VBAT Voltage		6	12	16	V
VCC Output Voltage		4.8	5	5.2	V
BUS (DC characteristics)					
Dominant Voltage at Reception	Voltage at which the receiving node determines Low level	-	-	0.423 x VBAT	V
Recessive Voltage at Reception	Voltage at which the receiving node determines High level	0.556 x VBAT	-	-	V
Hysteresis		-	-	0.133 x VBAT	V
GPIO_xx: Digital Output (PWM)					
Output HIGH Voltage	Load current -2mA, VCC = 5V	4	-	-	V
Output LOW Voltage	Load current 2 mA, VCC = 5V	-	-	1	V
LED ambient light driver					
LED Supply Voltage		-	12	24	V
LED Drive Current		-	-	3	A
Other settings					
Board Layer Structure	FR-4, 2 layers (through-hole via), PCB thickness 1.6mm, Cu thickness 35µm (surface layer)				
Board Size	100mm x 100mm				

Fig 6.1 shows the block diagram of the RD254C board used in this design.

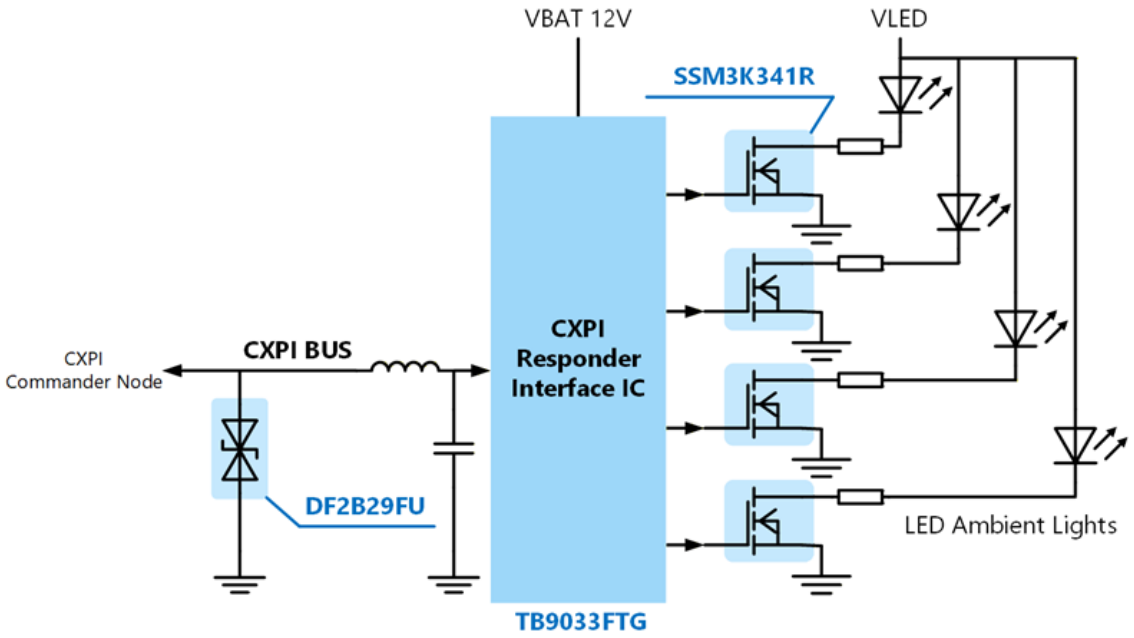


Fig 6.1 RD254C Block Diagram

Table 6.2 RD254C Board Control Signal Connection Specifications

GPIO (TB9033FTG)	Description	Connection
GPIO_16	PWM	CON7
GPIO_17	PWM	CON6
GPIO_30	PWM	CON5
GPIO_31	PWM	CON4

6.2. Main Components Used

This section describes the main components used on the RD254C board in this design.

6.2.1. CXPI Interface IC TB9033FTG

In this design, the automotive CXPI responder interface IC TB9033FTG, which incorporates hardware logic, is used in the bus circuit on the responder side.

The TB9033FTG provides 16-channel GPIO pins, of which 6 channels can be configured as A/D converter inputs and 4 channels can be configured as PWM outputs.

For details of this device, please refer to the previous section, *"5.2.1.* CXPI Interface IC TB9033FTG"

6.2.2. N-Channel MOSFET SSM3K341R

In this design, the N-channel MOSFET SSM3K341R is used for LED ambient light control.

For details of this device, please refer to the previous section, *"5.2.4.* N-Channel MOSFET SSM3K341R"

6.2.3. TVS Diode DF2B29FU

In this design, the bidirectional ESD protection diode DF2B29FU is used to protect the CXPI BUS circuit against electrostatic discharge (ESD).

For details of this device, please refer to the previous section, *"5.2.5.* TVS Diode DF2B29FU".

6.3. Circuit Design

This section describes the key points of the circuit design for each part of the RD254C board used in this design.

6.3.1. Power Supply Circuit

The design of the connector section, EMC-compliant filtering circuit, and indicator circuit is identical to that of the power supply circuit for the CXPI driver/receiver board.

For details, please refer to Section *"4.3.1. Power Supply Circuit"*.

6.3.2. CXPI BUS Signal Circuit

This circuit is a signal circuit for configuring the BUS line in accordance with the CXPI standard.

The design provides the fundamental functions required for CXPI communication and is intended to help ensure reliability in automotive environments.

Specifically, in addition to surge protection using an ESD protection diode, the circuit configuration combines a ferrite bead and capacitors to reduce the influence of high-frequency noise. Furthermore, C6 is provided as a spare pad that can be connected to GND, allowing adjustment flexible adjustment during EMC optimization.

It should be noted that the CXPI interface IC TB9033FTG has an internal 30kΩ pull-up resistor on the BUS pin. Therefore, in this configuration, the external components R1 and D1 are not mounted (NM: Not Mounted).

For other circuit configurations, the same design concept as the CXPI BUS signal circuit of the CXPI Door Mirror Drive board is applied. For details, please refer to Section "*5.3.2. CXPI BUS Signal Circuit.*"

6.3.3. TB9033FTG Node Address (NAD) Setting Circuit

This circuit sets the initial NAD (Node Address) of the TB9033FTG via three pins (ADR0 to ADR2) using jumpers JP1 to JP3 during initial configuration.

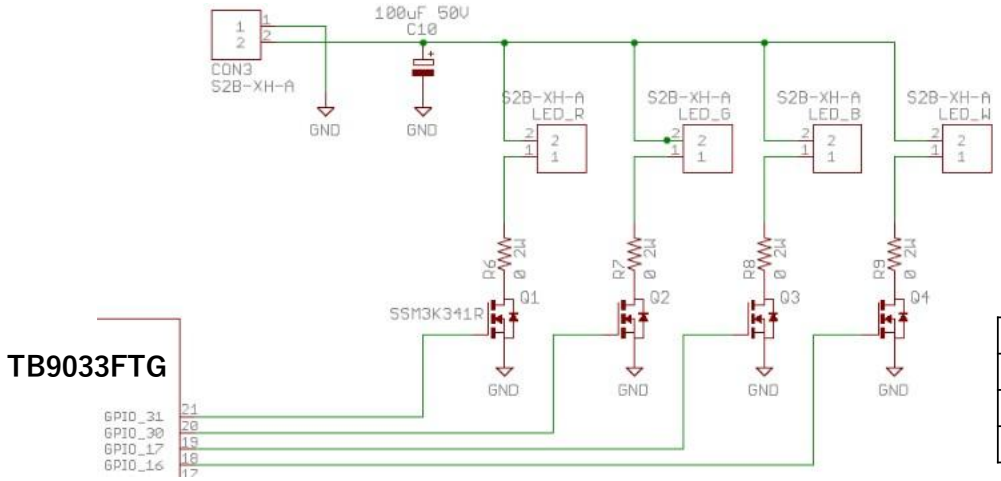
For details, please refer to the previous section, *"5.3.3. TB9033FTG Node Address (NAD) Setting Circuit"*.

6.3.4. LED Ambient Light Drive Circuit

This circuit is designed to drive the LED ambient light using the automotive power supply VBAT.

A MOSFET-based switching method is adopted for lighting control to ensure reliability and safety in an automotive environment. The N-channel MOSFET SSM3K341R is used as the switching device, and its gate is driven by GPIO signals from the CXPI interface IC TB9033FTG, enabling LED ON/OFF control as well as PWM dimming.

The current-limiting resistors R6~R9 limit the current flowing through the LED ambient light and maintain the rated current. In this design, LED ambient lights with internal current-limiting resistors are assumed; therefore, zero-ohm resistors (0Ω / 2W) are used. Depending on the specifications of the LED ambient light to be driven, these resistors should be replaced with appropriate values.



Ref.	Value
R6,7,8,9	0 Ω, 2 W
Q1,2,3,4	SSM3K341R
C10	100 µF, 50 V

Fig 6.2 LED Ambient Light Drive Circuit

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