

DCL34xx0B

DCL340L0B/DCL340H0B/DCL341L0B/DCL341H0B/DCL342L0B/DCL342H0B

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL340L0B/DCL340H0B/DCL341L0B/DCL341H0B/DCL342L0B/DCL342H0B are low power quad-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 3000V_{rms} rating as a withstand isolation voltage. These products can operate with a temperature range of -40 to 125 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 25 Mbps
Supply voltage	: 2.25 V to 5.5 V
Temperature Range	: -40 °C to 125 °C
Propagation Delay	: 33 ns Typ. (5.0 V operation)
Default Output	: High and Low Options
High CMTI(min.)	: ±30 kV/μs
Withstand Isolation Voltage	: 3 kV _{rms}
Package	: 16pin SSOP (16LD QSOP)
Safety-Related Certification	: UL1577, CQC, VDE DIN EN 60747-17
UL	: UL1577, File No. E519997
cUL	: CSA Component Acceptance Service Notice No. 5A
VDE	: DIN EN IEC 60747-17 (VDE 0884-17) (Planning)
CQC	: GB 4943.1-2022 (Planning)

Start of commercial production

2026-04

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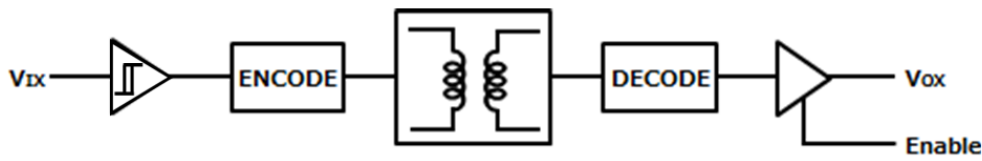
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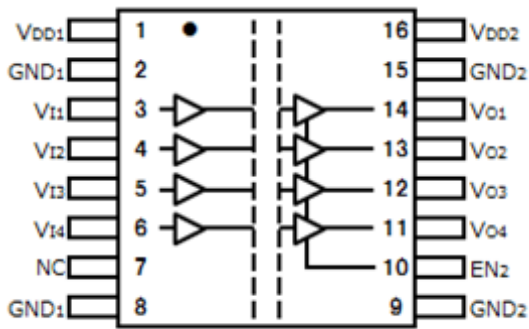
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4. Internal Circuit

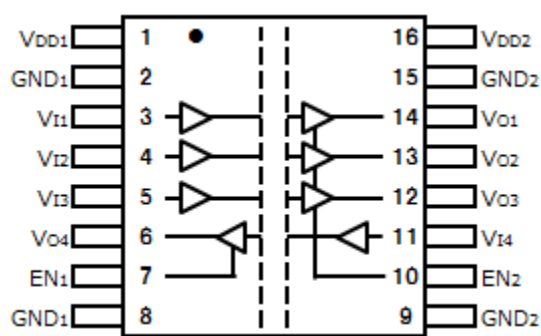


5. Pin configuration and Functions

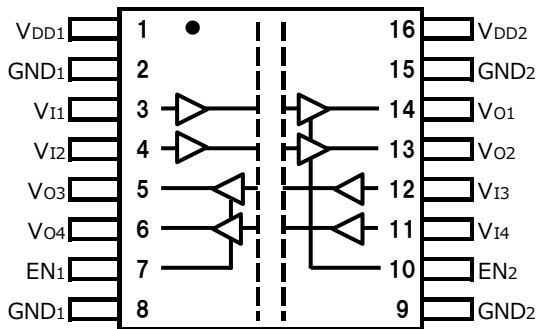
DCL340L0B / DCL340L0B



DCL341L0B / DCL341H0B



DCL342L0B / DCL342H0B



5.1. Pin Functions

NAME	PIN			I/O	DESCRIPTION
	DCL340L0B DCL340H0B	DCL341L0B DCL341H0B	DCL342L0B DCL342H0B		
V _{DD1}	1	1	1	-	Power Supply, side 1
GND ₁	2,8	2,8	2,8	-	GND connection for V _{DD1} , side 1
V _{I1}	3	3	3	I	Input, Channel1
V _{I2}	4	4	4	I	Input, Channel2
V _{I3}	5	5	12	I	Input, Channel3
V _{I4}	6	11	11	I	Input, Channel4
EN ₁	-	7	7	I	Output enable 1. Input pins on side 1 are enabled when EN ₁ is high, and in high impedance state when EN ₁ is low.
GND ₂	9,15	9,15	9,15	-	GND connection for V _{DD2} , side 2
EN ₂	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN ₂ is high, and in high impedance state when EN ₂ is low.
V _{O4}	11	6	6	O	Output, Channel4
V _{O3}	12	12	5	O	Output, Channel3
V _{O2}	13	13	13	O	Output, Channel2
V _{O1}	14	14	14	O	Output, Channel1
V _{DD2}	16	16	16	-	Power Supply, side 2
NC	7	-	-	-	Please use NC pin by open.

6. Functional Description

DCL340L0B/DCL340H0B / DCL341L0B/DCL341H0B / DCL342L0B/DCL342H0B

V _{DDI}	V _{DDO}	OUTPUT ENABLE (EN _x)	INPUT (V _{IX})	OUTPUT (V _{OX})	DESCRIPTION
PU	PU	H	L	L	Normal Operation
			H	H	
		L	L or H	Z	Output Disable mode
PU	PD	X	L or H	Undetermined	When V _{DDO} is unpowered, a channel output is undetermined.
PD	PU	H	X	Default	Default mode DCL34xL0B=L , DCL34xH0B=H
		L		Z	Output Disable mode
PD	PD	X	X	Undetermined	When V _{DDO} is unpowered, a channel output is undetermined.

PU= Powered up ($V_{DD} \geq 2.25\text{ V}$), PD= Powered down ($V_{DD} < 2.25\text{ V} \rightarrow 0\text{ V}$), H = High level, L = Low level, X = Don't Care

V_{DDI}, V_{DDO} : Supply voltages on the input and output sides of each channel.

EN_x : Output enable signal on the same side as the V_{OX} output.

V_{IX}, V_{OX} : Input and output signals of each channel.

When the input pin (V_{IX}) on the power-off side is set to "H", power is supplied to the device via the ESD circuit, so use is prohibited.

Don't leave the Input pin (V_{IX}) and Enable pin (EN_x) on the power ON side open because terminal circuits don't have pull-down resistor or pull-down resistor inside.

7. Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V _{DD1} , V _{DD2}	-0.5	6.0	V
Input Voltage	V _I	-0.5	V _{DDX} +0.5 ^(Note1)	V
Output Voltage	V _O	-0.5	V _{DDX} +0.5 ^(Note1)	V
Output Current	I _O	-15	15	mA
Storage Temperature	T _{stg}	-65	150	°C
Operating Temperature	T _{opr}	-40	125	°C
Soldering Temperature (10 s)	T _{sol}	-	260	°C
Maximum Withstanding Isolation Voltage (1 min.)	BV _S	-	3000	V _{rms}

Note1: Maximum voltage must not exceed 6 V. X = 1 or 2.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V _{DD1} , V _{DD2}	2.25	5.5	V
Junction Temperature	T _J	-40	150	°C
Operating Temperature	T _{opr}	-40	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 µF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND₁) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND₂) for V_{DD2} and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at $T_a = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_a \leq 125^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V _{IX} = H , I _{OH} = -20 μA	-	V _{OH}	V _{DDO} ^(Note1) -0.1	V _{DDO} ^(Note1)	-	V
	V _{IX} = H , I _{OH} = -4 mA			V _{DDO} ^(Note1) -0.4	V _{DDO} ^(Note1) -0.2	-	
Output Voltage Logic Low	V _{IX} = L , I _{OL} = 20 μA	-	V _{OL}	-	0.0	0.1	V
	V _{IX} = L , I _{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z _O	-	50	-	Ω
High-level input voltage	-	-	V _{IH}	0.7*V _{DDI} ^(Note1)	-	-	V
Low-level input voltage	-	-	V _{IL}	-	-	0.3*V _{DDI} ^(Note1)	V
Input Voltage Hysteresis	-	-	V _{HYS}	-	0.44	-	V
Input Current	V _I = V _{DDI} ^(Note1) or 0 V	-	I _I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t _{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 % , t _r = t _f = 2 ns, C _L = 15 pF	Fig. 12-1	t _{PHL} , t _{PLH}	-	33	46	ns
DC~10Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.7	8.0	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	16	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	5.0	ns
	Opposing Direction	-	t _{skOD}	-	-	7.0	
DC~25Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.7	13	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	21	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	10	ns
	Opposing Direction	-	t _{skOD}	-	-	12	
Output Rise Time	10 % - 90 %	Fig. 12-1	t _r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t _f	-	2.0	-	ns
Enable 3-state output enable time ^(Note3)	50 kHz, Duty = 50 % , t _r = t _f = 2 ns, C _L = 15 pF	Fig. 12-2	t _{PZL} , t _{PZH}	-	-	10	ns
Enable 3-state output disable time		Fig. 12-2	t _{PLZ} , t _{PHZ}	-	-	15	ns
Default output delay time from input power loss	V _{DDI} < 2.25 V → 0 V		t _{DO}	-	-	25	μs
Time from PU ⁽⁴⁾ to valid output data			t _{PU}	-	-	30	μs
Common mode transient immunity	V _I = V _{DDI} or 0 V , V _{CM} = 400 V ,T _a = 25°C	Fig. 12-3	CMTI	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up ($V_{DD} \geq 2.25\text{ V}$), After VDD is set powered up, normal operation become valid 30 μs later.

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at $T_a = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_a \leq 125^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V _{IX} = H , I _{OH} = -20 μA	-	V _{OH}	V _{DDO} ^(Note1) -0.1	V _{DDO} ^(Note1)	-	V
	V _{IX} = H , I _{OH} = -4 mA			V _{DDO} ^(Note1) -0.4	V _{DDO} ^(Note1) -0.2	-	
Output Voltage Logic Low	V _{IX} = L , I _{OL} = 20 μA	-	V _{OL}	-	0.0	0.1	V
	V _{IX} = L , I _{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z _O	-	50	-	Ω
High-level input voltage	-	-	V _{IH}	0.7*V _{DDI} ^(Note1)	-	-	V
Low-level input voltage	-	-	V _{IL}	-	-	0.3*V _{DDI} ^(Note1)	V
Input Voltage Hysteresis	-	-	V _{HYS}	-	0.25	-	V
Input Current	V _I = V _{DDI} ^(Note1) or 0 V	-	I _I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t _{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 % , t _r = t _f = 2 ns, C _L = 15 pF	Fig. 12-1	t _{PHL} , t _{PLH}	-	38	52	ns
DC~10Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.7	8.0	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	19	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	5.0	ns
	Opposing Direction	-	t _{skOD}	-	-	9.0	
DC~25Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.7	13	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	24	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	10	ns
	Opposing Direction	-	t _{skOD}	-	-	14	
Output Rise Time	10 % - 90 %	Fig. 12-1	t _r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t _f	-	2.0	-	ns
Enable 3-state output enable time ^(Note3)	50 kHz, Duty = 50 % , t _r = t _f = 2 ns, C _L = 15 pF	Fig. 12-2	t _{PZL} , t _{PZH}	-	-	15	ns
Enable 3-state output disable time		Fig. 12-2	t _{pLZ} , t _{pHZ}	-	-	20	ns
Default output delay time from input power loss	V _{DDI} < 2.25 V → 0 V		t _{DO}	-	-	30	μs
Time from PU ^(Note4) to valid output data			t _{PU}	-	-	30	μs
Common mode transient immunity	V _I = V _{DDI} or 0 V , V _{CM} = 400 V, T _a = 25°C	Fig. 12-3	CMTI	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up ($V_{DD} \geq 2.25\text{ V}$), After VDD is set powered up, normal operation become valid 30 μs later.

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = 2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, and $-40\text{ }^{\circ}\text{C} \leq T_a \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Output Voltage Logic High	V _{IX} = H , I _{OH} = -20 μA	-	V _{OH}	V _{DDO} ^(Note1) -0.1	V _{DDO} ^(Note1)	-	V
	V _{IX} = H , I _{OH} = -4 mA			V _{DDO} ^(Note1) -0.4	V _{DDO} ^(Note1) -0.2	-	
Output Voltage Logic Low	V _{IX} = L , I _{OL} = 20 μA	-	V _{OL}	-	0.0	0.1	V
	V _{IX} = L , I _{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	-	Z _O	-	50	-	Ω
High-level input voltage	-	-	V _{IH}	0.7*V _{DDI} ^(Note1)	-	-	V
Low-level input voltage	-	-	V _{IL}	-	-	0.3*V _{DDI} ^(Note1)	V
Input Voltage Hysteresis	-	-	V _{HYS}	-	0.22	-	V
Input Current	V _I = V _{DDI} ^(Note1) or 0 V	-	I _I	-	-	±1	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t _{bps}	DC	-	25	Mbps
Pulse Width	-	-	PW	40	-	-	ns
Propagation Delay	50 kHz, Duty = 50 % , t _r =t _f = 2 ns, C _L = 15 pF	Fig. 12-1	t _{PHL} , t _{PLH}	-	45	63	ns
DC~10Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.1	8.0	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	24	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	7.0	ns
	Opposing Direction	-	t _{skOD}	-	-	11	
DC~25Mbps							
Pulse Width Distortion	t _{PHL} – t _{PLH}	Fig. 12-1	PWD	-	0.1	13	ns
Propagation Delay Skew ^(Note2) (Between any two units)	-	-	t _{PSK}	-	-	29	ns
Channel Matching	Same Direction	-	t _{skCD}	-	-	12	ns
	Opposing Direction	-	t _{skOD}	-	-	16	
Output Rise Time	10 % - 90 %	Fig. 12-1	t _r	-	2.0	-	ns
Output Fall Time	90 % - 10 %	Fig. 12-1	t _f	-	2.0	-	ns
Enable 3-state output enable time ^(Note3)	50 kHz, Duty = 50 % , t _r = t _f = 2 ns, C _L = 15 pF	Fig. 12-2	t _{pZL} , t _{pZH}	-	-	20	ns
Enable 3-state output disable time		Fig. 12-2	t _{pLZ} , t _{pHZ}	-	-	25	ns
Default output delay time from input power loss	V _{DDI} < 2.25 V → 0 V		t _{DO}	-	-	40	μs
Time from PU ^(Note4) to valid output data			t _{PU}	-	-	30	μs
Common mode transient immunity	V _I = V _{DDI} or 0 V , V _{CM} = 400 V , T _a = 25 °C	Fig. 12-3	CMTI	30	-	-	kV/μs

Note1: V_{DDI} = Input-side V_{DDX} , V_{DDO} = Output-side V_{DDX}

Note2: Propagation delay difference (between parts) is applied under the same operating conditions (power supply voltage, input current, temperature conditions, etc.).

Note3: When ENx signal is changed from Low to High, the output signal (V_{OX}) is valid after the output enable time. The output signal (V_{OX}) within the output enable time is undefined.

Note4: PU = Powered up ($V_{DD} \geq 2.25\text{ V}$), After VDD is set powered up, normal operation become valid 30 μs later.

9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-40\text{ }^{\circ}\text{C} \leq T_a \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted.

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	280	530	μA
		$I_{DD2(Q)}$	-	370	1110	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	415	630	μA
		$I_{DD2(1)}$	-	520	1280	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	420	630	μA
		$I_{DD2(1)}$	-	680	1440	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	9.3	13.2	mA
		$I_{DD2(25)}$	-	8.1	10.6	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	305	645	μA
		$I_{DD2(Q)}$	-	340	940	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	440	790	μA
		$I_{DD2(1)}$	-	495	1105	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	490	845	μA
		$I_{DD2(1)}$	-	625	1240	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	9.1	12.7	mA
		$I_{DD2(25)}$	-	8.8	11.4	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	I _{DD1(Q)}	-	330	795	μA
		I _{DD2(Q)}	-	310	780	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	I _{DD1(1)}	-	465	935	μA
		I _{DD2(1)}	-	465	935	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(1)}	-	560	1030	μA
		I _{DD2(1)}	-	560	1030	μA
25 Mbps	f _{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(25)}	-	9.0	12.1	mA
		I _{DD2(25)}	-	9.0	12.1	mA

9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40\text{ }^{\circ}\text{C} \leq T_a \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted.

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	210	395	μA
		$I_{DD2(Q)}$	-	290	890	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	295	460	μA
		$I_{DD2(1)}$	-	385	995	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	300	460	μA
		$I_{DD2(1)}$	-	495	1130	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	6.7	10.5	mA
		$I_{DD2(25)}$	-	5.4	7.3	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	235	505	μA
		$I_{DD2(Q)}$	-	260	745	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	320	580	μA
		$I_{DD2(1)}$	-	360	845	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	350	620	μA
		$I_{DD2(1)}$	-	445	950	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	6.5	9.6	mA
		$I_{DD2(25)}$	-	5.8	7.8	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	I _{DD1(Q)}	-	250	620	μA
		I _{DD2(Q)}	-	240	610	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	I _{DD1(1)}	-	340	710	μA
		I _{DD2(1)}	-	340	710	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(1)}	-	395	780	μA
		I _{DD2(1)}	-	395	780	μA
25 Mbps	f _{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(25)}	-	6.1	8.6	mA
		I _{DD2(25)}	-	6.1	8.6	mA

9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD1} = V_{DD2} = 2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, and $-40\text{ }^{\circ}\text{C} \leq T_a \leq 125\text{ }^{\circ}\text{C}$, unless otherwise noted

(1) DCL340x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	190	355	μA
		$I_{DD2(Q)}$	-	260	825	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	270	405	μA
		$I_{DD2(1)}$	-	330	905	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	270	405	μA
		$I_{DD2(1)}$	-	415	1010	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	6.4	9.7	mA
		$I_{DD2(25)}$	-	4.3	6.3	mA

(2) DCL341x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	$I_{DD1(Q)}$	-	210	455	μA
		$I_{DD2(Q)}$	-	240	690	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. No load	$I_{DD1(1)}$	-	280	520	μA
		$I_{DD2(1)}$	-	310	765	μA
1 Mbps	$f_{CLK} = 500\text{ kHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(1)}$	-	305	545	μA
		$I_{DD2(1)}$	-	375	845	μA
25 Mbps	$f_{CLK} = 12.5\text{ MHz}$, duty = 50 % cycle square wave. $C_L = 15\text{ pF}$	$I_{DD1(25)}$	-	5.7	8.4	mA
		$I_{DD2(25)}$	-	4.6	6.3	mA

(3) DCL342x0B

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	EN1,EN2 = High Enable VI = 0 or 1	I _{DD1(Q)}	-	230	570	μA
		I _{DD2(Q)}	-	220	570	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. No load	I _{DD1(1)}	-	290	635	μA
		I _{DD2(1)}	-	290	635	μA
1 Mbps	f _{CLK} = 500 kHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(1)}	-	335	690	μA
		I _{DD2(1)}	-	335	690	μA
25 Mbps	f _{CLK} = 12.5 MHz, duty = 50 % cycle square wave. C _L = 15 pF	I _{DD1(25)}	-	5.2	7.3	mA
		I _{DD2(25)}	-	5.2	7.3	mA

10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clearance	CLR	Shortest terminal-to-terminal distance through air	3.4	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	3.4	mm
Distance Through The Insulation	DTI	Minimum internal gap	8.5	μm
Comparative Tracking Index	CTI		400	V
Material Group	-	According to IEC 60664-1	II	-
Overtoltage Category Per IEC 60664-1	-	Rated main voltage ≤ 300 V _{RMS}	I-III	-
DIN EN IEC 60747-17; (VDE 0884-17)				
Maximum Repetitive Peak Isolation Voltage	V _{IORM}	AC voltage (bipolar)	566	V _{PK}
Maximum Transient Isolation Voltage	V _{IOTM}	V _{TEST} = V _{IOTM} , t = 60 s (qualification) , V _{TEST} = 1.2 x V _{IOTM} , t = 1 s (100 % production)	4243	V _{PK}
Maximum Impulse Voltage	V _{IMP}	IEC 62368-1 1.2/50 μs waveform	4000	V _{PK}
Maximum surge isolation voltage	V _{IOSM}	Test method per IEC 61000-4-5, 1.2/50 μs waveform, V _{IOSM} ≥ 1.3 × V _{IMP} (qualification)	5200	V _{PK}
Apparent charge measuring voltage	V _{pd(m)}	Method A, After Input/Output safety test subgroup2&3, V _{ini,a} = V _{IOTM} , V _{pd(m)} = 1.2 x V _{IORM} t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	680	V _{PK}
		Method A, After environmental tests subgroup 1, V _{ini,a} = V _{IOTM} , V _{pd(m)} = 1.3 x V _{IORM} t _{ini} = 60 s, t _m = 10 s, partial discharge < 5 pC	736	
		Method B1; At routine test (100 % production) and preconditioning (type test) V _{ini,b} ≥ 1.2 x V _{IOTM} , V _{pd(m)} = 1.5 x V _{IORM} t _{ini,b} = 1 s, t _m = 1 s partial discharge < 5 pC	849	
Barrier capacitance, input to output	C _{IO}	f = 1 MHz	1.7	pF
DCL340x0B				
Input Capacitance	C _I	input : V _{I1} ~V _{I3}	1.8	pF
		input : V _{I4}	2.3	pF
DCL341x0B				
Input Capacitance	C _I	input : V _{I1} ~V _{I3}	1.8	pF
		input : V _{I4}	4.2	pF
DCL342x0B				
Input Capacitance	C _I	input : V _{I1} ,V _{I2}	1.8	pF
		input : V _{I3}	3.6	pF
		input : V _{I4}	4.2	pF
Isolation Resistance	R _{IO}	V _{IO} = 500 V, T _A = 25 °C	>10 ¹²	Ω
		V _{IO} = 500 V, 100 °C ≤ T _A ≤ 125 °C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150 °C	>10 ⁹	
Pollution Degree	-	-	2	-
Climatic Category	-	-	40/125/21	-
UL 1577				
Maximum Withstand Isolation Voltage	V _{ISO}	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100 % production)	3000	V _{rms}

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output or Supply Current	I_S	$V_{DD1} = V_{DD2} = 5.5\text{ V}$, $T_j = 150\text{ }^{\circ}\text{C}$, $T_a = 25\text{ }^{\circ}\text{C}$	287	mA
		$V_{DD1} = V_{DD2} = 3.6\text{ V}$, $T_j = 150\text{ }^{\circ}\text{C}$, $T_a = 25\text{ }^{\circ}\text{C}$	439	mA
		$V_{DD1} = V_{DD2} = 2.75\text{ V}$, $T_j = 150\text{ }^{\circ}\text{C}$, $T_a = 25\text{ }^{\circ}\text{C}$	575	mA
Safety Input, Output or Total Power	P_S	$T_j = 150^{\circ}\text{C}$, $T_a = 25^{\circ}\text{C}$	1580	W
Maximum Safety Temperature	T_S	-	150	$^{\circ}\text{C}$

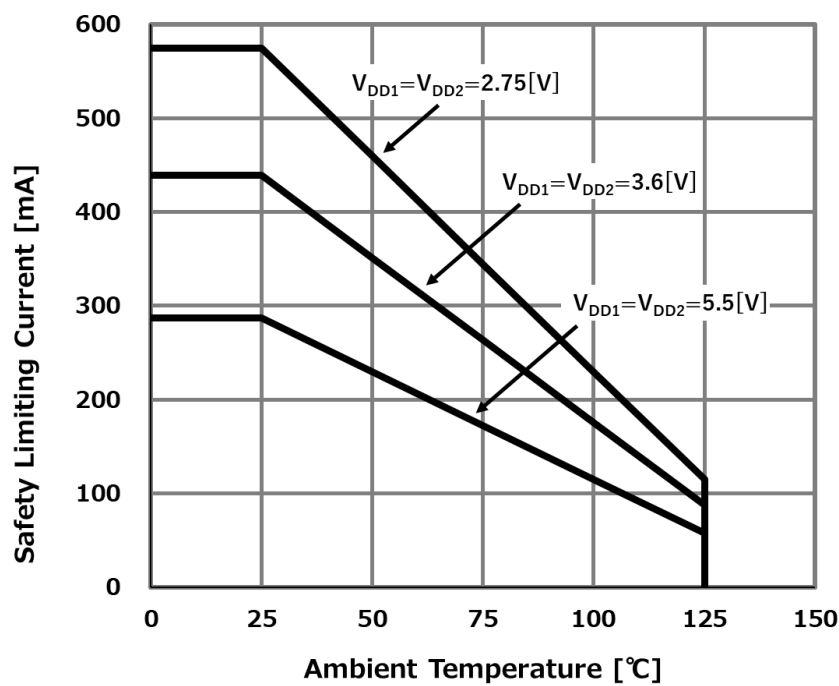


Fig. 11.1 Thermal Derating Curve for Safety Limiting Current-Ta

12. Test Circuit

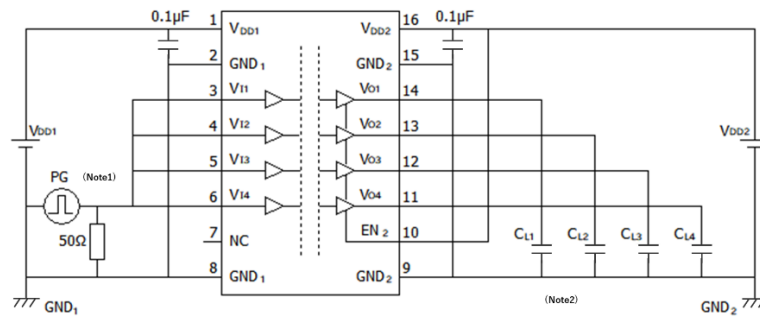


Fig. 12-1-1: DCL340L0B/DCL340H0B Switching Test Circuit

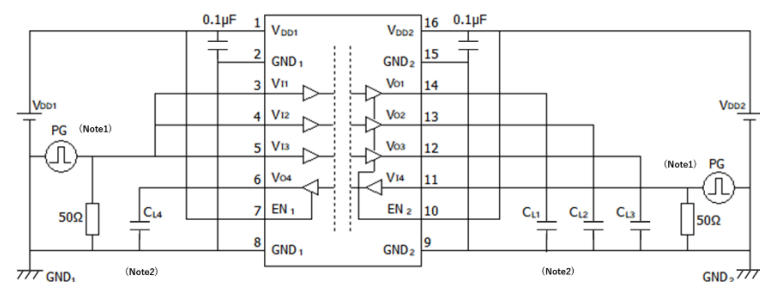


Fig. 12-1-2: DCL341L0B/DCL341H0B Switching Test Circuit

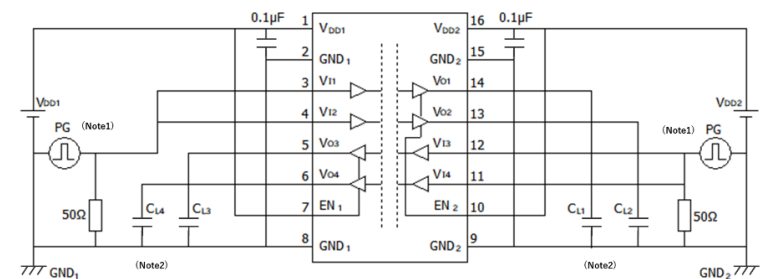


Fig. 12-1-3: DCL342L0B/DCL342H0B Switching Test Circuit

Note1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50 \text{ kHz}$, 50 % duty cycle, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$, $Z_0 = 50 \text{ }\Omega$. At the input, $50 \text{ }\Omega$ resistor is required to terminate input generator signal. It is needed not in actual application.

Note2: $C_{IX} = 15 \text{ pF}$ includes instrumentation and fixture capacitance.

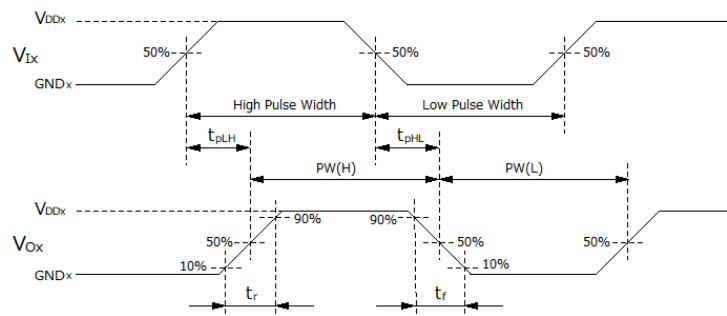


Fig. 12-1-4: DCL34xx0B Switching Waveforms

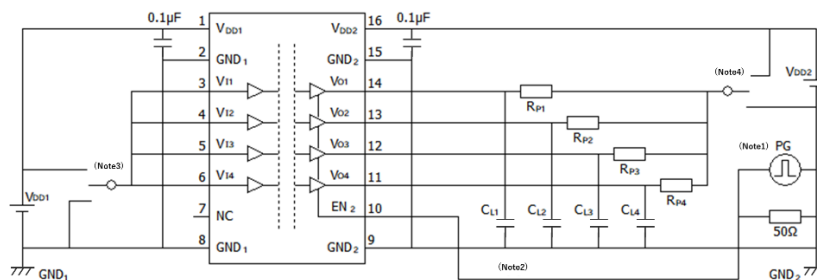


Fig. 12-2-1: DCL340L0B/DCL340H0B Enable Propagation Delay Time Test Circuit

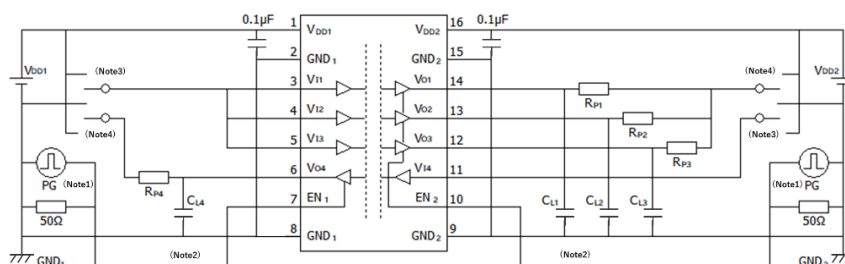


Fig. 12-2-2: DCL341L0B/DCL341H0B Enable Propagation Delay Time Test Circuit

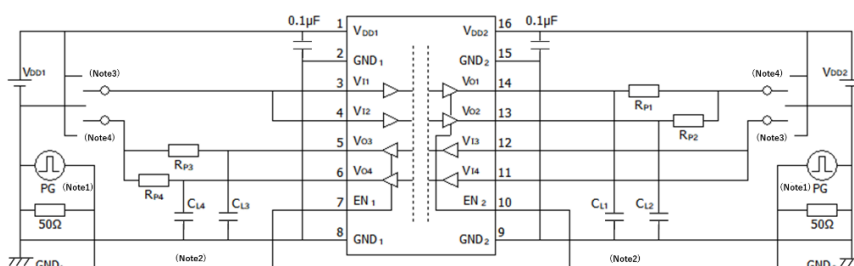


Fig. 12-2-3: DCL342L0B/DCL342H0B Enable Propagation Delay Time Test Circuit

Note1: The input pulse is supplied by a generator having the following characteristics: $PRR \leq 50 \text{ kHz}$, 50 % duty cycle, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$, $Z_0 = 50 \Omega$. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

Note2: $C_{LX} = 15 \text{ pF}$ includes instrumentation and fixture capacitance.

Note3: GND for t_{pZL} , t_{pLZ} , V_{DD} for t_{pZH} , t_{pHZ}

Note4: V_{DD} for t_{pZL} , t_{pLZ} , GND for t_{pZH} , t_{pHZ} .

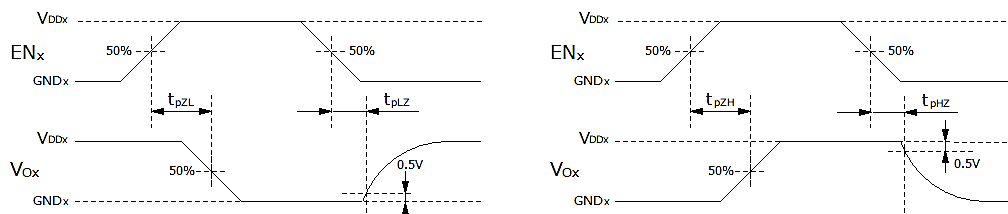


Fig. 12-2-4: DCL34xL0B/DCL34xH0B Enable Propagation Delay Time Waveforms

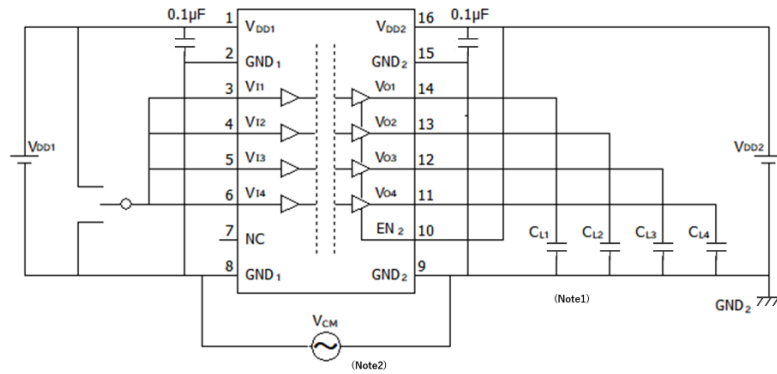


Fig. 12-3-1: DCL340L0B/DCL340H0B Common-Mode Transient Immunity Test Circuit

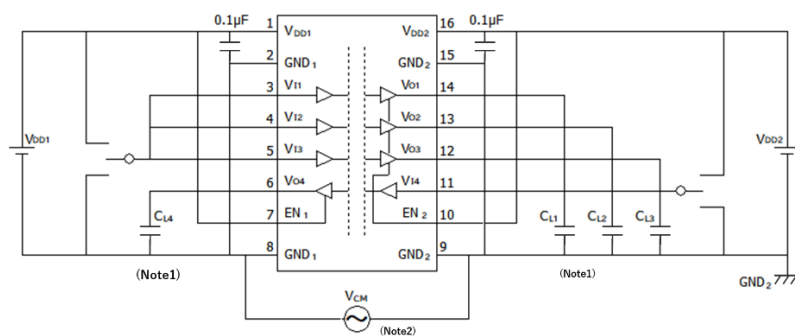


Fig. 12-3-2: DCL341L0B/DCL341H0B Common-Mode Transient Immunity Test Circuit

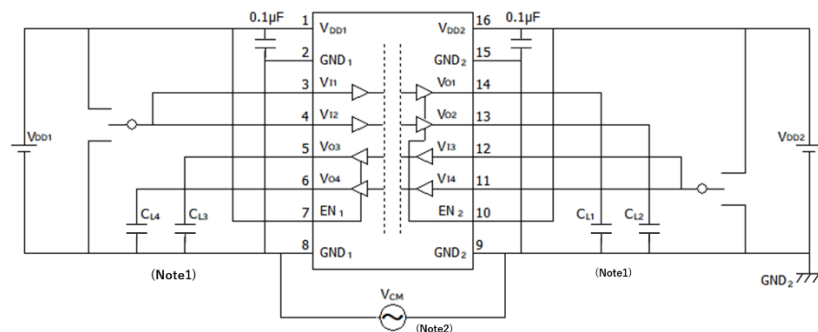


Fig. 12-3-3: DCL342L0B/DCL342H0B Common-Mode Transient Immunity Test Circuit

Note1: $C_{LX} = 15 \text{ pF}$ includes instrumentation and fixture capacitance.

Note2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND₁ or with reference to GND₂.

13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

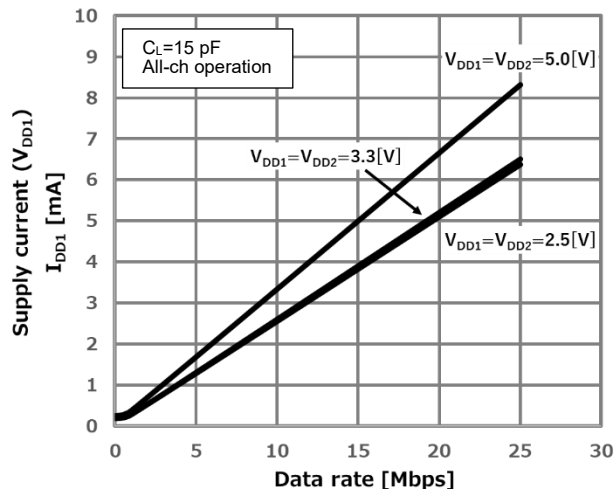


Fig.13.1. DCL340x0B I_{DD1} Supply Current - Data rate

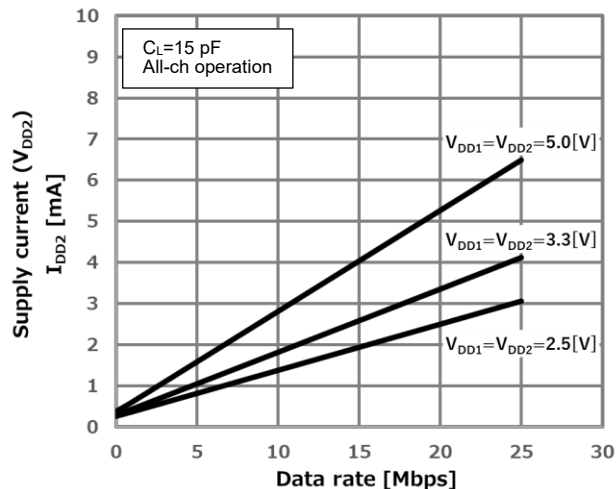


Fig.13.2. DCL340x0B I_{DD2} Supply Current - Data rate

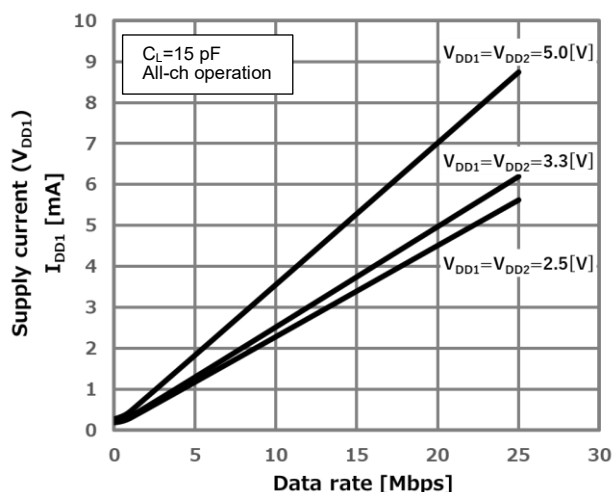


Fig.13.3. DCL341x0B I_{DD1} Supply Current - Data rate

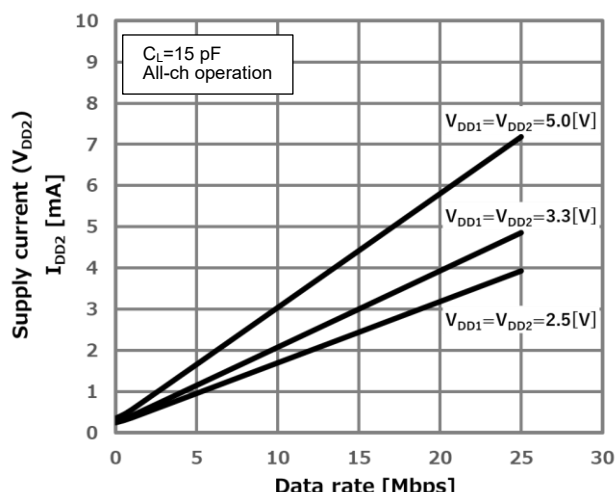


Fig.13.4. DCL341x0B I_{DD2} Supply Current - Data rate

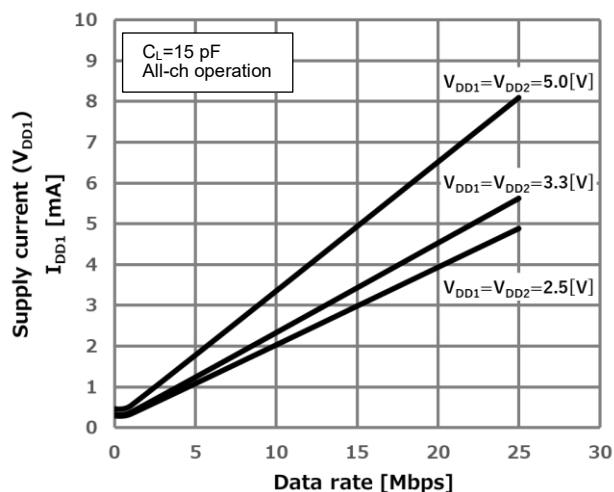


Fig.13.5. DCL342x0B I_{DD1} Supply Current - Data rate

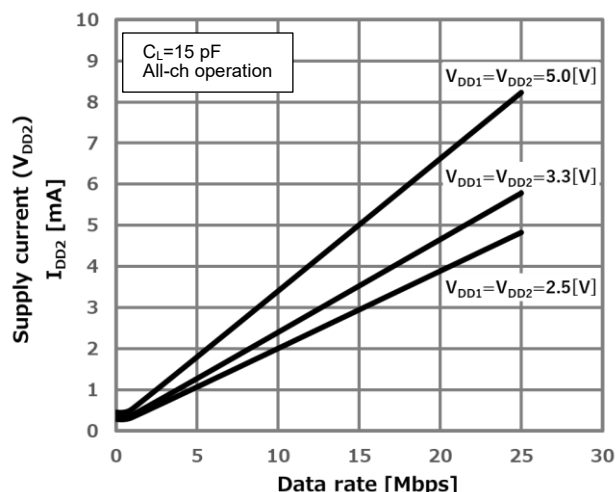


Fig.13.6. DCL342x0B I_{DD2} Supply Current - Data rate

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

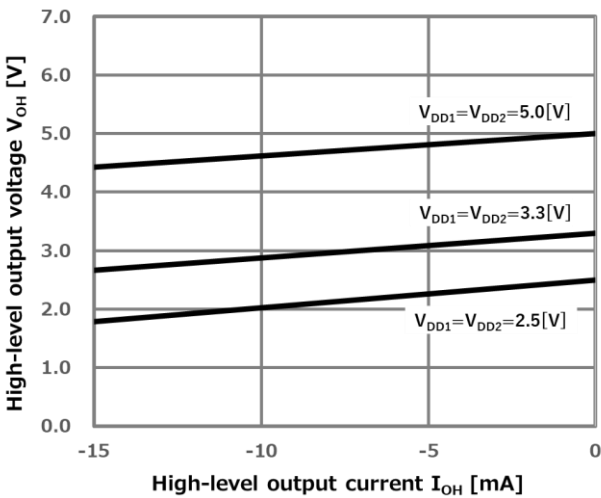


Fig.13.3. $V_{OH}-I_{OH}$

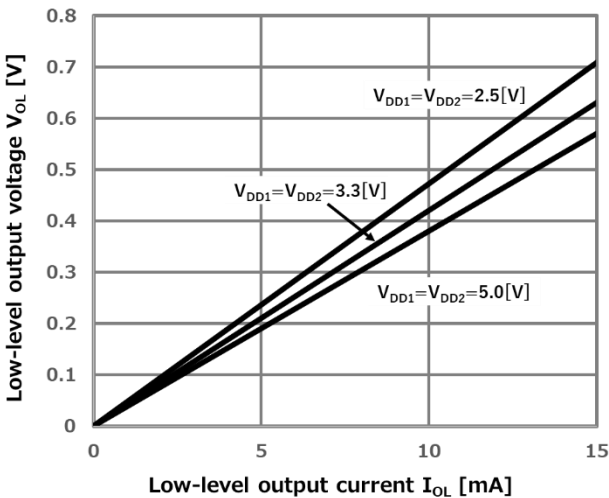


Fig.13.4. $V_{OL}-I_{OL}$

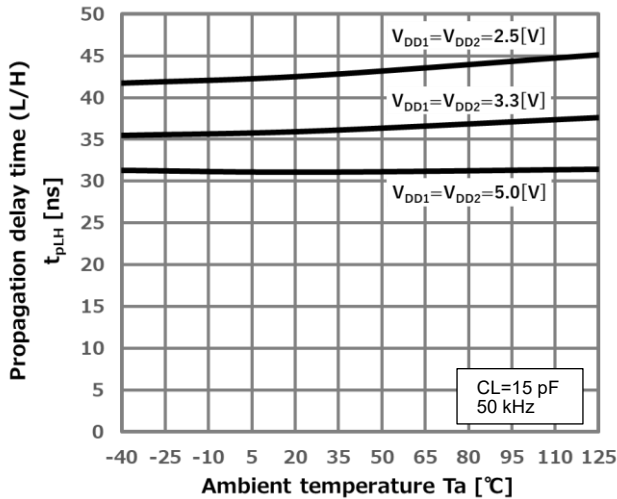


Fig.13.5. Propagation Delay Time $t_{pLH}-T_a$

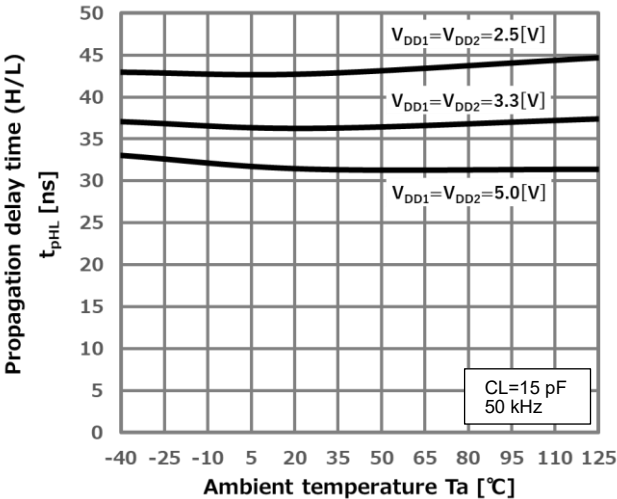
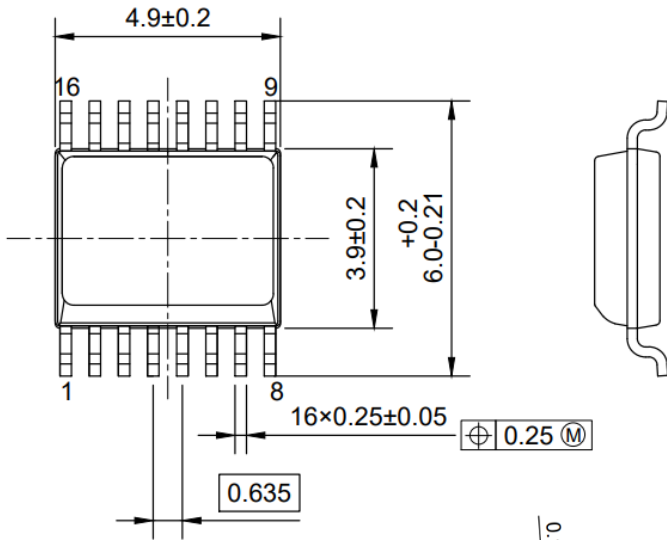
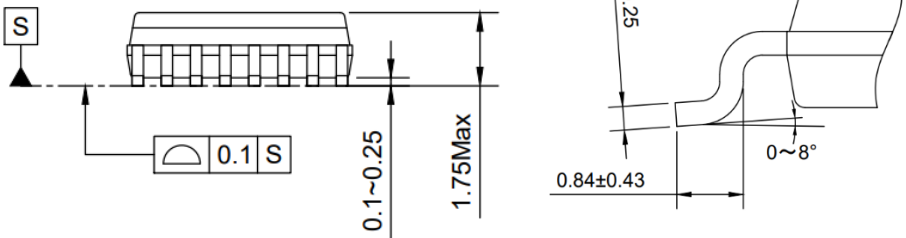


Fig.13.6. Propagation Delay Time $t_{pHL}-T_a$

14. Package Information

Package Name	SSOP16 (P-SSOP16-0405-0.64-001)
Implementation category	Surface Mount
Pin Number	16
Weight (g)	0.074 (Typ.)
Package Dimension (mm) Width × Length × Height	4.9 × 6.0 × 1.75 (Max)
Package Dimension(mm) / Land Pattern Example (mm)	Package Dimension  Land Pattern Dimensions (for reference only)  Notes : Land Pattern Dimensions • All linear dimensions are given in millimeters unless otherwise specified. • This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only. TOSHIBA is not responsible for any incorrect or incomplete drawings and information. • You are solely responsible for all aspects of your own land pattern, including but not limited to soldering processes. • The drawing shown may not accurately represent the actual shape or dimensions. • Before creating and producing designs and using, customers must also refer to and comply with the latest versions of all relevant TOSHIBA information and the instructions for the application that Product will be used with or for.

15. Ordering guide

Model	V _{DD1} end Number of inputs	V _{DD2} end Number of inputs	Default Output	Data rate [Mbps]	Control signal	Temperature range [°C]	Package
DCL340L0B	4	0	L	25	Output Enable	-40 ~ 125	SSOP16
DCL340H0B	4	0	H	25	Output Enable	-40 ~ 125	SSOP16
DCL341L0B	3	1	L	25	Output Enable	-40 ~ 125	SSOP16
DCL341H0B	3	1	H	25	Output Enable	-40 ~ 125	SSOP16
DCL342L0B	2	2	L	25	Output Enable	-40 ~ 125	SSOP16
DCL342H0B	2	2	H	25	Output Enable	-40 ~ 125	SSOP16

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