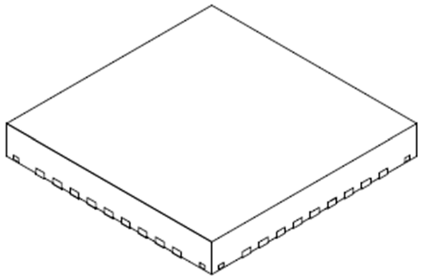
Bi-CMOS Linear Integrated Circuit Silicon Monolithic

TB9M040FTG

IC for automotive three-phase brushless DC motor

1. Description

The TB9M040FTG is an integrated IC combining an automotive microcontroller unit (MCU) and a motor driver. It incorporates Toshiba's unique Vector Engine (VE) to simplify motor vector control and reduce CPU load. The product is developed in accordance with ISO 26262 functional safety standards.



P-VQFN36-0606-0.50-004

weight: 0.102g (typ.)

2. Applications

For automotive equipment (electric valves, HVAC dampers, flaps, and grille shutters), three-phase small brushless DC motor control and drive.

3. Features

- System size reduction is achievable through integration of an MCU, a three-phase brushless DC motor driver, a high-side driver, a LIN transceiver, and an automotive power supply system.
- Built-in power MOSFETs enable direct drive of three-phase brushless DC motors.
- The high-side driver output can supply a 5 V power source.
- It features Toshiba's proprietary Vector Engine (VE), which reduces CPU load in FOC motor control applications.
- Built-in BEMF detection enables sensorless motor control.

Do not design your products or systems based on the information on this document. Please contact your Toshiba sales representative for updated information before designing your products.

4. Functions

- 32 bit Arm® Cortex®-M23 processor
  - Serial Wire Debug Support
  - 32ch Interrupt Controller
  - Up to 40 MHz clock frequency
- 12 KBytes ROM (BootLoader, Flash API) (incECC SEC/DED)
- 80 KBytes Code Flash (incl. ECC SEC/DED)
- 4 KBytes SRAM (incl. ECC SEC/DED)
- 32-bit Compare Timers (DTIMER)
- 28-bit Capture Timer (8 inputs, 6 measurements)
- Watchdog Timer (WATCHDOG)
- Power saving modes (CPU Sleep, Standby)
- 4ch Pulse Width Modulator Generator (PWMGEN)
- CRC
- 10 General-purpose I/O Ports (GPIO)
- 12-bit A/D Converter (MADC) with 4 analog inputs + internal monitors
- Vector Engine (VE)
- Programmable Motor Driver (PMD)
- Encoder (ENC)
- LDOs (LDO5V, LDO15V)
- High Side Driver
- Power On Reset (POR5V, PORL)
- 2 on-chip OSCs (IOSCH, IOSCL)
- External OSC
- PLL
- LIN ISO17987 transceiver + controller
- 1 full duplex serial interfaces (UART) with LIN support
- SPI-I/F
- Motor driver (2A max×3ch) with built-in shunt resistor including charge pump
- High-speed operational amplifier for motor current sensing via shunt
- Over current protection (LDO, Motor driver)
- Over temperature protection
- Package P-VQFN36-0606-0.50
- Single power supply from 6.0V to 18V
- Temperature Range Tj = -40°C to +175°C
- Green package (RoHS compliant)
- AEC-Q100 grade 0 qualified

5. Block Diagram

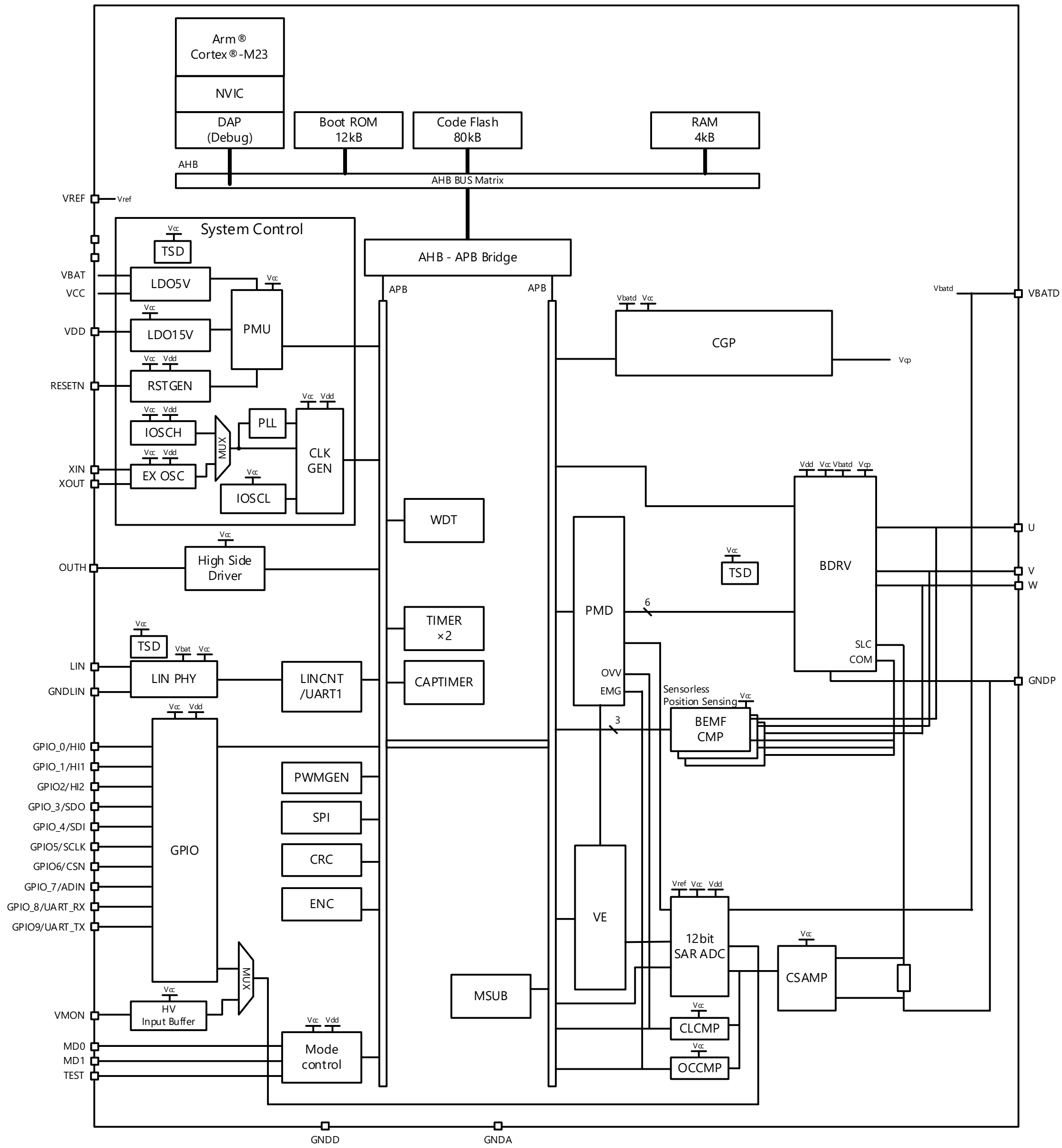


Figure 5.1 Block Diagram

6. Pin Assignments

(Top view)

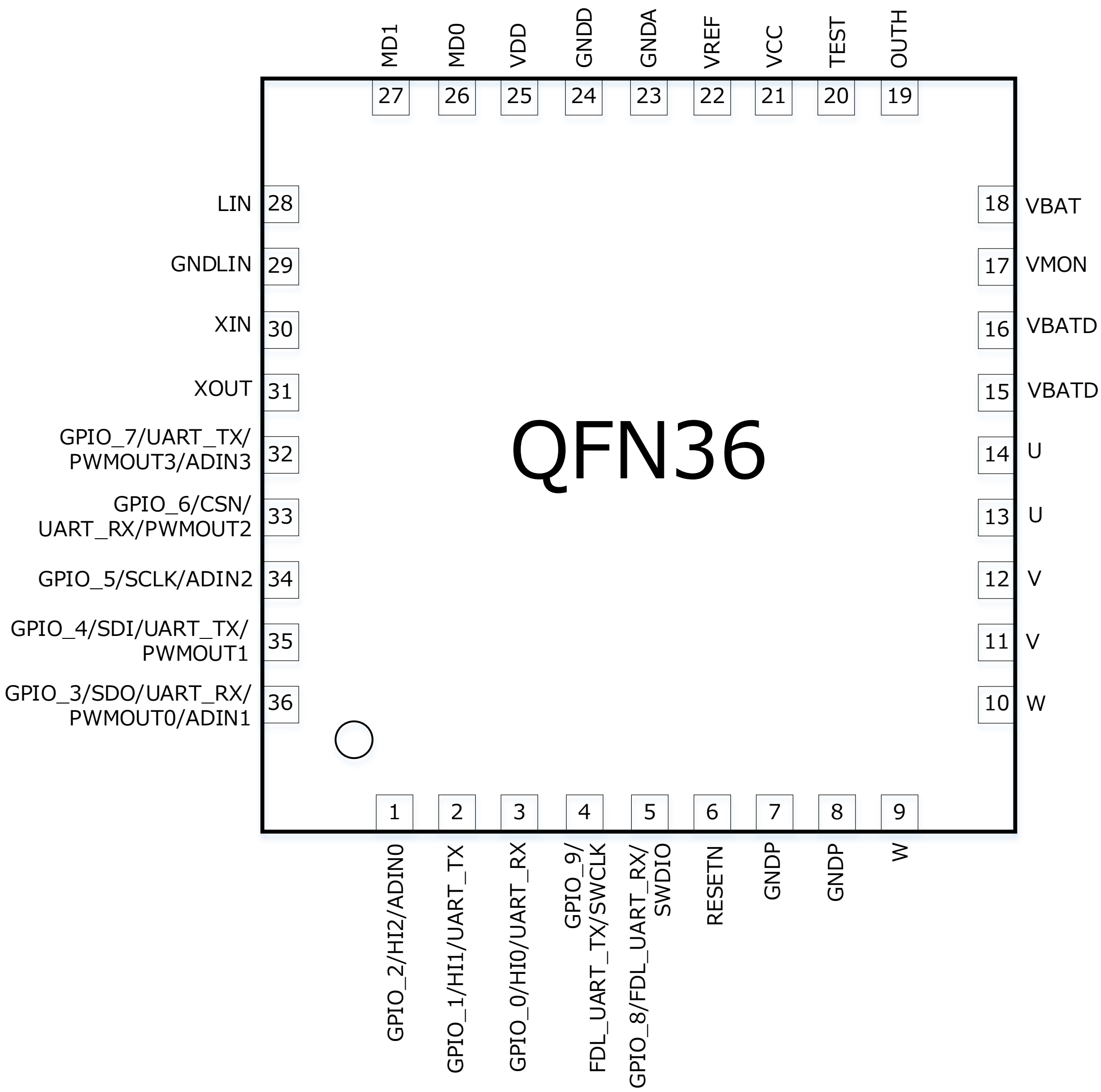


Figure 6.1 Pin Assignment Diagram

7. Pin Description

Table 7.1 Pin Description

Pin No.	Symbol	I/O	Description
1	GPIO_2/HI2/ADIN0	I/O	General-purpose I/O port / Hall sensor input / 12-bit ADC input
2	GPIO_1/HI1/UART_TX	I/O	General-purpose I/O port / Hall sensor input / UART_TX
3	GPIO_0/HI0/UART_RX	I/O	General-purpose I/O port / Hall sensor input / UART_RX
4	GPIO_9/FDL_UART_TX/SWCLK	I/O	General-purpose I/O port / FDL_UART TX / Debug SWCLK
5	GPIO_8/FDL_UART_RX/SWDIO	I/O	General-purpose I/O port / FDL_UART RX / Debug SWDIO
6	RESETN	I/O	Reset I/O
7	GNDP	-	Power GND
8	GNDP	-	Power GND
9	W	I/O	Phase-W motor connection pin
10	W	I/O	Phase-W motor connection pin
11	V	I/O	Phase-V motor connection pin
12	V	I/O	Phase-V motor connection pin
13	U	I/O	Phase-U motor connection pin
14	U	I/O	Phase-U motor connection pin
15	VBATD	I	Battery voltage regulator input for driver circuit
16	VBATD	I	Battery voltage regulator input for driver circuit
17	VMON	I	Battery voltage regulator input (for ADC input)
18	VBAT	I	Battery voltage regulator input
19	OUTH	O	High side driver output (VCC)
20	TEST	I	Test mode select
21	VCC	O	5-volt regulator output
22	VREF	I	ADC reference voltage regulator input
23	GNDA	-	Analog GND
24	GNDD	-	Digital GND
25	VDD	O	1.5-volt regulator output
26	MD0	I	Mode select
27	MD1	I	Mode select
28	LIN	I/O	LIN bus line
29	GNDLIN	-	Ground for LIN Phy
30	XIN	I	Crystal or ceramic oscillator connection pin
31	XOUT	O	Crystal or ceramic oscillator connection pin
32	GPIO_7/UART_TX/PWMOUT3/ADIN3	I/O	General-purpose I/O port / UART_TX / PWM output / 12-bit ADC input
33	GPIO_6/CSN/UART_RX/PWMOUT2	I/O	General-purpose I/O port / SPI chip select / UART_RX / PWM output
34	GPIO_5/SCLK/ADIN2	I/O	General-purpose I/O port / SPI data clock / 12-bit ADC input
35	GPIO_4/SDI/UART_TX/PWMOUT1	I/O	General-purpose I/O port / SPI data input / UART_TX / PWM output
36	GPIO_3/SDO/UART_RX/PWMOUT0/ADIN1	I/O	General-purpose I/O port / SPI data output / UART_RX / 12-bit ADC input / PWM output
-	EP	-	Exposed pad, connect to GND

8. I/O Equivalent Circuits

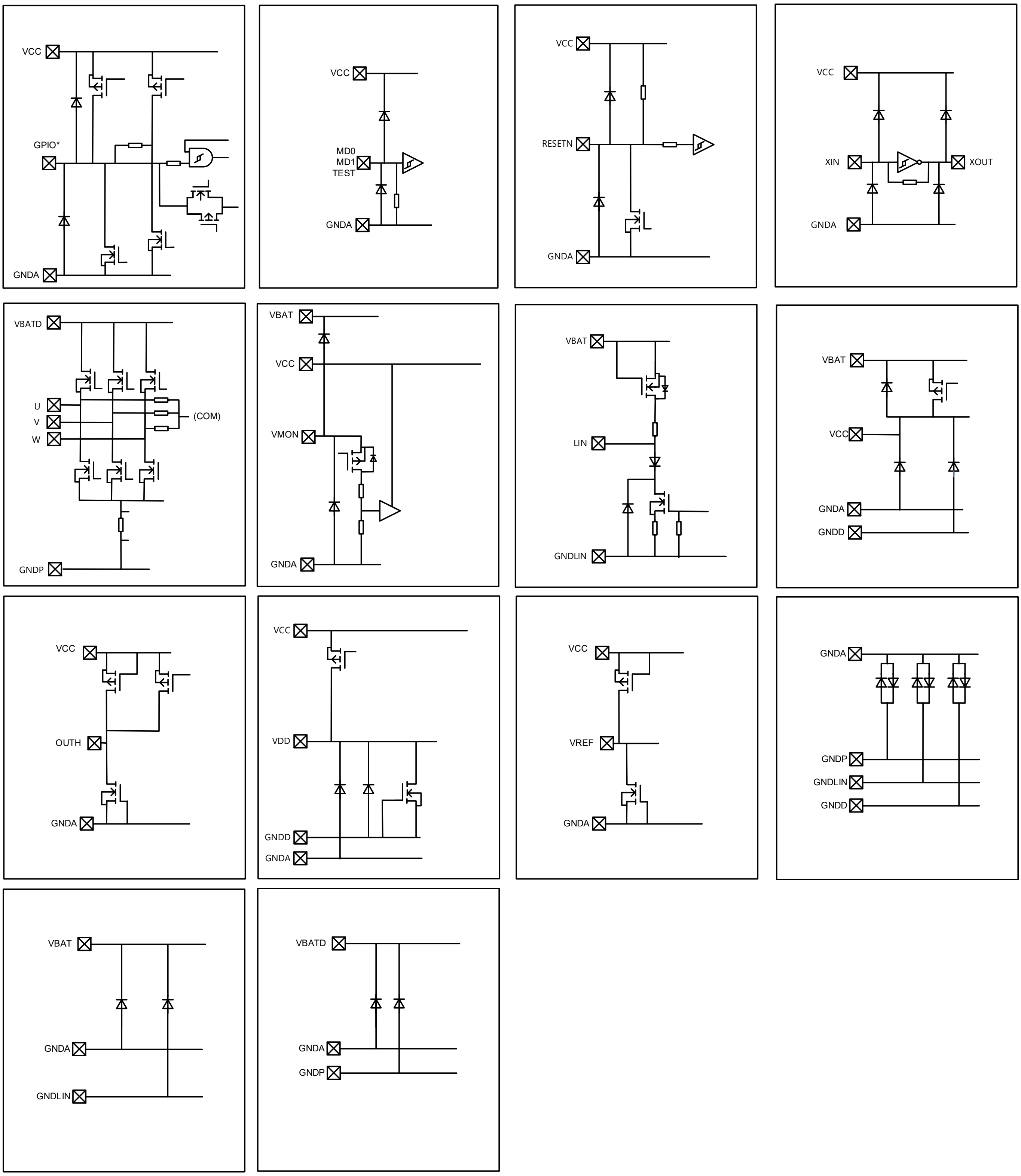


Figure 8.1 I/O Equivalent Circuit Diagrams

9. Functional Description

9.1. Bridge Drivers (BDRV) Circuit

- This is a three-phase inverter circuit (high-side Nch MOSFET / low-side Nch MOSFET) for driving a BLDC motor. (Maximum output current capability: 2A)
- The ON/OFF control is performed according to the drive signals from the digital circuit.
- Abnormal conditions are detected when the VDS of the built-in FET rises while the FET is ON (HSVDSDET, LSVDSDET).
- HSVDSDET can be enabled or disabled via register settings (flag output only).
- LSVDSDET can be enabled or disabled via register settings. When disabled, the flag is not asserted.
- When OCCMP, HSVDSDET, or LSVDSDET is detected, BDRV output is set to Hi-Z state for protection (forced off).
- A back-EMF position detection circuit using a virtual neutral point method is integrated.

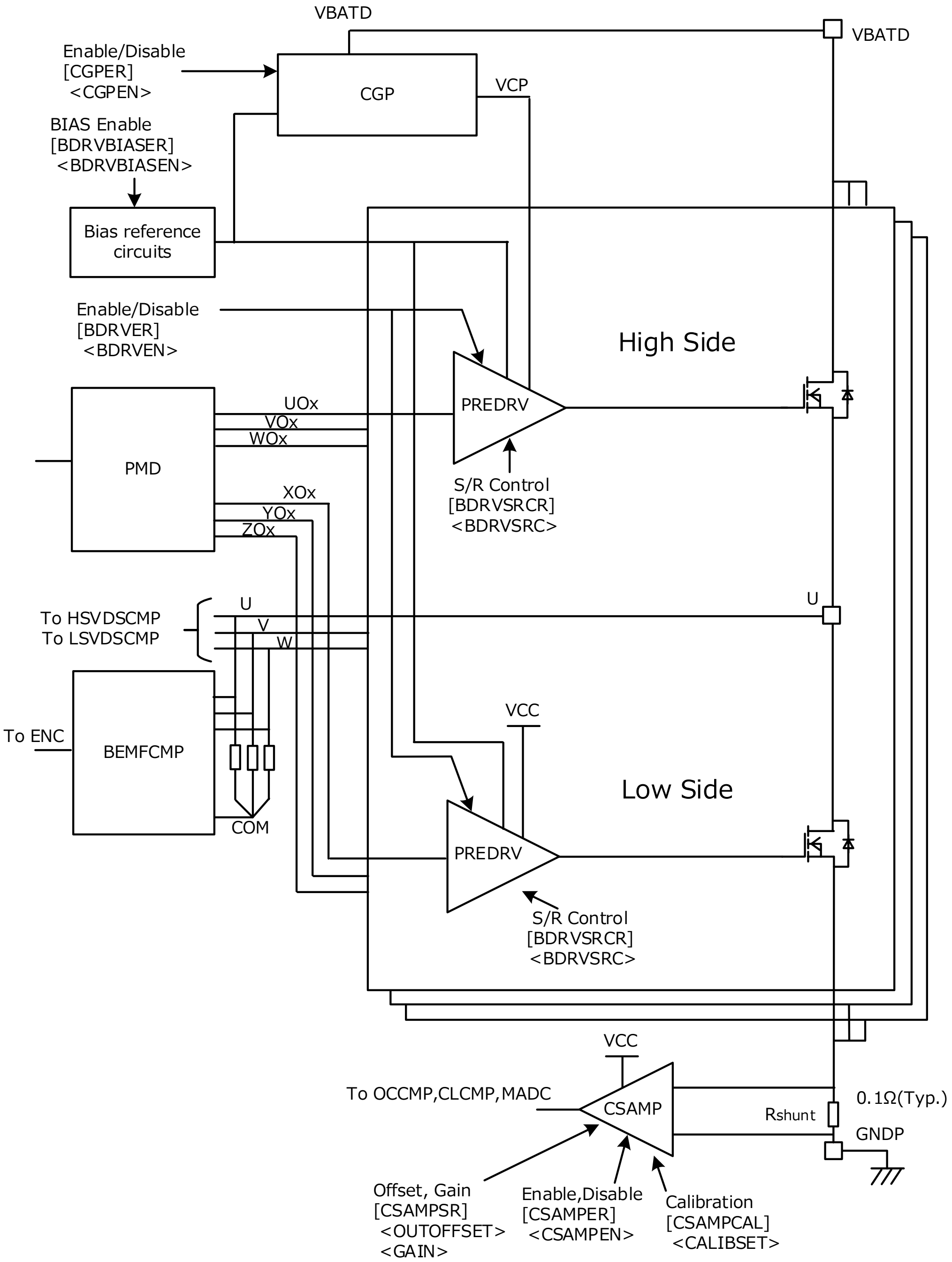


Figure 9.1.1 BDRV Circuit Diagram

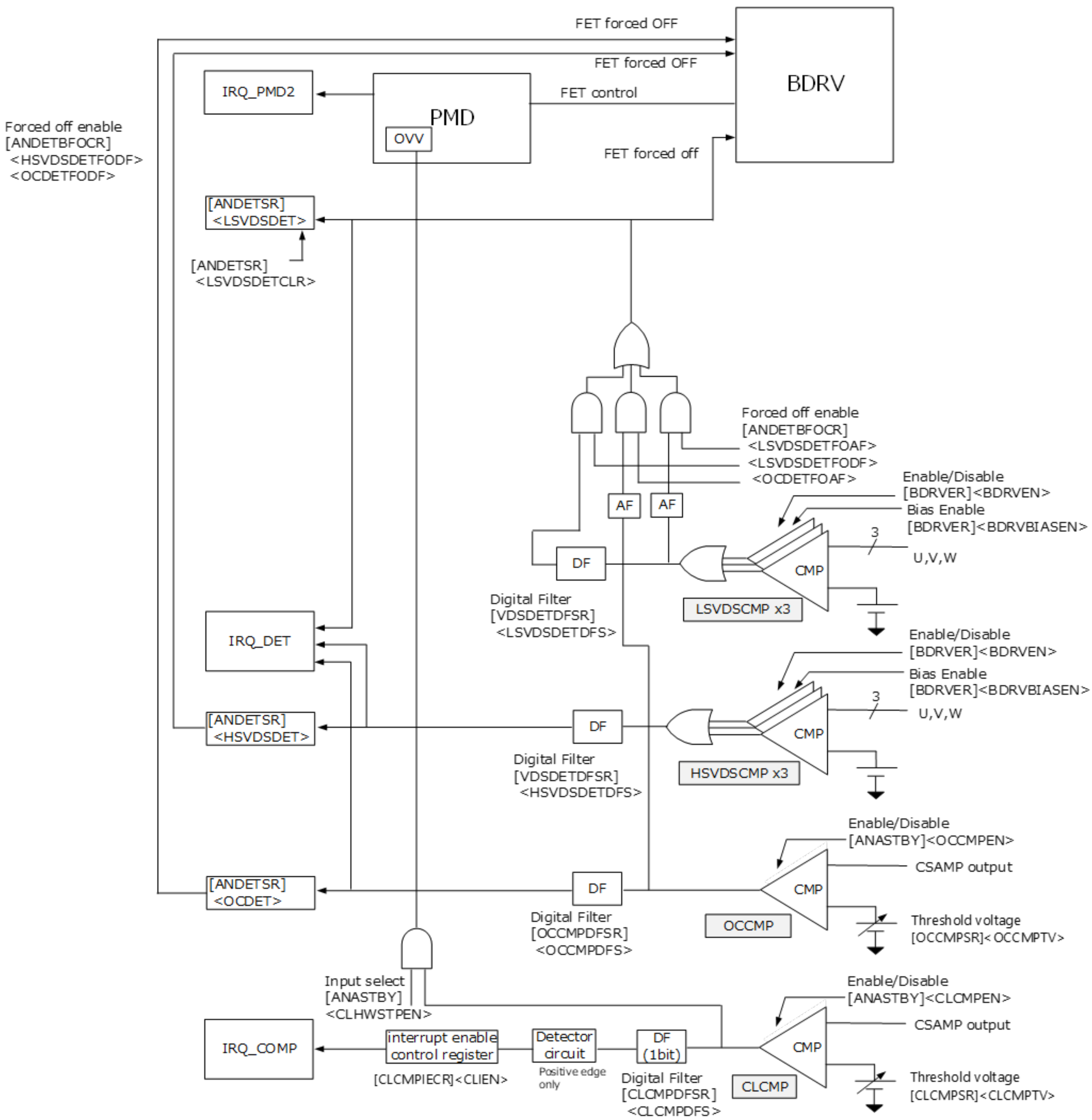


Figure 9.1.1 BDRV Abnormality Detection Block Diagram

9.2. High Side Driver (HSD)

- This product incorporates one channel of a high-side driver (HSD), powered from VCC (5 V).
- The HSD channel includes an overcurrent detection function.
- The HSD channel can be configured for either register control or PWM control.

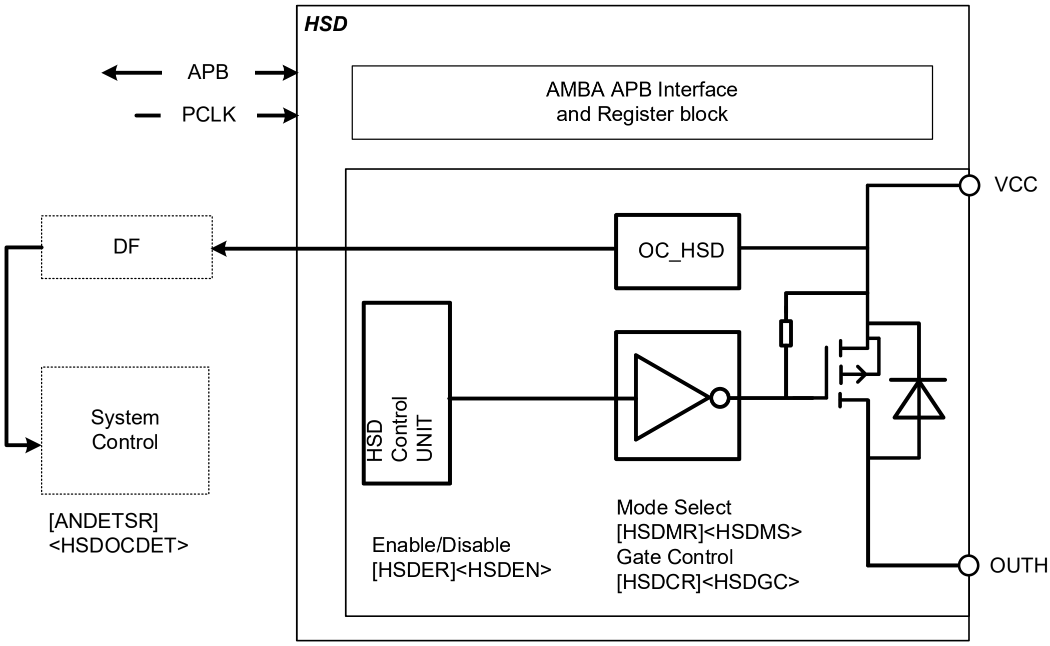


Figure 9.2.1 High Side Driver Block Diagram

9.3. Current-Sense Amplifier (CSAMP)

- The Current-Sense Amplifier (CSAMP) amplifies the voltage across the built-in shunt resistor (Typ. 0.1Ω) by the gain programmed via a 3-bit register field.
- The amplified output is sent to the 12-bit ADC (MADC), overcurrent detection comparator (OCCMP), and current limit comparator (CLCMP).
- The output offset voltage can be adjusted.

Refer to Figure 9.1.1 "BDRV Block Diagram" for the module configuration of CSAMP.

9.4. Current Limit Comparator (CLCMP)

- This function performs current limiting when the output of the current-sense amplifier exceeds a threshold value.
- The voltage output from the current-sense amplifier is input to this comparator.
- The CLCMP incorporates a digital filter to prevent malfunction caused by noise.

For the configuration related to abnormality detection, refer to Figure 9.1.2 BDRV Abnormality Detection Block Diagram.

9.5. Overcurrent Detection Comparator (OCCMP)

- This function detects an abnormal condition when the output of the current-sense amplifier exceeds a threshold value.
- The overcurrent detection function can be enabled or disabled (flag only) via register settings.
- The OCCMP incorporates a digital filter to prevent malfunction caused by noise

For the configuration related to abnormality detection, refer to Figure 9.1.2 BDRV Abnormality Detection Block Diagram.

9.6. Vector Engine(VE)

Table 9.6.1 VE Function List

Category	Function	Description
Calculation	Basic functions	Fixed-point calculation Vector control tasks Tasks for interfacing with the PMD and MADC
	Current control tasks	PI control of d-axis and q-axis currents ・Non-interference control ・Output limiting based on scalar voltage values
	SIN/COS Calculation 1 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	SIN/COS Calculation 2 task	Calculates the sine and cosine values of phase θ
	SIN/COS Calculation 3 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	Output Voltage Transformation task	・Coordinate axis transformation (inverse Park transformation) 2 types of phase transformation (space vector modulation and inverse Clark transformation)
	Output Control task	Converts three-phase voltage into PWM output settings for the PMD (2 types) ・Allows output limiting ・Allows dead-time compensation
	Trigger Generation task	Calculates the PMD's AD conversion sampling timing from three-phase duty cycles (2 types)
	Current Correction Preparation task	Corrects detected current values for low inductance motor. Used in combination with Input Process 6 tasks.
	Input Process tasks	Reads conversion results from the MADC and converts them into fixed-point values (4 types) Supports current polarity determination (hysteresis/reverse hysteresis)
	Input current transformation task	・Phase transformation (Clark transformation) ・Coordinate axis transformation
	Individual functions task	・Arctangent (ATAN) calculation ・Square-root calculation ・No Operation(NOP)
	Position Estimation task	Calculates electrical angular velocity and phase θ from motor parameters, voltage, and current (2 types)
	Position Sensor Input Process task	Calculates phase θ and electrical angular velocity from the inputs from a position sensor such as an encoder that generates multiple pulses per revolution
Schedule management	Program Schedule control	・Program schedule capable of defining the order in which to execute tasks and their start-up control ・Supports up to 32 tasks
	Start-up control	・Repetition start ・Starts the input schedule upon completion of an AD conversion Starts executing an Input Process task upon ADC-complete interrupt when the VE is in the Standby state following the completion of an output schedule
Interrupt control	Schedule-complete interrupt	Generates an interruption when a task with the END flag set to "1" is executed repeatedly for the specified number of times ([REPTIME]).
	Error interrupt	Interrupt generated when the VE receives a PWM interrupt from the PMD during the execution of an output schedule, judging it as an error.

Other	Outputs for debugging	Outputs a signal that indicates that the task is running by toggling the debug output when the task starts and stops. For example, depending on the timing of the PMD debug output, the period indicating the operation may appear to be inverted (L output). This can be monitored by the debug output function of the PMD.

9.7. Programmable Motor Driver (PMD)

Table 9.7.1 PMD Function List

Category	Function	Description
PWM output	Resolution	The count resolution for PWM carriers is 1/VECLK. The PWM frequency and duty cycle are programmed with 15-bit values.
	PWM carrier generation	Capable of generating PWM carriers with a frequency between 0.06 kHz and 117.18 kHz (when VECLK=60 MHz) and with a 15-bit amplitude ・Four types of carrier waveform (triangular, sawtooth, inverted triangular, and inverted sawtooth) ・Selectable carrier waveforms for each phase ・Capable of producing phase differences between the base carrier and each of the U, V, and W phases independently.
	Three-phase PWM generation	Three-phase PWM waveforms are generated by comparing the PWM carriers and the programmed duty cycles. The duty cycles of the three phases can be the same or independently programmed.
	Commutation control	Each of the six output ports can be programmed to be driven to the PWM output level, logic High, or logic Low. PWM waveforms can be generated independently for each of the three phases with a common PWM carrier (three-phase complementary PWM).
AD conversion triggering	Synchronous ADC trigger generation	Generates MADC synchronous trigger signals to start AD conversion at any timing synchronous to the PWM carrier
Protection functions	Protection control	Turns off the PWM outputs in response to a protection input signal ・ Provides protection control
	Dead-time control	Inserts a dead-time period to prevent a short-circuit between high-side and low-side switches (U/X, V/Y, W/Z) during their switching when generating three-phase complementary PWM signals
Register buffering	–	Double- and triple-buffered registers allow the PWM period, duty cycles, ADC trigger timing, and the commutation control settings for the six output ports to be changed dynamically. ・ The update timing of execute buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, and 4) the center and end of the PWM period. ・ The update timing of intermediate buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, 4) the 1/4 point of the PWM period, 5) the 3/4 point of the PWM period, 6) center and end point of the PWM period, and 7) the 1/4 and 3/4 point of the PWM period.
Interrupt requests	PWM interrupt (INTPWM)	Capable of generating interrupt requests synchronous to a PWM waveform ・ The interrupt timing is selectable from the center and end of the base carrier. ・ The interval between PWM interrupts is selectable from one-half, one, two, and four PWM periods. ・ Capable of enabling and disabling the decimation of synchronous MADC triggers and buffer updates when interruptions are decimated
	OVV interrupt (INTOVV)	Interrupt request generated in the event of a protection event via an OVV input
Debug output	–	Capable of monitoring the operating timing of the motor-related peripherals via an output port ・ Monitor timing of the synchronous MADC trigger output from the PMD ・ Monitor timing of interrupt requests from motor-related peripherals ・ Monitor MADC conversion ・ Monitor timing of VE task transitions ・ Monitor ENC internal signal.

9.8. Memory Map

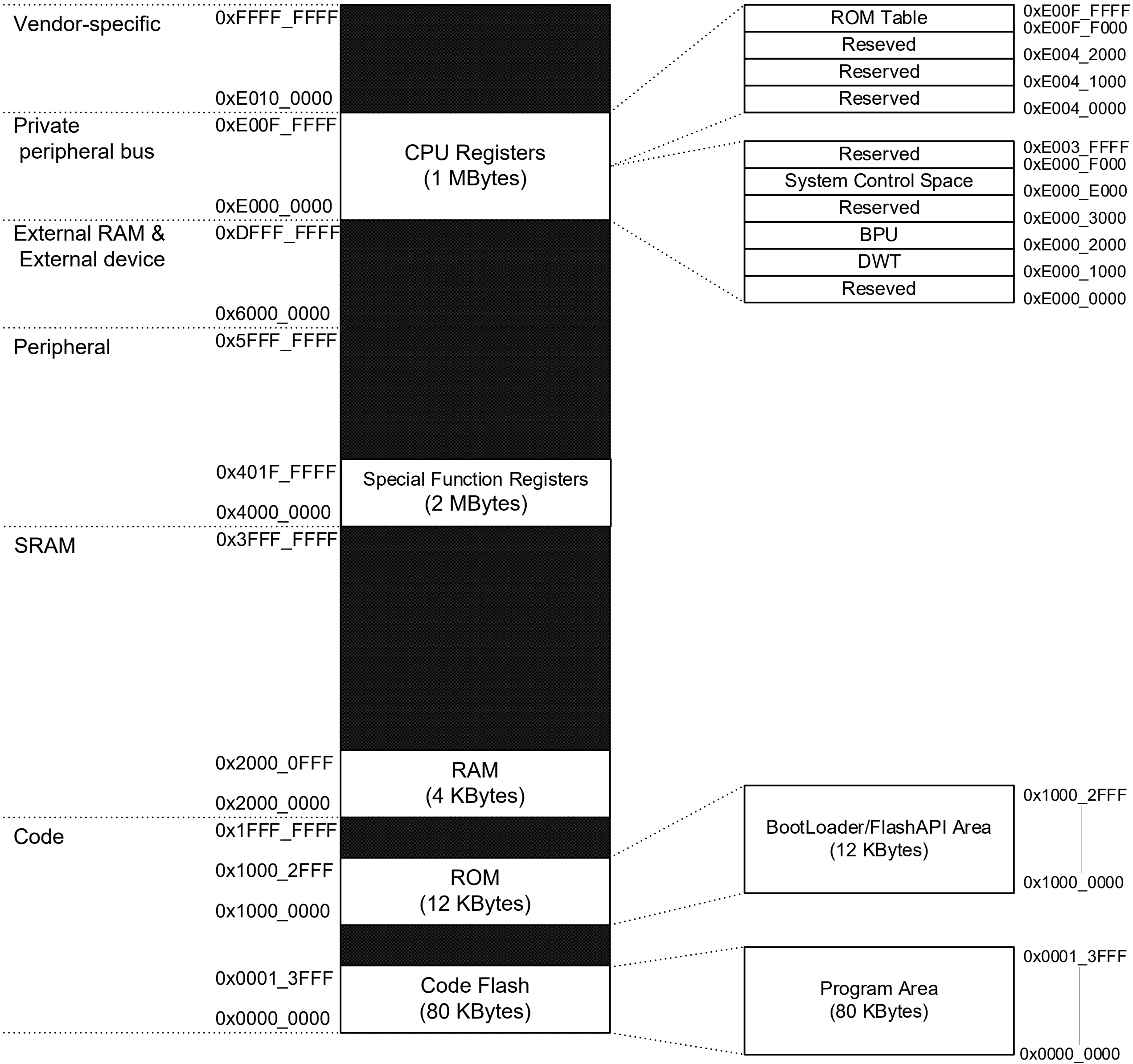


Figure 9.8.1 Memory Map (Normal/Debug Mode)

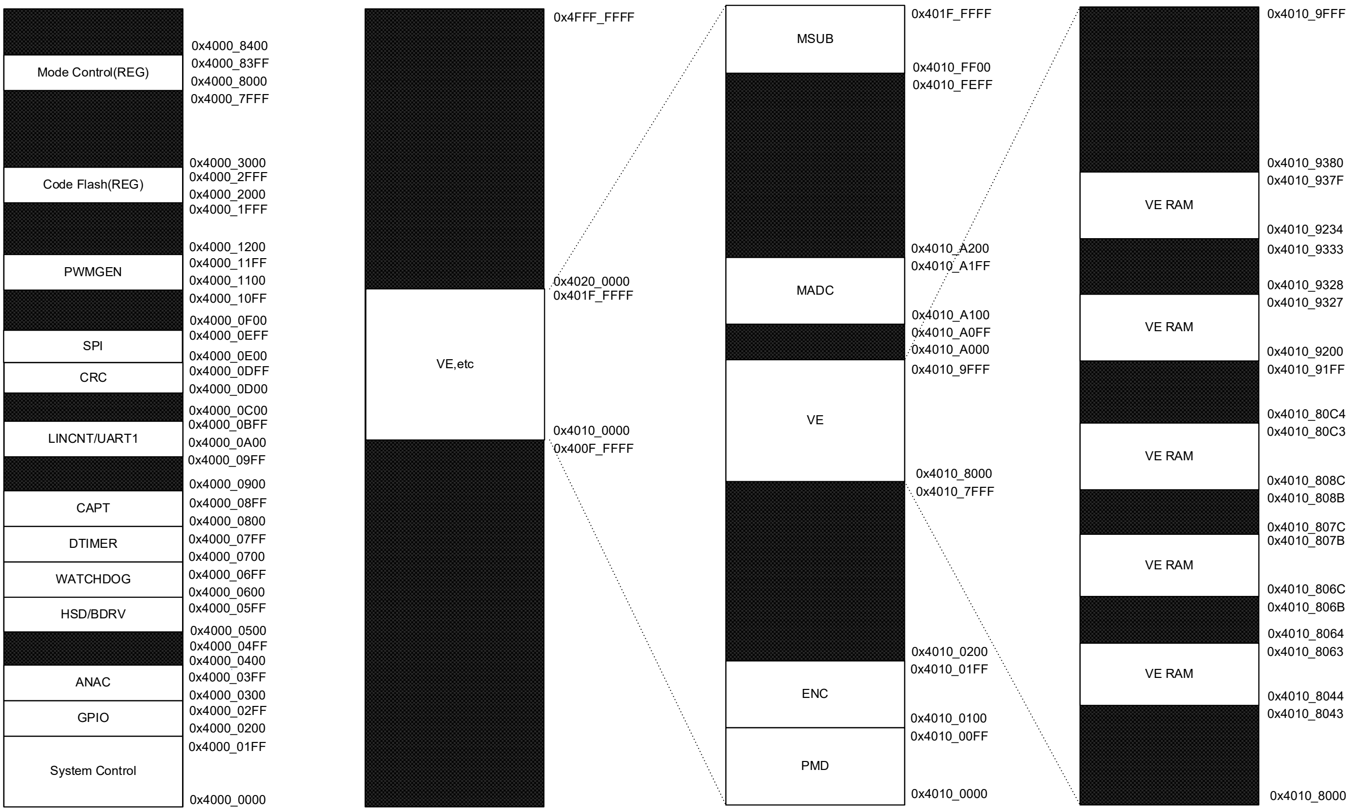


Figure 9.8.2 Memory Map (SPECIAL FUNCTION REGISTERS)

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

Table 10.1.1 Absolute Maximum Ratings

Characteristic	Symbol	Pin(s)	Rating	Unit
Supply voltage	Vbat	VBAT, VBATD	-0.3 to +40 (Note2)	V
	Vcc	VCC, VREF	-0.3 to +6	
	Vdd	VDD	-0.3 to +2.1	
Ground-to-ground voltage differential	Vgnd	GNDA, GNDD, GNDP, GNDLIN	-0.3 to +0.3	
Input voltage	Vin1	LIN	-27 to +40 (Note1)	V
	Vin4	VMON	-0.3 to Vbat+0.3 (40 V max)	
	Vin7	TEST, MD0, MD1, RESETN GPIO_x, XIN	-0.3 to Vcc+0.3 (6 V max)	
Output voltage	Vout1	LIN	-27 to +40 (Note1)	V
	Vout5	XOUT, RESETN GPIO_x	-0.3 to Vcc+0.3 (max 6V)	
	Vout6	OUTH	-0.3 to Vcc+0.3 (max 6V)	
	Vout7	U,V,W	-0.3 to Vcc+0.3 (max 40V)	
Operating temperature	Ta	-	-40 to +150	°C
Storage temperature	Tstg	-	-55 to +150	°C

Note:
- The absolute maximum ratings must never be exceeded, even momentarily. Exceeding these ratings might cause permanent destruction or degradation of an IC and adversely affect other components. Ensure that the design prevents exceeding the absolute maximum ratings under any operating conditions. Additionally, always operate within the specified operating range.
- For ratings above ±18V, there are time limitations: 18–28V (≤ 90 minutes), 28–40V (≤ 400 ms).
- Do not allow the output current at the U, V, and W terminals to remain at 2 A or higher for longer than 10 ms.

Note1: VBAT = 6.0 to 18 V
Note2: A temporary voltage difference between the VBAT pin and the VBATD pin is acceptable. However, if voltage is applied to VBATD while LDO5V is not operating properly, the system may lose control and behave unpredictably.

10.2. Operating Ranges

Table 10.2.1 Operating Ranges

Characteristic	Symbol	Rating	Unit	Remarks
Supply voltage	Vbat	18 to 27	V	Electrical characteristics are not guaranteed. (Note1)
		6 to 18		Vbat range in which electrical characteristics are guaranteed.
Operating temperature	Topr	-40 to 150	°C	Ambient temperature, Ta
		-40 to 175		Junction temperature, Tj (Note1)

Note1: Not tested in a pre-shipment test

10.3. Overall Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Standby current 1	Istby1	VBAT VBATD VMON	Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=25°C	-	-	20	μA
Standby current 2	Istby2		Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=70°C Guaranteed by design	-	-	90	μA

10.4. Reset Generator and Standby Time

Vbat=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Low-level reset output voltage	Voutlrst	RESETN	Iout=+5 mA	0	-	0.4	V
High-level input threshold voltage	Vihrst		-	VCC ×0.75	-	-	V
Low-level input threshold voltage	Vilrst		-	-	-	VCC ×0.25	V
Input noise filter (analog)	Tfilrst		-	10	20	40	μs
Input pull-up resistor	Rpullup		Between the VCC and RESETN pins	30	50	100	kΩ
WATCHDOG reset time	Twdt	-	Time from a WATCHDOG reset request to an internal reset release (except when the flash memory is busy)	-	70	-	μs
Power-on reset settling time	Trst1	-	Time from recovery from a VCC undervoltage condition to a CPU reset release	-	-	8	ms
Recovery settling time	Trst2	-	Time from when a wake-up request is detected to when a CPU reset is released after the LDO15V stabilizes	-	-	2	ms
External oscillator settling time	Trst3	-	Time from when the oscillator is started by software to when it settles to a steady state (when a 16-MHz CERALOCK ceramic resonator from Murata is used)	-	-	1	ms
PLL settling time	Tpll	-	-	-	-	140	μs

Note: The startup stabilization time is extended by up to 10 ms when [ANUCONFSR]<CPLDO15>=0 (cool-down period of 10 ms). When <CPLDO15>=1, no additional time is required.

10.5. 5-V Regulator (LDO5V)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VCC output voltage 1	Vcc1	VCC	Iload = -10 μA to -135 mA (Total VCC/VDD current consumption of maximum self-consumption current inside the IC and external load current on OUTH (max 40 mA)) Tj = -40 to 150°C	4.9	5.0	5.1	V
VCC output voltage 3	Vcc3		Iload = -10 μA to -135 mA (Total VCC/VDD current consumption of maximum self-consumption current inside the IC and external load current on OUTH (max 40 mA)) Tj = 150 to 175°C	4.8	5.0	5.2	V
Current limit 1	Ilimit1		VCC ≥ 4.0 V	-850	-475	-250	mA
Current limit 2	Ilimit2		VCC ≤ 3.0 V	-260	-112	-10	mA
Dropout voltage	Vdrop		Vbat = 4.8 V,Iload = -120 mA < (-5mA + current consumed by LDO5V)	-	0.2	0.45	V
Undervoltage detection voltage 1	Vrst1		VCC falling (UV_VCC)	4.0	-	4.35	V
Undervoltage release voltage 1	Vrstr1		VCC rising (UV_VCC)	4.2	-	4.75	V
Undervoltage detection voltage 3	Vrst3		VCC falling (POR5V)	3.07	3.45	3.83	V
Undervoltage release voltage 3	Vrstr3		VCC rising (POR5V)	3.22	3.60	3.98	V

Note:
- Connect a capacitor of 1.0 μF or more as close as possible to the VCC pin.
- The current limit at VCC in Standby mode is Current Ilimit2.

10.6. 1.5-V Regulator (LDO15V)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VDD output voltage	Vdd	VDD	Iload = -10 μA to -60 mA + (Total VDD current consumption of maximum self consumption current inside the IC and external load current (max 1mA))	1.45	1.5	1.55	V
Current limit 3	Ilimit3		-	-250	-150	-70	mA
Undervoltage detection voltage 2	Vrst2		VDD falling	1.3	-	1.4	V
Undervoltage release voltage 2	Vrstr2		VDD rising	1.35	-	1.45	V
Overvoltage detection/release voltage	Vddov		-	1.55	-	1.65	V

Note: Connect a capacitor of 2.2 μF or more as close as possible to the VDD pin.

10.7. Charge Pump

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output voltage 1	Vcp1	VCP	-	-	VBATD+ 4.7	-	V
Boost overvoltage detection threshold voltage	Vcplim1	VCP	-	31	33	35	V
Boost overvoltage recovery threshold voltage	Vcplim_r1	VCP	-	29.5	31.5	33.5	V
Boost disable threshold voltage 2	Vcpstop2	VCP	-	34	36	38	V
Boost enable threshold voltage 2	Vcpstop_r2	VCP	-	32	34	36	V
Boost drop detection threshold voltage	Uvvcpdet	VCP,VBATD	VCP-VBATD	2.3	2.65	3.00	V
Boost drop release threshold voltage	Uvvcprel	VCP,VBATD	VCP-VBATD	2.35	2.70	3.05	V

Note: Enable the charge pump when VBAT ≥ 5 V.

10.8. Oscillator

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Oscillation frequency 1 (HFCLK)	Fosc1	-	-	19	20	21	MHz
Oscillation frequency 2 (LFCLK)	Fosc2	-	-	24	32	40	kHz
Oscillation frequency 3 (XCLK)	Fosc3	XIN XOUT	Supported external ceramic resonators or crystal oscillator parameters	16 (Note1)	-	20 (Note1)	MHz

Note1: Typical value of an external oscillator.
Contact the manufacturer of external components for the matching with XCLK.
Toshiba has tested the CSTNE16M0VH3C000R0 and CSTNE20M0VH3C000R0 and confirmed that they operate with the XCLK properly.

10.9. 12-bit ADC

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Conversion time 1	Tconv1	-	Settling time + Conversion time MADCCLK=30MHz	-	1.33	-	µs
INL1	Inl1	-	Guaranteed by design	-2	-	2	LSB
DNL1	Dnl1	-	Guaranteed by design	-1	-	2	LSB
Total error 1	Err_total1	-	Guaranteed by design	-6	-	6	LSB
Input voltage division ratio	Ratio_r1	VBATD	Buffer input voltage division ratio Input voltage range: 6 to 27 V	0.095	0.1	0.105	Times
Amplifier Error	Err_amp2	-	Buffer AMP input/output error: Input voltage range: 0.2 V to power supply voltage	-10	-	10	mV

Note: The pull-down resistor for input attenuation when the 12-bit ADC is enabled is 250 kΩ (typ.).

10.10. Bridge Drivers (BRDV)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
ON Resistance 1	Ron1	VBATD,U,V,W,GNDP	Output = High (Between VBATD and U, V, W) Tj = –40 to 150°C	-	0.43	(0.8)	Ω
ON Resistance 2	Ron2	VBATD,U,V,W,GNDP	Output = Low (Between U, V, W and GNDP) Tj = –40 to 150°C	-	0.5	(0.9)	Ω
Peak Output Current	Idrvpeak	VBATD,U,V,W,GNDP	(Note1)	-2	-	2	A
RMS Output Current	Idrvrms	VBATD,U,V,W,GNDP	(Note1)	-1.4	-	1.4	A
Output Off-Leakage 1	Ioff1	VBATD,U,V,W,GNDP	Output = OFF, U = V = W = VBATD (Note2)	-	-	10	μA
Output Off-Leakage 2	Ioff2	VBATD,U,V,W,GNDP	Output = OFF, U = V = W = 0 V (Note2)	-10	-	-	μA
Slew Rate 1	Drvsr1	U,V,W	[BDRVSRCR]<BDRVSRC>=101 VBATD=12V、Rload=12Ω Rise 10⇒90% (VBATD)	5.83	17.5	52.5	V/μs
Slew Rate 2	Drvsr2	U,V,W	[BDRVSRCR]<BDRVSRC>=101 VBATD=12V、Rload=12Ω Fall 90⇒10% (VBATD)	5.83	17.5	52.5	V/μs
VDS Detection Threshold 1	VDS1	U,V,W	High Side (Output = High)	1.60	2.36	2.88	V
VDS Detection Threshold 2	VDS2	U,V,W	Low Side (Output = Low)	2.38	3.61	5.00	V
Digital Filter Time 1	Tvdsfil1	-	Filter Time Setting Register: [VDSDETDFSR]<LSVDSDETDFS>=111 Match 256 times at 10 MHz	24.4	25.6	26.9	μs
Digital Filter Time 2	Tvdsfil2	-	Filter Time Setting Register: [VDSDETDFSR]<LSVDSDETDFS>=000 Match 8 times at 10 MHz	0.76	0.8	0.84	μs
Digital Filter Time 3	Tvdsfil3	-	Filter Time Setting Register: [VDSDETDFSR]< HSVDSDETDFS>=111 Match 256 times at 10 MHz	24.4	25.6	26.9	μs
Digital Filter Time 4	Tvdstfil4	-	Filter Time Setting Register: [VDSDETDFSR]< HSVDSDETDFS>=000 Match 8 times at 10 MHz	0.76	0.8	0.84	μs
Dead Time	Tdead	-	Dead Time Setting Register: [DTR]<DTR[9:0]> = 0x02D 3 μs setting, VECLK = 60 MHz	(TBD)	(TBD)	(TBD)	μs

Note1: The value applies when used within the Tj temperature range. It is a specification value based on the condition that thermal management for both the board and the IC keeps Tj ≤ 175°C. It does not imply that heat generation is acceptable this current to flow.

Note2: Leakage current of the FETs in the BDRV block, excluding the current flowing through the induced voltage circuit.

10.11. Current-Sense Amplifier (CSAMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Gain 2	Gain2	-	Programmed to be ×10	0.84	1	1.16	Times
Gain 3	Gain3		Programmed to be ×15	1.26	1.5	1.74	Times
Gain 4	Gain4		Programmed to be ×20	1.68	2	2.32	Times
Gain 5	Gain5		Programmed to be ×40	3.36	4	4.64	Times
Gain 6	Gain6		Programmed to be ×60	5.04	6	6.96	Times
Output offset voltage 1	Vooffset1	-	Programmed to be V_{REF}/ 2 Gain60 after calibration, including input offset	V_{REF}/2 -0.0606	2.5	V_{REF}/2 +0.0606	V
Output offset voltage 2	Vooffset2	-	Programmed to be V_{REF}/ 5 Gain60 after calibration, including input offset	V_{REF}/5 -0.0606	1.0	V_{REF}/5 +0.0606	V
Output offset voltage 3	Vooffset3	-	Programmed to be V_{REF}/ 8 Gain60 after calibration, including input offset	V_{REF}/8 -0.0606	0.625	V_{REF}/8 +0.0606	V
Output offset voltage 4	Vooffset4	-	Programmed to be V_{REF}/ 10 Gain60 after calibration, including input offset	V_{REF}/10 -0.0606	0.5	V_{REF}/10 +0.0606	V
Settling time 2	Tsettle2	-	Gain = 20, output voltage: 2.5V ↔ 3.5 V No external input filter Time required for the output voltage to settle to within ±2% of its final value Guaranteed by design (See Figure 10.11.1)	-	-	0.8	μs
Settling time 3	Tsettle3	-	Gain = 60, output voltage: 2.5V ↔ 3.5 V No external input filter Time required for the output voltage to settle to within ±2% of its final value Guaranteed by design (See Figure 10.11.1)	-	-	1.7	μs
High-level output voltage	Voh_amp	-	-	VCC-0.3	-	-	V
Low-level output voltage	Vol_amp	-	-	-	-	0.3	V

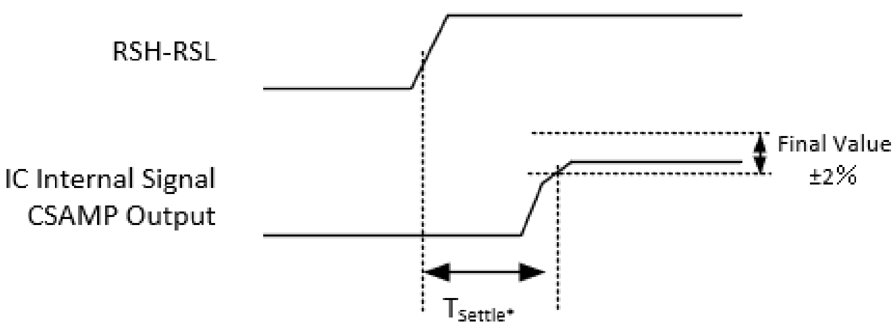


Figure 10.11.1 Measurement of Settling Time

10.12. Current Limit Comparator (CLCMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Current-limiting voltage threshold 1	Vlimit1	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV> = 00000 Minimum setting	VCC×32/64 -0.039	2.500	VCC×32/64 +0.039	mV
Current-limiting voltage threshold 2	Vlimit2	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV> = 00001	VCC×33/64 -0.039	2.578	VCC×33/64 +0.039	V
Current-limiting voltage threshold 3	Vlimit3	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV> = 00011	VCC×35/64 -0.039	2.734	VCC×35/64 +0.039	V
Current-limiting voltage threshold 4	Vlimit4	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV> = 00111	VCC×39/64 -0.039	3.047	VCC×39/64 +0.039	V
Current-limiting voltage threshold 5	Vlimit5	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV> = 01111	VCC×47/64 -0.039	3.672	VCC×47/64 +0.039	V
Current-limiting voltage threshold 6	Vlimit6	-	Current Limit Threshold Setting Register: [CLCMPSR]<CLCMPTV>=11111 Maximum setting	VCC×63/64 -0.039	4.922	VCC×63/64 +0.039	V
Digital filtering time 1	Tclfil1	-	Digital Filter Time Setting Register: OVV Control register: [OVVCR]<OVVCNT[4:0]> = 0x0F VECLK = 60 MHz	3.8	4.0	4.2	μs
Digital filtering time 4	Tclfil4	-	Digital Filter Time Setting Register: OVV Control register: [OVVCR]<OVVCNT[4:0]> = 0x06 VECLK = 60 MHz	1.52	1.6	1.68	μs
Digital filtering time 2	Tclfil2	-	Digital Filter Time Setting Register: [CLCMPDFSR]<CLCMPDFS>=1 32 counts at 10 MHz	3.04	3.2	3.36	μs
Digital filtering time 3	Tclfil3	-	Digital Filter Time Setting Register: [CLCMPDFSR]<CLCMPDFS>=0 16 counts at 10 MHz	1.52	1.6	1.68	μs

Note: Digital filtering time 1 and 4 is a characteristic of a digital filter located on a different path from the one with digital filtering time 2 and digital filtering time 3.
The digital filter with digital filtering time 1 and 4 can be disabled via a special function register.

10.13. Overcurrent Detection Comparator (OCCMP)

Vbat=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Voltage threshold 1 for overcurrent detection	Voc1	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 00000 Minimum setting	VCC×32/ 64 -0.039	2.500	VCC×32/ 64 +0.039	mV
Voltage threshold 2 for overcurrent detection	Voc2	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 00001	VCC×33/ 64 -0.039	2.578	VCC×33/ 64 +0.039	V
Voltage threshold 3 for overcurrent detection	Voc3	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 00011	VCC×35/ 64 -0.039	2.734	VCC×35/ 64 +0.039	V
Voltage threshold 4 for overcurrent detection	Voc4	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 00111	VCC×39/ 64 -0.039	3.047	VCC×39/ 64 +0.039	V
Voltage threshold 5 for overcurrent detection	Voc5	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 01111 Maximum setting	VCC×47/ 64 -0.039	3.672	VCC×47/ 64 +0.039	V
Voltage threshold 6 for overcurrent detection	Voc6	-	Current-Limit Threshold Setting Register: [OCCMPSR]<OCCMPTV> = 11111 Maximum setting	VCC×63/ 64 -0.039	4.922	VCC×63/ 64 +0.039	V
Digital filtering time 2	Tocfil2	-	Digital Filter Time Setting Register: [OCCMPDFSR]<OCCMPDFS> = 11 64 counts at 10 MHz	6.08	6.4	6.72	µs
Digital filtering time 3	Tocfil3	-	Digital Filter Time Setting Register: [OCCMPDFSR]<OCCMPDFS> = 00 16 counts at 10 MHz	1.52	1.6	1.68	µs

10.14. Back-EMF Comparator (BEMFCMP)

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Input offset voltage 1	Voffset1	U, V, W	When U-phase measurement: V=W=0 V When V-phase measurement: U=W=0 V When W-phase measurement: U=V= 0 V	-80	-	80	mV
Input offset voltage 21	Voffset21	U, V, W	When measuring U: V = 6 V, W = 0 V Comparator output transitions from Lo to High Measure U-phase voltage − 3 V When measuring V: U = 0 V, W = 6 V Comparator output transitions from Lo to High Measure V-phase voltage − 3 V When measuring W: U = 6 V, V = 0 V Comparator output transitions from Lo to High Measure W-phase voltage − 3 V	-75	-	75	mV
Input offset voltage 22	Voffset22	U, V, W	When measuring U: V = 12 V, W = 0 V Comparator output transitions from Lo to High Measure U-phase voltage − 6 V When measuring V: U = 0 V, W = 12 V Comparator output transitions from Lo to High Measure V-phase voltage − 6 V When measuring W: U = 12 V, V = 0 V Comparator output transitions from Lo to High Measure W-phase voltage − 6 V	-50	-	50	mV
Input offset voltage 23	Voffset23	U, V, W	When measuring U: V = 18 V, W = 0 V Comparator output transitions from Lo to High Measure U-phase voltage − 9 V When measuring V: U = 0 V, W = 18 V Comparator output transitions from Lo to High Measure V-phase voltage − 9 V When measuring W: U = 18 V, V = 0 V Comparator output transitions from Lo to High Measure W-phase voltage − 9 V	-75	-	75	mv
BEMFCMP filtering time	Tbemffil	-	Input Processing Control register: [INPCR]<FILVAL[6:0]> = 0x3C VECLK = 60 MHz	0.95	1	1.05	μs

10.15. Thermal Shutdown (TSD) Circuit

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
TSD detection temperature	Ttsd	-	Guaranteed by design	175	190	205	°C
TSD recovery temperature	Ttsdr	-	Guaranteed by design	145	160	175	°C

Note:
- TSD is not tested in a pre-shipment test. Only an evaluation is performed.
- The TSD circuits for the 5-volt regulator (LDO5V) and the LINPHY have the same electrical characteristics.

10.16. LIN

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Supply voltage range	V_{VB}	VBAT	ECU operating voltage range (ISO 17987-4 Param 9, SAE J2602-1)	8.0	-	18.0	V
Supply voltage range	V_{SUP}	VBAT	Note: ISO 17987-4 Param 10 and SAE J2602-1 of LIN configuration is defined 7.0V(min), IC requires 6.0V(min) on 5V regulator.	6.0	-	18.0	V
Supply voltage MAX Ratings	$V_{SUP\_NON\_OP}$	VBAT	Voltage range with in which the device is not destroyed. An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation. (ISO 17987-4 Param 11, SAE J2602-1)	-0.3	-	40	V
BUS MAX Ratings	$V_{BUS\_MAX\_RATING}$	LIN	Voltage range with in which the device is not destroyed. (ISO 17987-4 Param 82) An optional time limit for the maximum value shall be at least 400 ms. No guarantee of correct operation.	-27	-	40	V
Receiver threshold voltage, recessive to dominant edge	V_{th_rec}	LIN	Low Voltage: Recessive Input Threshold (SAE J2602-1)	0.4	-	0.53	V_{SUP}
Receiver threshold voltage, dominant to recessive edge	V_{th_dom}	LIN	High Voltage: Dominant Input Threshold (SAE J2602-1)	0.47	-	0.6	V_{SUP}
BUS current limitation	I_{BUS_LIM}	LIN	Current Limitation for Driver dominant state driver on VBUS = VBAT_max (ISO 17987-4 Param 12)	40	-	200	mA
Leakage current (dominant)	$I_{BUS\_PAS\_dom}$	LIN	Input leakage current at the receiver incl. responder Pull Up resistance as specified in ISO 17987-4 Param 26 driver of VBUS = 0 V VBAT = 12 V (ISO 17987-4 Param 13)	-1	-	-	mA
Leakage current (recessive)	$I_{BUS\_PAS\_rec}$	LIN	Driver off 8 V < VBAT < 18 V, 8 V < VBUS < 18 V, VBUS > VBAT (ISO 17987-4 Param 14)	-	-	20	μA
Leakage current1	$I_{BUS\_NO\_GND}$	LIN	Control unit disconnected from ground GNDDevice = VSUP 0 V < VBUS < 18 V VBAT = 12 V Loss of local ground shall not affect communication in the residual network. (ISO 17987-4 Param 15)	-1	-	1	mA
Leakage current2	$I_{BUS\_NO\_BAT}$	LIN	VBAT disconnected VSUP = GND 0 V < VBUS < 18 V Node shall sustain the current that can flow under this condition. Bus shall remain operational under this condition. (ISO 17987-4 Param 16 and SAE J2602-1)	-	-	23	μA
Voltage of Receiver dominant state	V_{BUS_dom}	LIN	Receiver dominant state (ISO 17987-4 Param 17) Note: ISO 17987-4 Param 17 of LINPHY configuration is not defined as minimum voltage.	-27	-	0.4× VBAT	V

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Voltage of Receiver recessive state	V_{BUS_rec}	LIN	Receiver recessive state (ISO 17987-4 Param 18)	0.6	-	-	V_{SUP}
Receiver center voltage	V_{BUS_CNT}	LIN	VBUS_CNT = (Vth_dom + Vth_rec)/2 (ISO 17987-4 Param 19)	0.475	-	0.525	V_{SUP}
Receiver hysteresis	V_{HYS}	LIN	VHYS = Vth_rec–Vth_dom (ISO 17987-4 Param 20 and SAE J2602-1)	0.07	-	0.175	V_{SUP}
Duty cycle D1 (for worst case at 20 kbps)	D1	LIN	THRec(max) =0,744 × VSUP; THDom(max) =0,581 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 50 µs; D1 = tBus_rec(min)/(2 × tBIT) (ISO 17987-4 Param 27) <PHYFBRM>=0	0.396	-	-	-
Duty cycle D2 (for worst case at 20 kbps)	D2	LIN	THRec(min) =0,422 × VSUP; THDom(min) =0,284 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 50 µs; D2 = tBus_rec(max)/(2 × tBIT) (ISO 17987-4 Param 28) <PHYFBRM>=0	-	-	0.581	-
Duty cycle D3 (for worst case at 10 kbps)	D3	LIN	THRec(max) =0,778 × VSUP; THDom(max) =0,616 × VSUP; VSUP = 7,0 V to 18 V; tBIT = 96 µs; D3 = tBus_rec(min)/(2 × tBIT) (ISO 17987-4 Param 29) <PHYFBRM>=0	0.417	-	-	-
Duty cycle D4 (for worst case at 10 kbps)	D4	LIN	THRec(min) =0,389 × VSUP; THDom(min) =0,251 × VSUP; VSUP = 7,6 V to 18 V; tBIT = 96 µs; D4 = tBus_rec(max)/(2 × tBIT) (ISO 17987-4 Param 30) <PHYFBRM>=0	-	-	0.59	-
Propagation delay	t_{rx_pd}	LIN	Propagation delay of receiver ・ (ISO 17987-4 Param 31) ・ bus dominant to RxD LOW(t_{rx_pdf}) ・ bus recessive to RxD HIGH(t_{rx_pdr}) (See Figure 10.16.1)	-	-	6	µs
Receiver delay symmetry	t_{rx_sym}	LIN	Symmetry of receiver propagation delay rising edge with respect to falling edge (ISO 17987-4 Param 32) $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdf}$	-2	-	2	µs
Bus pull-up resistance1	$R_{RESPONDER}$	LIN	internal resistance (ISO 17987-4 Param 26, SAE J2602-1)	20	30	60	kΩ
Bus pull-up resistance2	$R_{COMMANDER}$	LIN	The serial diode is mandatory. Only for valid for transceiver with integrated commander Pull Up resistance. (ISO 17987-4 Param 25, SAE J2602-1) external resistance	900	-	1100	Ω
LIN input capacity (Guaranteed by design)	$C_{RESPONDER}$	LIN	Capacitance of responder node (ISO 17987-4 Param 37) 250pF -220pF = 30pF max	-	-	30	pF
Current consumption in sleep mode (Guaranteed by design)	I_{sleep_LIN}	VBAT	VBAT=12V, RT=25°C, Only working LIN bus Wakeup signal Only LINPHY current consumption at [PMUSCR]<LIN_MODE>=0(Sleep Operate Mode)	-	-	3	µA

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Dominant time for bus wakeup	t_{WAKE}	LIN	Wakeup pulse width from LIN bus (See Figure 10.16.2)	30	-	150	μs
Turn off time to standby	t_{sleep}	-	Turn off time from Active to Standby mode	-	-	1	ms
Wake-up threshold voltage	V_{BUSwk}	LIN	Threshold voltage for Wakeup signal detection	0.4	0.5	0.6	V_{SUP}
ESD Susceptibility HBM1 pins LIN vs. LINGND	V_{ESDLIN}	LIN	IEC61000-4-2 Conducted HBM	-6	-	6	kV
ESD Susceptibility HBM3 pins LIN vs. LINGND	$V_{ESDLIN3}$		AEC-Q100-002	-6	-	6	kV

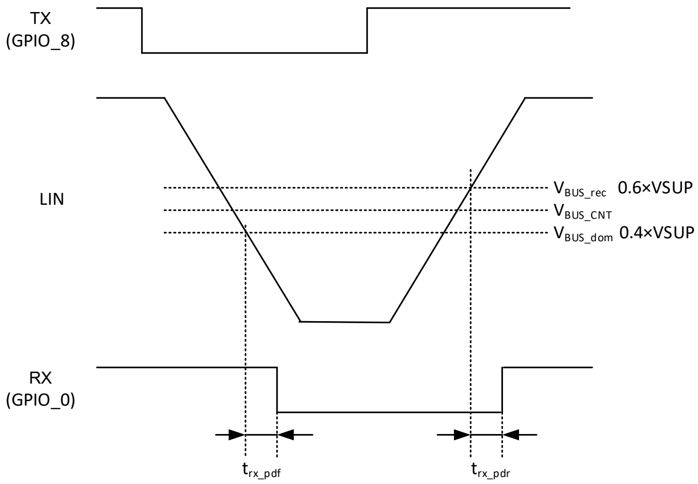


Figure 10.16.1 Measurement of LIN Propagation delay

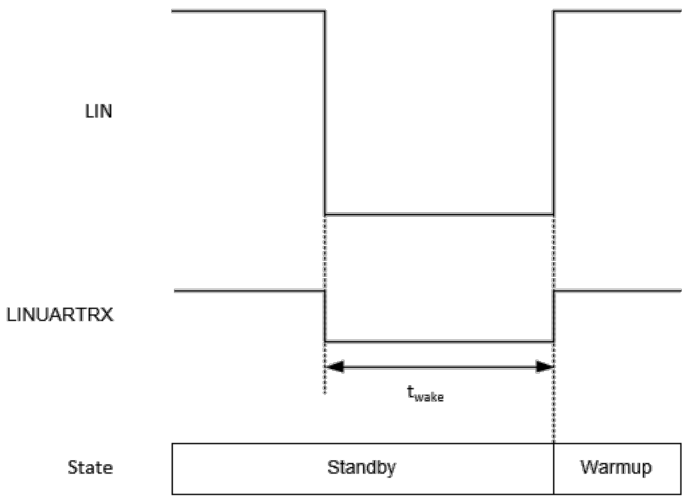


Figure 10.16.2 Measurement of LIN Dominant time for bus Wakeup

10.17. UART

VBAT=6 to 18V, VCC=4.8 to 5.2V, VDD=1.45 to 1.55V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Data rate	Fuart	UART_RX, UART_TX	-	-	-	1	Mbps

10.18. SPI

VBAT=6 to 18V, VCC=4.8 to 5.2V, VDD=1.45 to 1.55V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
SCLK period (Controller)	Tm	SCLK	(See Figure 10.18.1, Figure 10.18.2)	T×m ≥250 ns	-	-	ns
SCLK period (Target)	Ts		(See Figure 10.18.3, Figure 0.18.4)	T×n ≥1 μs	-	-	ns
SCLK Low-level pulse width in Controller mode	Twlm		(See Figure 10.18.1, Figure 10.18.2)	0.4	-	0.6	Tm
SCLK High-level pulse width in Controller mode	Twhm		(See Figure 10.18.1, Figure 10.18.2)	0.4	-	0.6	Tm
SCLK Low-level pulse width in Target mode	Twls		(See Figure 10.18.3, Figure 10.18.4)	0.4	-	0.6	Ts
SCLK High-level pulse width in Target mode	Twhs		(See Figure 10.18.3, Figure 10.18.4)	0.4	-	0.6	Ts
SCLK rise/fall to SDO valid in Controller mode	Todsm		(See Figure 10.18.1, Figure 10.18.2)	-	-	50	ns
SCLK rise/fall to SDO hold in Controller mode	Todhm		(See Figure 10.18.1, Figure 10.18.2)	-20	-	-	ns
SCLK rise/fall to SDI valid in Controller mode	Tidsm		(See Figure 10.18.1, Figure 10.18.2)	55	-	-	ns
SDI hold time from SCLK rise/fall in Controller mode	Tidhm		(See Figure 10.18.1, Figure 10.18.2)	100	-	-	ns
CSN valid to SCLK rise/fall in Controller mode	Tofsm	CSN SCLK	(See Figure 10.18.1, Figure 10.18.2)	T×m -50	-	-	ns

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
SCLK rise/fall to SDO valid in Target mode	Todss	SCLK	(See Figure 10.18.3, Figure 10.18.4)	-	-	3T+90	ns
SCLK rise/fall to SDO hold in Target mode	Todhs		(See Figure 10.18.3, Figure 10.18.4)	2T	-	-	ns
SCLK rise/fall to SDI valid in Target mode	Tidss		(See Figure 10.18.3, Figure 10.18.4)	10	-	-	ns
SCLK rise/fall edge to SDI hold in Target mode	Tidhs		(See Figure 10.18.3, Figure 10.18.4)	3T+20	-	-	ns
CSN valid to SCLK rise/fall in Target mode	Tifss	CSN SCLK	(See Figure 10.18.3, Figure 10.18.4)	T×n -20	-	-	ns
SCLK rise/fall to CSN deasserted in Controller mode	Tofhm		(See Figure 10.18.1, Figure 10.18.2)	T×m -50	-	-	ns
SCLK rise/fall to CSN deasserted in Target mode	Tifhs		(See Figure 10.18.3, Figure 10.18.4)	T×n -20	-	-	ns

Note:
- Load capacitance, CL = 100 pF
- [GPOPSR]< GPIOPSx>=11 (6mA setting)
- The electric character of Section 10.18 is Guaranteed by design.
- T represents the SSPCLK period (e.g., 25 ns at 40 MHz).
- n represents a ratio of the SCLK period to the SSPCLK period (n ≥ 12).
- m represents the ratio of the SCLK period to the SSPCLK period (65024 ≥ m ≥ 12).

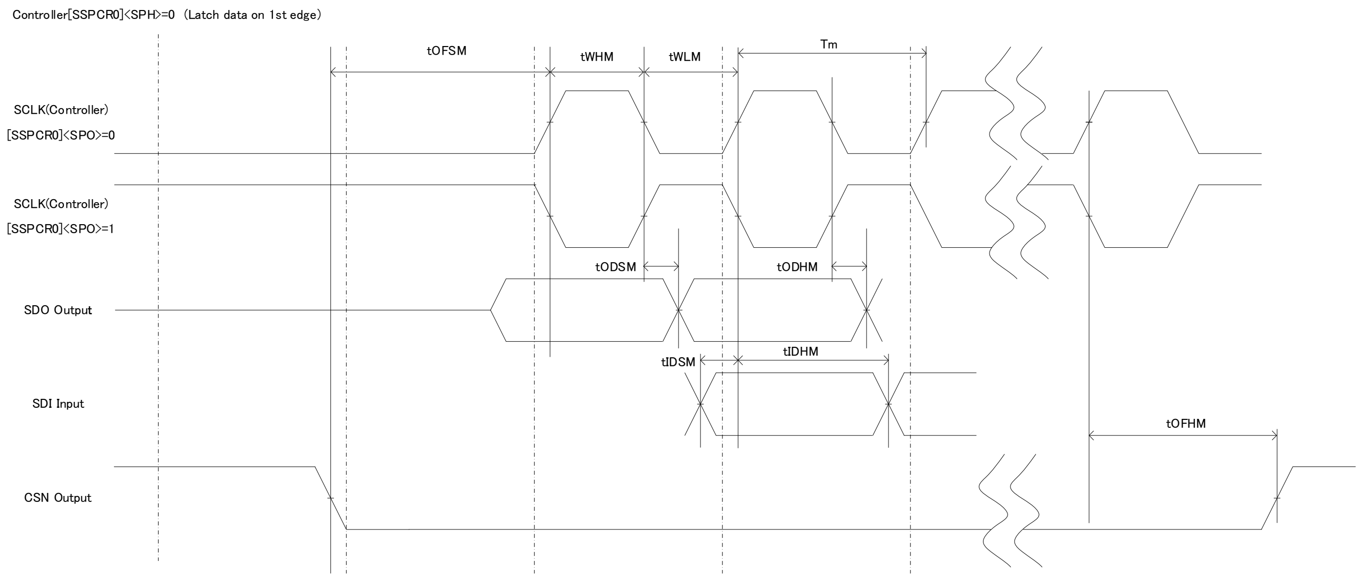


Figure 10.18.1 SPI Communication Waveform 1

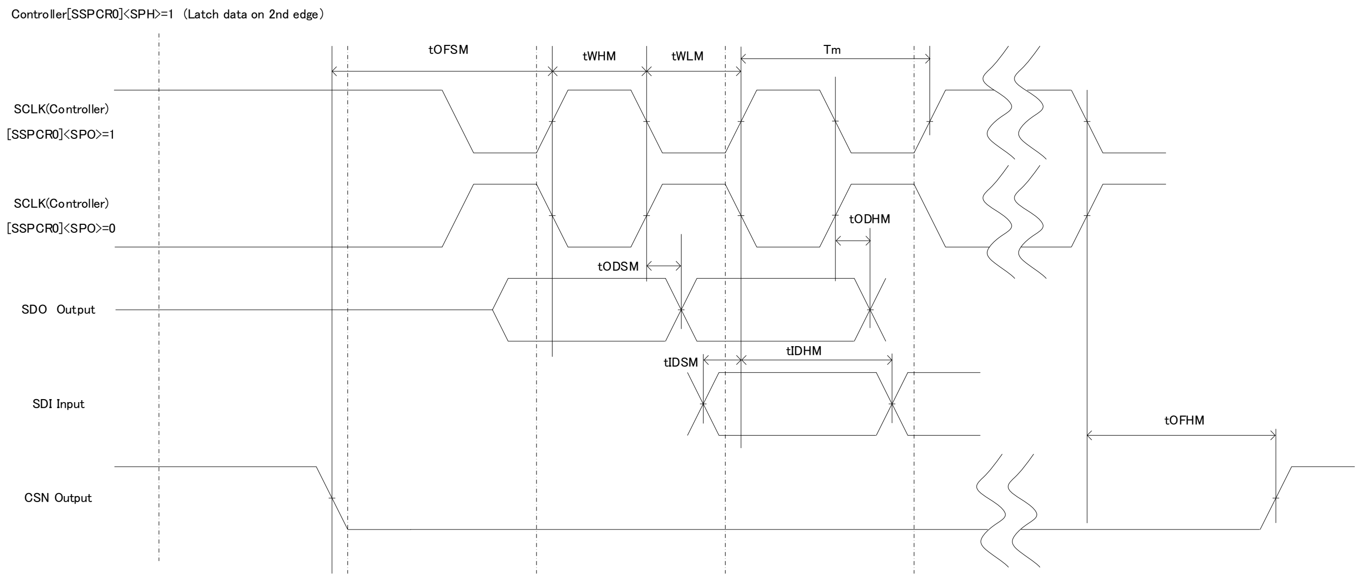


Figure 10.18.2 SPI Communication Waveform 2

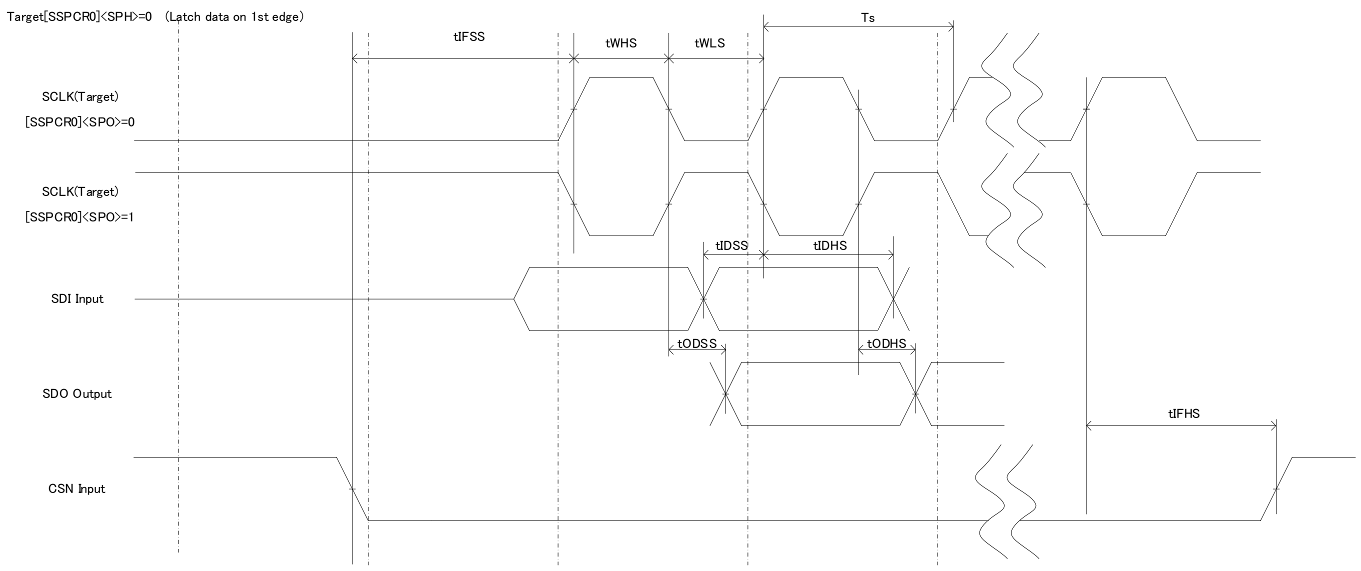


Figure 10.18.3 SPI Communication Waveform 3

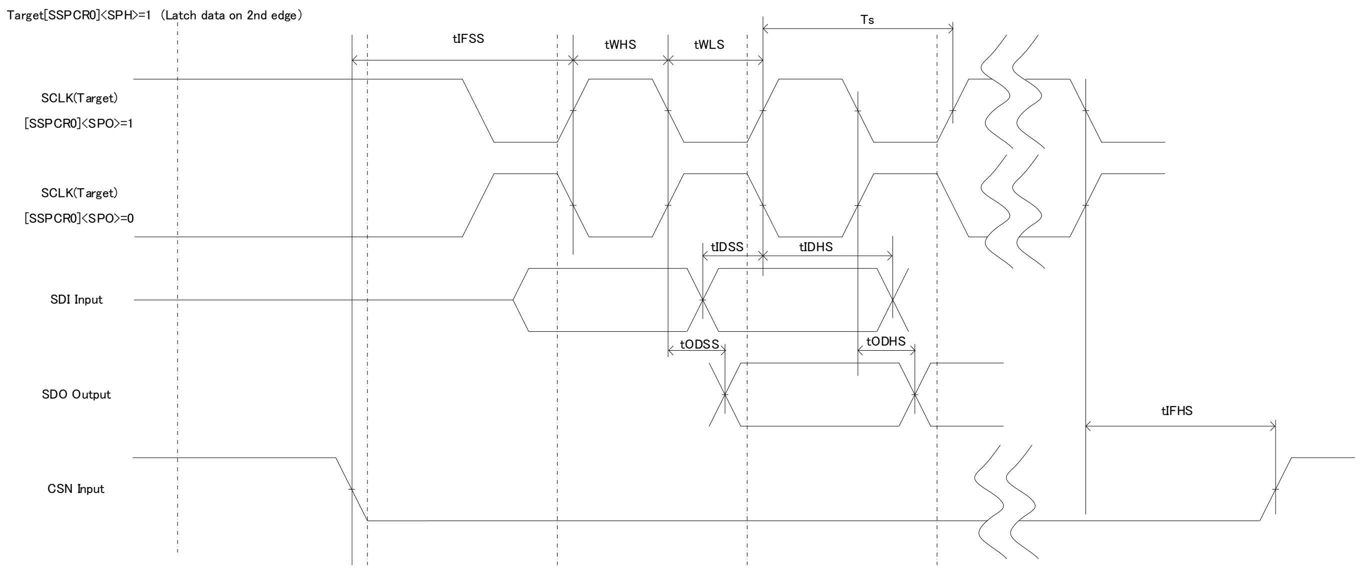


Figure 10.18.4 SPI Communication Waveform 4

10.19. GPIO

VBAT=6 to 18V, VCC=4.8 to 5.2V, VDD=1.45 to 1.55V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
High-level input threshold voltage	Vinh	GPIO_x	-	VCC×0.75	-	-	V
Low-level input threshold voltage	Vinl		-	-	-	VCC ×0.25	V
Pull-up resistor	Rpullup		-	30	50	100	kΩ
Pull-down resistor	Rpulldown		-	30	50	100	kΩ
High-level output voltage	Vouth		Load condition: [GPOPSR]<GPIOPSx>=00: -1mA [GPOPSR]<GPIOPSx>=01: -2mA [GPOPSR]<GPIOPSx>=10: -4mA [GPOPSR]<GPIOPSx>=11: -6mA	VCC×0.8	-	-	V
Low-level output voltage	Voutl		Load condition: [GPOPSR]<GPIOPSx>=00: 1mA [GPOPSR]<GPIOPSx>=01: 2mA [GPOPSR]<GPIOPSx>=10: 4mA [GPOPSR]<GPIOPSx>=11: 6mA	-	-	0.5	V

10.20. Flash (Code Flash)

VBAT=6 to 18V, VCC=4.8 to 5.2V, VDD=1.45 to 1.55V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Conditions	Values			Unit
				Min	Typ.	Max	
Bus frequency	-	-	-	-	-	42	MHz
Read frequency	-	-	-	-	-	10.5	MHz
Data retention time 1	-	-	Tj=85°C, after 1,000 program/erase cycles	40	-	-	years
Data retention time 2	-	-	Tj = 85°C, after 30k program/erase cycles (Rear 16KBytes of 80KBytes: 0x0001_0000 to 0x0001_3FFF)	5	-	-	years
Flash capacity	-	-	-	-	80	-	KBytes
Data access size	-	-	Same as read/write operations	-	Word (32 bits)	-	-
Erase time	-	-	80KBytes, Tj = -40 to 150°C	-	100	-	ms
Program time	-	-	Tj = -40 to 150°C	-	2.5	-	s
Erase block size	-	-	-	-	8	-	KBytes
Erase block time	-	-	1 block (8KBytes), Tj = -40 to 150°C	-	6.8	7.2	ms
Program block size	-	-	-	-	128	-	Bytes
Program block time	-	-	128Bytes, Tj = -40 to 150°C	-	2.4	2.6	ms

Note: It is necessary to set the number of wait cycles for read access according to the bus frequency.

10.21. Other

VBAT=6 to 18V, VCC=4.8 to 5.2V, VDD=1.45 to 1.55V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
High-level input threshold voltage	Vmdinh	MD0 MD1	-	VCC ×0.75	-	-	V
Low-level input threshold voltage	Vmdinl		-	-	-	VCC ×0.25	V
Pull-down resistor	Rmdpd		-	30	50	100	kΩ

11. Application Circuit Example

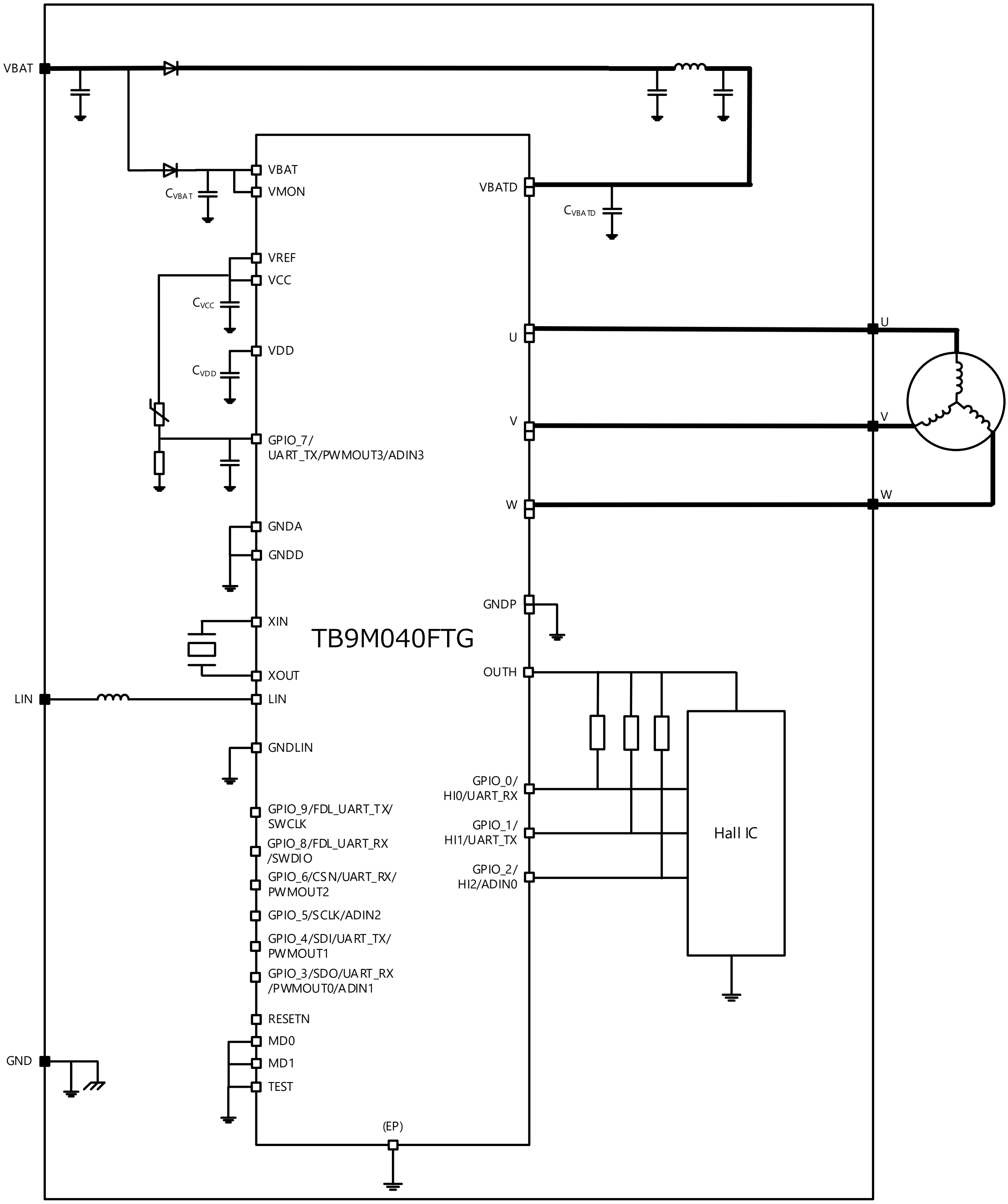


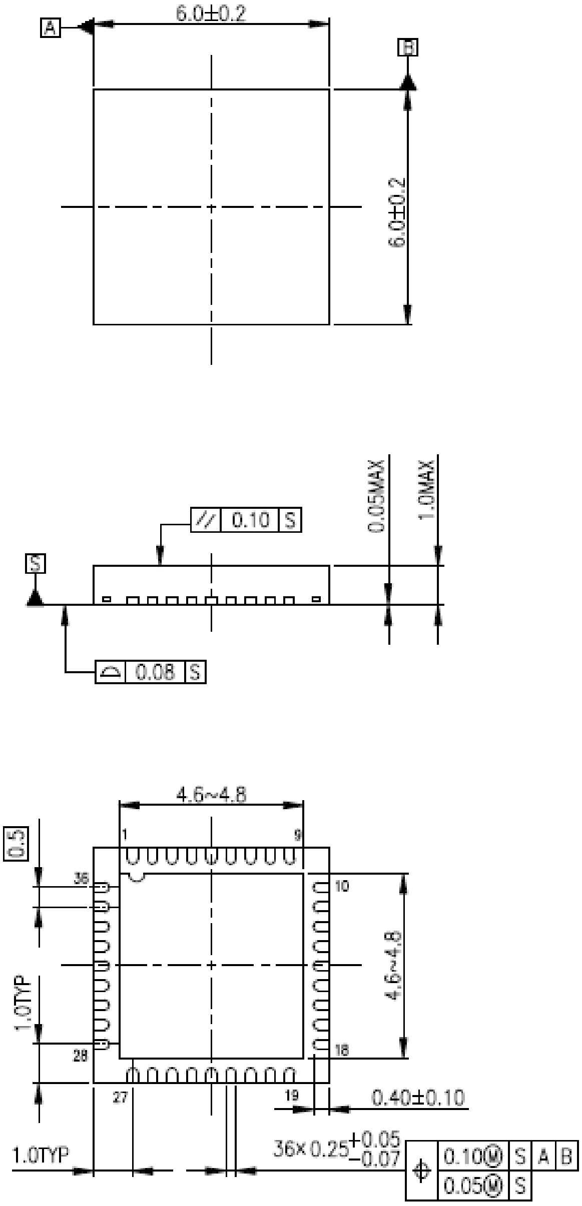
Figure 11.1 Application Circuit Example

12. Package Information

12.1. Package Dimensions

P-VQFN36-0606-0.50-004

Unit:mm



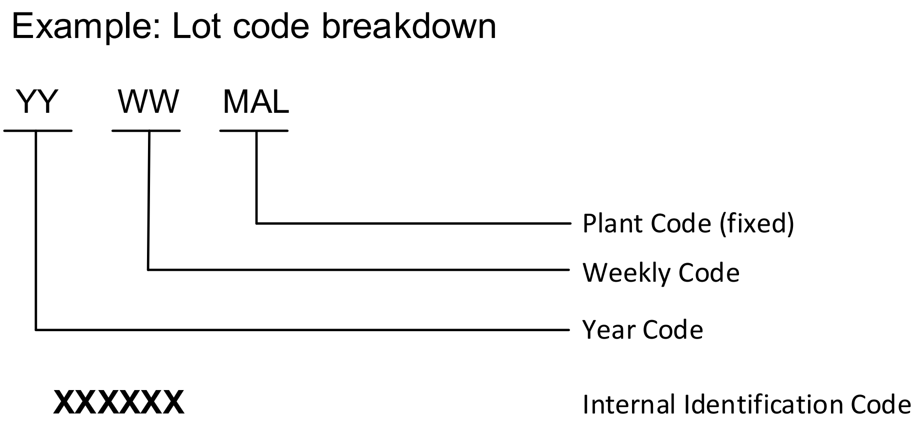
Weight: 0.102g (typ.)

Figure 12.1 Package Dimensions

12.2. Marking

Product name: TB9M040FTG

Figure 12.2 Marking



13. IC Usage Considerations

13.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

13.2. Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

RESTRICTIONS ON PRODUCT USE

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