SiC MOSFET (TOLL Package) Half-bridge Board

Design Guide

RD262-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

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1. Introduction

This design guide describes the design overview of each circuit block of the SiC MOSFET (TOLL package) Half-bridge Board (hereafter referred to as “this design”).

This design is a half-bridge board equipped with two SiC MOSFETs. Two types of boards were developed, each mounting 650V SiC MOSFETs. As shown in Figure. 1.1, this design can be connected to the Power Daughter Card Interface (board socket) of the Half-Bridge Motherboard of the SpeedVal Kit™ provided by Wolfspeed. By inserting this design into the Half-Bridge Motherboard, evaluation of our latest SiC MOSFETs can be performed conveniently. In this design, characteristic evaluation was conducted using a boost DC-DC converter configuration assuming PFC applications.

In this design, the same device is mounted on both the high-side and low-side positions for each of the TW027U65C and TW048U65C boards. By replacing the board, SiC MOSFETs with different specifications can be evaluated under the same evaluation conditions.

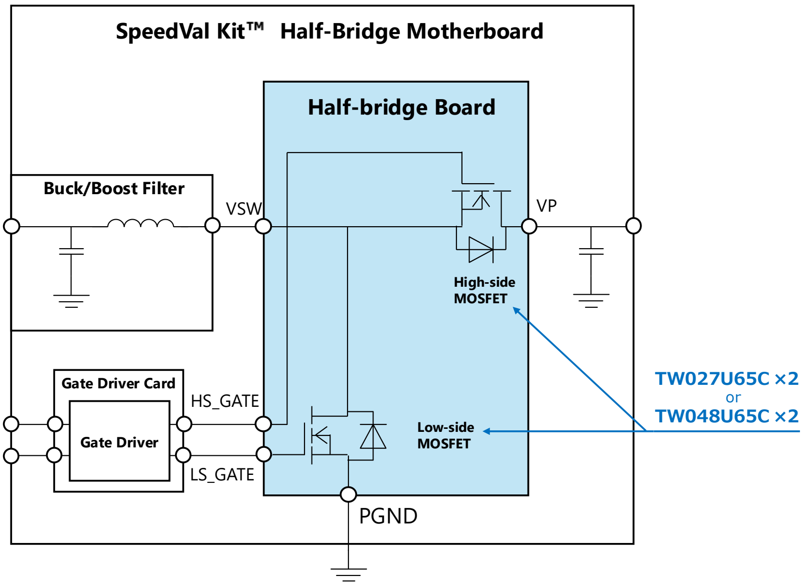


Fig. 1.1 Example of Usage of This Design

2. Board Specifications

The appearance of this design is shown in Fig. 2.1, and the board specifications are listed in Table 2.1. The area highlighted by the red frame indicates the card edge, which can be connected to the Power Daughter Card Interface (board socket) of the SpeedVal Kit™ Half-Bridge Motherboard.

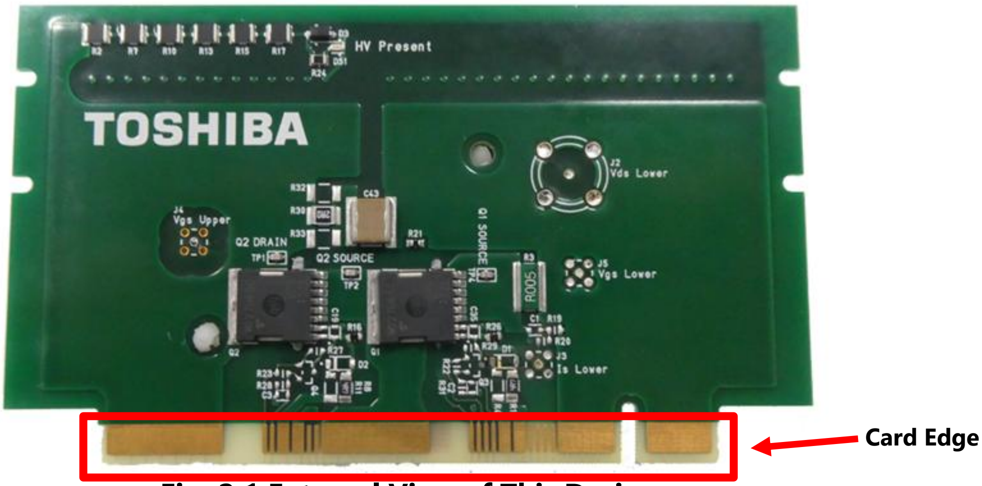


Fig. 2.1 External View of This Design

External dimensions: 110 × 65 × 30mm
(including rear-side heat sink)

Table 2.1 Board Specifications

Board Name	TW027U65C-Mounted Board	TW048U65C-Mounted Board
Mounted Device	TW027U65C	TW048U65C
Substrate Structure	FR-4, 4-Layers (through-hole via), t1.6mm Cu Thickness 155µm (outer layers), 140µm (inner layers)	
Functions	Miller Clamp (High-side / Low-side) Thermistor for Board Temperature Measurement	

3. Main Components

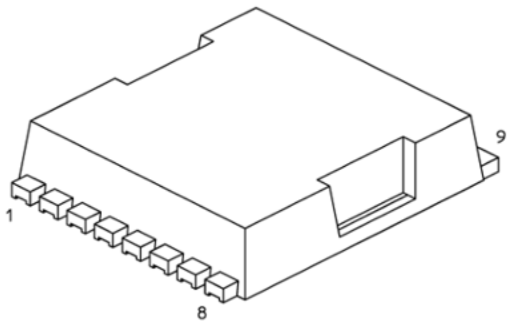
This chapter describes the components used in this design.
In this design, two types of half-bridge boards are developed, one populated with two TW027U65C devices and the other populated with two TW048U65C devices. On each half-bridge board, the same device is mounted on both the high-side and low-side positions.

3.1. SiC MOSFET TW027U65C

The 650V-rated SiC MOSFET TW027U65C is used as the switching device of the half-bridge board. The main features of the TW027U65C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 27mΩ (typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V (V_{DS} = 10V, I_D = 3mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout



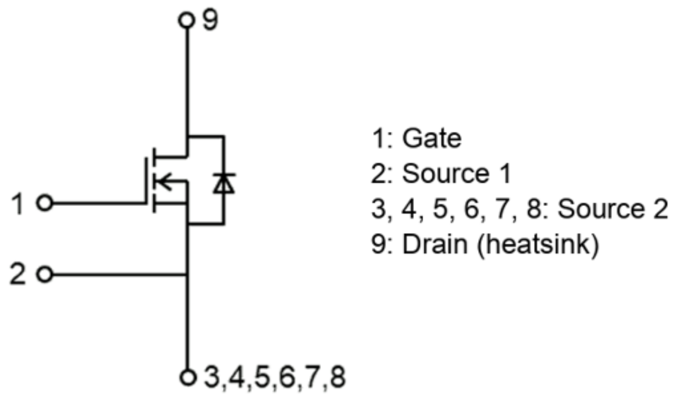


Fig. 3.1 Appearance and Terminal Layout of TW027U65C

3.2. SiC MOSFET TW048U65C

The 650V-rated SiC MOSFET TW048U65C is used as the switching device of the half-bridge board. The main features of the TW048U65C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 48mΩ (typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V (V_{DS} = 10V, I_D = 1.6mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout

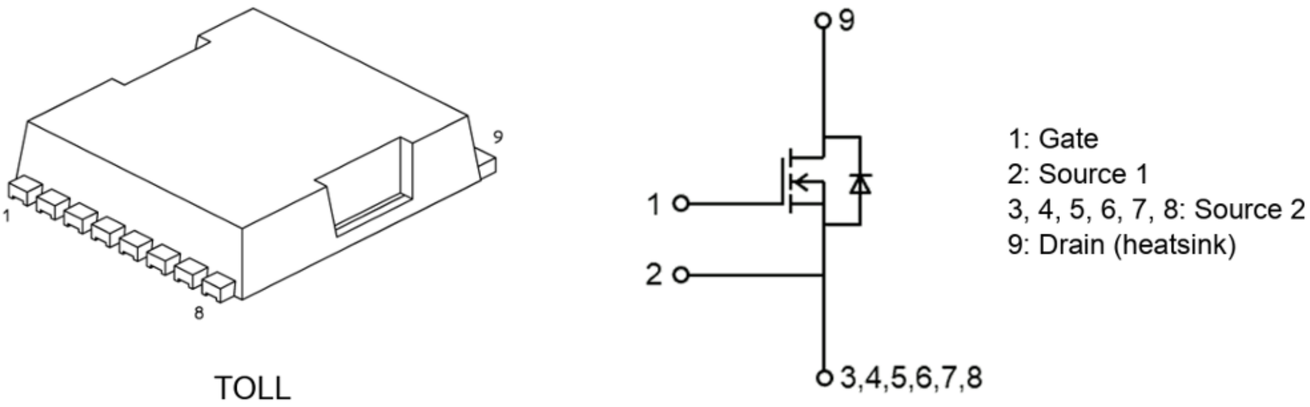


Fig. 3.2 Appearance and Terminal Layout of TW048U65C

4. Circuit Design

This chapter describes the points of circuit design of this design.

4.1. Gate Drive Circuit

Fig. 4.1 shows the gate drive circuit for the low-side SiC MOSFET (Q1).

The design of the gate drive circuit affects both power supply efficiency and EMI noise. In general, there is a trade-off between efficiency and EMI, so a balanced design approach is required. To tune EMI, adjust the value of the gate series resistor R1 and verify the results. The MOSFET turn-on speed is determined by R1. During turn-on, diode D1 bypasses R4, therefore R4 does not affect the turn-on speed. The turn-off speed is determined by the equivalent resistance of R1 in parallel with R4. To change only the turn-on speed, adjust R1. To change only the turn-off speed, adjust R4. Note that increasing gate resistance slows the MOSFET switching speed and may reduce power supply efficiency. In this design, R1 is populated with 4.7 Ω, while D1 and R4 are not populated. If independent adjustment of turn-on and turn-off is required, populate D1 and R4 and tune the resistor values while monitoring the actual waveforms.

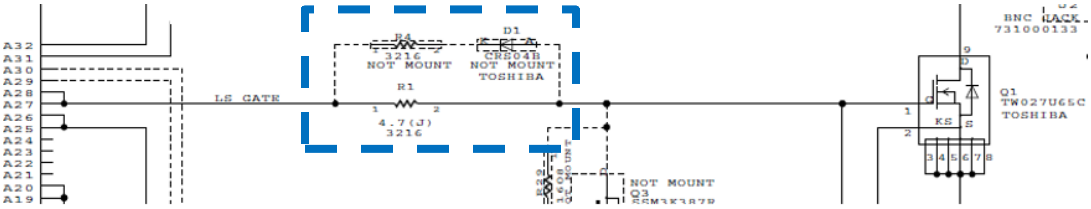


Fig. 4.1 Gate Drive Circuit (Q1)

4.2. Miller Clamp Circuit

Fig. 4.2 shows the Miller clamp circuit for the low-side SiC MOSFET (Q1).

The Miller clamp circuit is used to prevent false turn-on (self turn-on) of the gate caused by the Miller capacitance.] When Q1 in the half-bridge is in the off state, turning on the Miller-clamp MOSFET (Q3) prevents the current flowing through the Miller capacitance from flowing into the gate resistor of Q1. This suppresses a rise in the gate voltage and helps prevent self turn-on. When using a gate driver that supports the Miller clamp function, the Miller clamp function can be enabled by populating the components in the dotted-line area in Fig. 4.2.

Although not described in this guide, an application note that "MOSFET Self-Turn-On Phenomenon" is available. Please refer to it.

In this design, the Miller clamp function is not populated. If the gate driver you use includes an internal MOSFET for Miller clamping, use a 0Ω jumper for R29. If it does not include an internal MOSFET, the Miller clamp function can be implemented by adding MOSFET Q3. As an example, when using MOSFET Q3, use 10kΩ for R22 and a 0Ω jumper for R31.

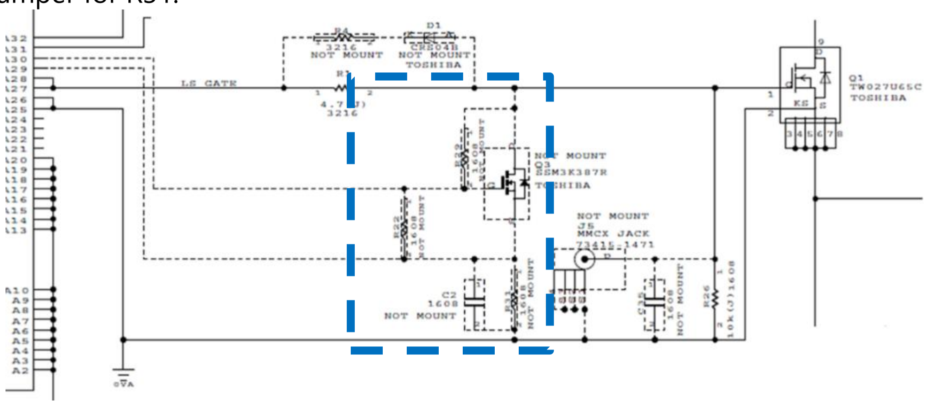


Fig. 4.2 Miller Clamp Circuit

4.3. Current Waveform Measurement Circuit

Fig. 4.3 shows the current waveform measurement circuit.

By placing a shunt resistor R3 on the source side of the low-side MOSFET (Q1) and installing an MMCX jack (Note 1) connector at J3 for waveform observation, the current waveform can be measured. The filter circuit configuration can be adjusted depending on the operating environment. When measuring efficiency, it is recommended to jumper R3 with a 0Ω resistor to reduce power loss.

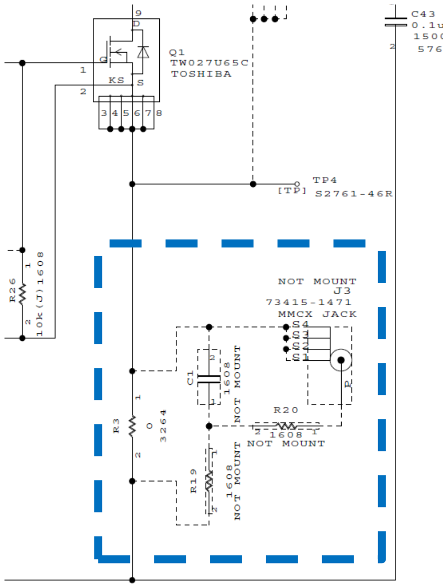


Fig. 4.3 Current Waveform Measurement Circuit

(Note 1) MMCX : Micro-miniature Coaxial Connector

4.4. Waveform Measurement Circuits

In this design, connectors are provided to enable measurement of gate signals and the half-bridge midpoint (VSW) voltage.

As shown in Fig. 4.4, use J4 (MMCX jack) for waveform measurement of the high-side MOSFET (Q2). For waveform measurement of the low-side MOSFET (Q1), use J5 (MMCX jack) in the same manner.

When measuring the waveform of the high-side MOSFET (Q2), note that the reference point differs from other measurement points. Therefore, use an appropriate probe and measurement setup.

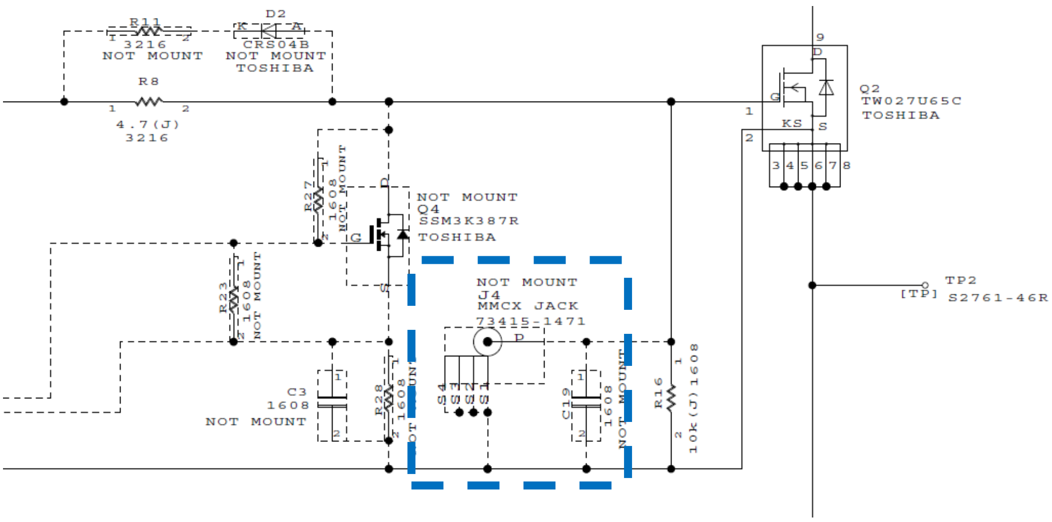


Fig. 4.4 Gate Signal Measurement Circuit

To measure the half-bridge midpoint (VSW) at the source side of the high-side MOSFET (Q2) and the drain side of the low-side MOSFET (Q1), use J2 (BNC jack) as shown in Fig. 4.5.

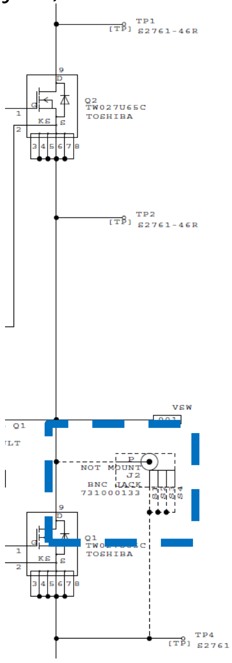


Fig. 4.5 Half-Bridge Midpoint (VSW) Measurement Circuit

4.5. Board Temperature Measurement Circuit

As shown in Fig. 4.6, a thermistor (R21) is used to measure the on-board temperature around the SiC MOSFET in this design. Since it is directly connected to the card edge, the temperature can be monitored at the half-bridge board connection interface.

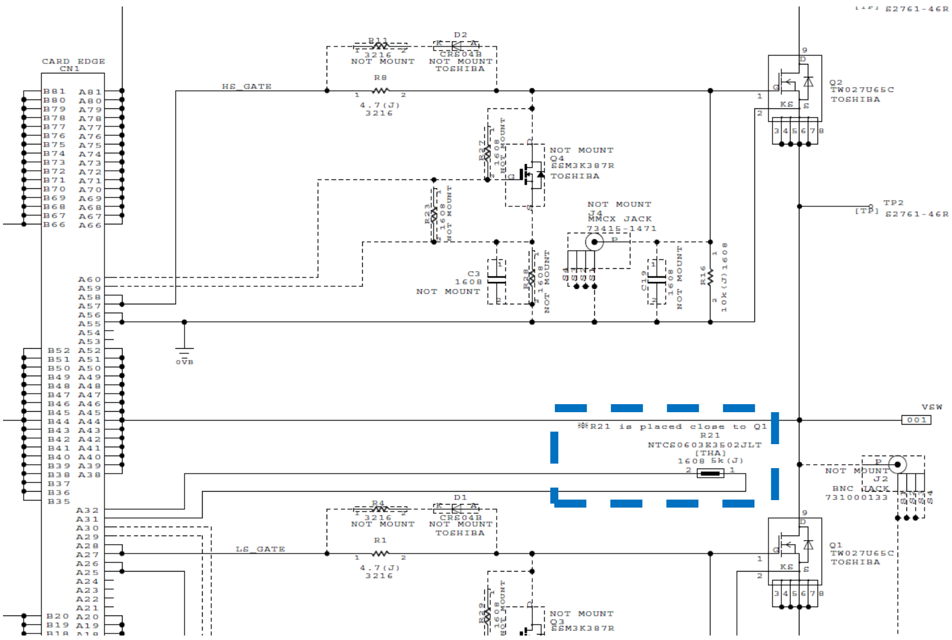


Fig. 4.6 Board Temperature Measurement Circuit

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