

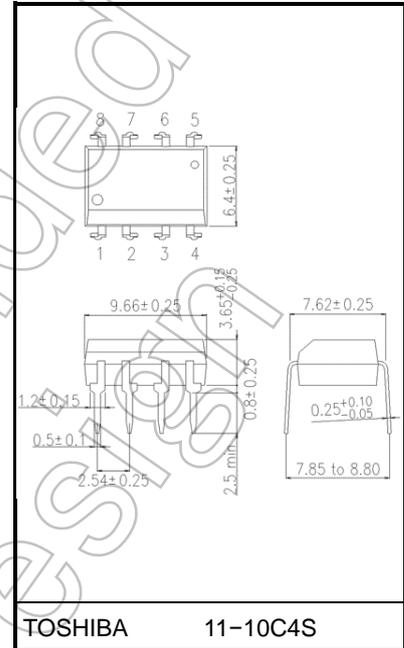
6N138, 6N139

Current Loop Driver
 Low Input Current Line Receiver
 CMOS Logic Interface

Unit: mm

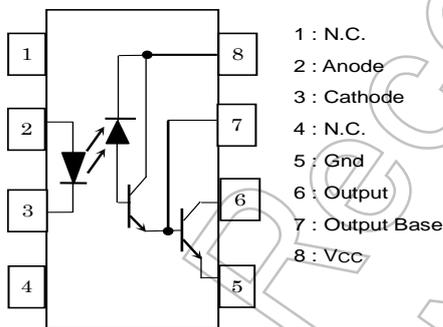
The TOSHIBA 6N138 and 6N139 consists of an infrared emitting diode coupled with a split-Darlington output configuration. A high speed Ired manufactured with an unique LPE junction, has the virtue of fast rise and fall time at low drive current.

- Isolation voltage: 2500 Vrms (min)
- Current transfer ratio
 - : 6N138 – 300% (min) (IF=1.6mA)
 - : 6N139 – 400% (min) (IF=0.5mA)
- Switching time: 6N138 – tPHL = 10μs (max)
 - tPLH = 35μs (max)
 - 6N139 – tPHL = 1μs (max)
 - tPLH = 7μs (max)
- UL-recognized: UL 1577, File No.E67349

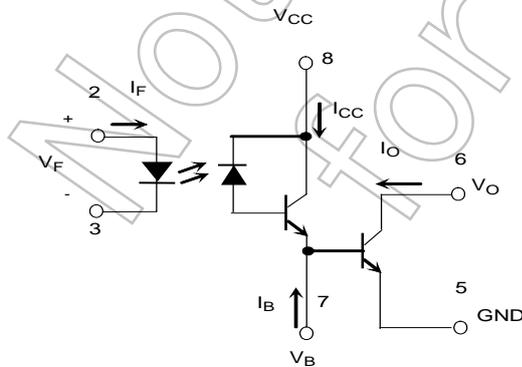


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



Start of commercial production
 1988-02

Absolute Maximum Ratings (*) (Ta = 0°C to + 70°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current (Note 1)	I _F	20	mA
	Pulse forward current	I _{FP} ^(*)	40	mA
	Total pulse forward current	I _{FP} ^(**)	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation (Note 2)	P _D	35	mW
Detector	Output current (Note 3)	I _O	60	mA
	Emitter-base reverse voltage	V _{EB}	0.5	V
	Supply voltage	V _{CC} ^(*)	-0.5 to 18	V
	Output voltage	V _O ^(*)	-0.5 to 18	V
	Output power dissipation (Note 4)	P _O	100	mW
Operating temperature range		T _{opr}	0 to 70	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead solder temperature (10s) ^(*)		T _{sol}	260	°C
Isolation voltage (60s, R.H. ≤ 60%)		BV _S ^(**)	2500	V _{rms}
			3540	V _{dc}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

(*) JEDEC registered data

(**) Not registered JEDEC

(*1) 50 % duty cycle, 1 ms pulse width

(*2) Pulse width 1 μs, 300 pps

(*3) 6N138... -0.5 to 7 V

(*4) 1.6 mm below seating plane

Electrical Characteristics

Over Recommended Temperature ($T_a = 0^\circ\text{C}$ to 70°C , unless otherwise noted)

Characteristics		Symbol	Test Condition	Min	(*5)Typ.	Max	Unit
Current transfer ratio (Note 5, 6)	6N139	CTR(*)	$I_F = 0.5 \text{ mA}, V_O = 0.4 \text{ V}$ $V_{CC} = 4.5 \text{ V}$	400	800	—	%
	6N138		$I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}$ $V_{CC} = 4.5 \text{ V}$	500	900	—	
Logic low output voltage (Note 6)	6N139	VOL	$I_F = 1.6 \text{ mA}, I_O = 6.4 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	—	0.1	0.4	V
			$I_F = 5 \text{ mA}, I_O = 15 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	—	0.1	0.4	
			$I_F = 12 \text{ mA}, I_O = 24 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	—	0.2	0.4	
	6N138	$I_F = 1.6 \text{ mA}, I_O = 4.8 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	—	0.1	0.4		
Logic high output current (Note 6)	6N139	IOH(*)	$I_F = 0 \text{ mA}, V_O = V_{CC} = 18 \text{ V}$	—	0.05	100	μA
	6N138		$I_F = 0 \text{ mA}, V_O = V_{CC} = 7 \text{ V}$	—	0.05	250	
Logic low supply current (Note 6)	ICCL		$I_F = 1.6 \text{ mA}, V_O = \text{Open}$ $V_{CC} = 5 \text{ V}$	—	0.2	—	mA
Logic high supply current (Note 6)	ICCH		$I_F = 0 \text{ mA}, V_O = \text{Open}, V_{CC} = 5 \text{ V}$	—	10	—	nA
Input forward voltage	VF(*)		$I_F = 1.6 \text{ mA}, T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Input reverse breakdown voltage	BVR(*)		$I_R = 10 \mu\text{A}, T_a = 25^\circ\text{C}$	5	—	—	V
Temperature coefficient of forward voltage	$\Delta V_F / \Delta T_a$		$I_F = 1.6 \text{ mA}$	—	-1.9	—	$\text{mV} / ^\circ\text{C}$
Input capacitance	CIN		$f = 1 \text{ MHz}, V_F = 0 \text{ V}$	—	60	—	pF
Resistance (input-output)	RI-O		$V_{I-O} = 500 \text{ V}$ $R.H. \leq 60 \%$ (Note 7),	—	10^{12}	—	Ω
Capacitance (input-output)	CI-O		$f = 1 \text{ MHz}, V = 0 \text{ V}$ (Note 7)	—	0.6	—	pF

(**) JEDEC registered data.

(*5) All typical values are at $T_a = 25^\circ\text{C}$ and $V_{CC} = 5 \text{ V}$, unless otherwise noted.

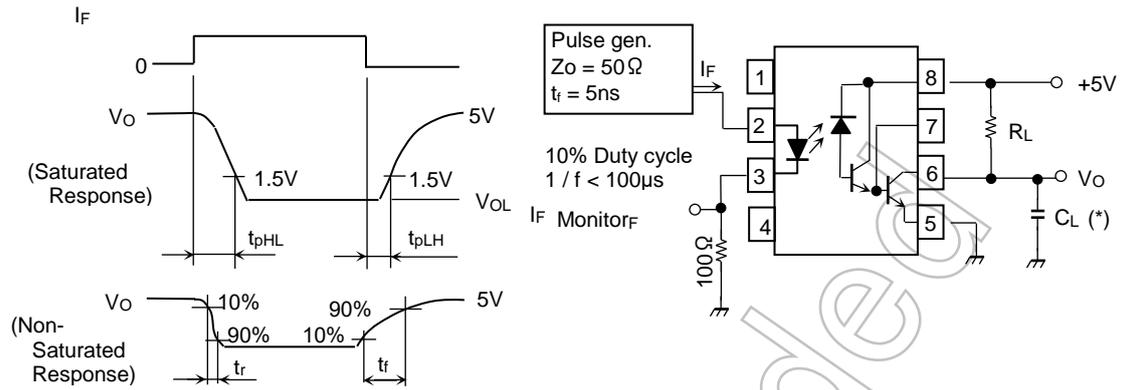
Switching Specifications (Ta=25°C, Vcc=5V, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to logic low at output (Note 6, 8)	6N139	t _{pHL} (*)	1	I _F = 0.5 mA, R _L = 4.7 kΩ	—	5	25	μs
				I _F = 12 mA, R _L = 270 Ω	—	0.2	1	
	6N138			I _F = 1.6 mA, R _L = 2.2 kΩ	—	1	10	
Propagation delay time to logic high at output (Note 6, 8)	6N139	t _{pLH} (*)	1	I _F = 0.5 mA, R _L = 4.7 kΩ	—	5	60	μs
				I _F = 12 mA, R _L = 270 Ω	—	1	7	
	6N138			I _F = 1.6 mA, R _L = 2.2 kΩ	—	4	35	
Common mode transient immunity at logic high level output (Note 9)		CM _H	2	I _F = 0 mA, R _L = 2.2 kΩ V _{CM} = 400 V _{p-p}	—	500	—	V / μs
Common mode transient immunity at logic low level output (Note 9)		CM _L	2	I _F = 1.6 mA R _L = 2.2 kΩ V _{CM} = 400 V _{p-p}	—	-500	—	V / μs

(*)JEDEC registered data.

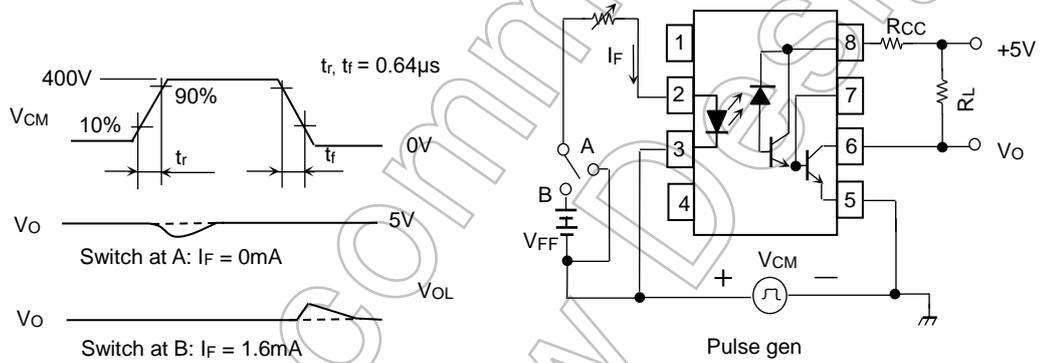
- (Note 1): Derate linearly above 50 °C free-air temperature at a rate of 0.4 mA / °C
- (Note 2): Derate linearly above 50 °C free-air temperature at a rate of 0.7 mW / °C
- (Note 3): Derate linearly above 25 °C free-air temperature at a rate of 0.7 mA / °C
- (Note 4): Derate linearly above 25 °C free-air temperature at a rate of 2.0 mW / °C
- (Note 5): DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100 %.
- (Note 6): Pin 7 open.
- (Note 7): Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
- (Note 8): Use of a resistor between pin 5 and 7 will decrease gain and delay time.
- (Note 9): Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM} / dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a logic high state (i.e. V_O > 2.0 V).
Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} / dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e. V_O < 0.8 V).

Test Circuit 1.



(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 2.



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