Bi-CMOS Linear Integrated Circuit Silicon Monolithic

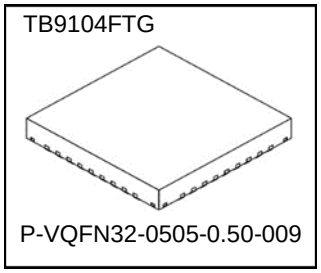
TB9104FTG

Automotive 1channel H-bridge (2channel Half-bridge) Gate Driver

1. Description

The TB9104FTG is a single-channel H-bridge gate driver and a two-channel half-bridge gate driver for automotive applications. When in standby mode, power consumption can be reduced. It is equipped with a charge pump circuit, current sense amplifier, SPI communication circuit, PWM circuit, and various abnormal detection circuits. Motor rotation instructions can be given not only through the pin but also via SPI.

In the event of an abnormal detection, the gate drive will shut down according to preset settings. Additionally, abnormalities will be notified through the DIAG_X terminal, and detailed information will be provided via SPI communication.



Weight: 0.07g (Typ.)

2. Applications

It is suitable for motor control applications such as sliding doors, back doors, seats, windows, and mirrors when used in combination with n-type MOSFETs.

Rotation instructions can also be controlled via SPI, allowing for shared wiring among multiple ICs.

3. Features

- Standby mode: Low power consumption, capable of standby operation.
- Equipped with a charge pump: 2x boost configuration.
- Power supply: Possible to the battery reverse connection prevention circuit.
- Gate driver section: Equipped with two modes: half-bridge mode and H-bridge mode.
  - Half bridge mode: Available in 2 channels.
    - Independently for each channel, manage the high-side and low-side MOSFETs in a time-controlled manner to prevent through current.
  - H bridge mode: Can be used as a single channel by combining half bridges.
    - Manage four n-type MOSFETs to prevent through current.
- Equipped with various anomaly detection features:
  - VCC pin (analog power supply) low voltage detection
  - VB pin (battery) low voltage detection
  - VCP pin (charge pump voltage) high voltage detection, boost under-voltage detection.
  - RPPO pin (power supply for battery reverse connection prevention circuit) abnormal voltage drop detection.
  - SPI anomalies (format anomalies, command violations, etc.)
  - Overheating detection
  - Monitoring the drain-source voltage of the external n-type MOSFET (overcurrent detection)
- Notification from DIAG_X terminal: Upon anomaly detection.
- Built-in motor current sense amplifier circuit:
  - Built-in offset calibration function
- Built-in SPI communication circuit: Drive instructions can also be issued from SPI, built-in PWM waveform generation circuit for H-bridge mode.
- Three power supplies are required: battery power (5.7 to 18V), MCU system power (4.5 to 5.5V), and analog system power (4.5 to 5.5V).
- Ambient temperature (Ta): -40 to 125°C, junction temperature (Tj): -40 to 150°C
- AEC-Q100 Grade 1 Qualified: (scheduled)
- Small package: (VQFN32: 5mm square)

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4. Block Diagram

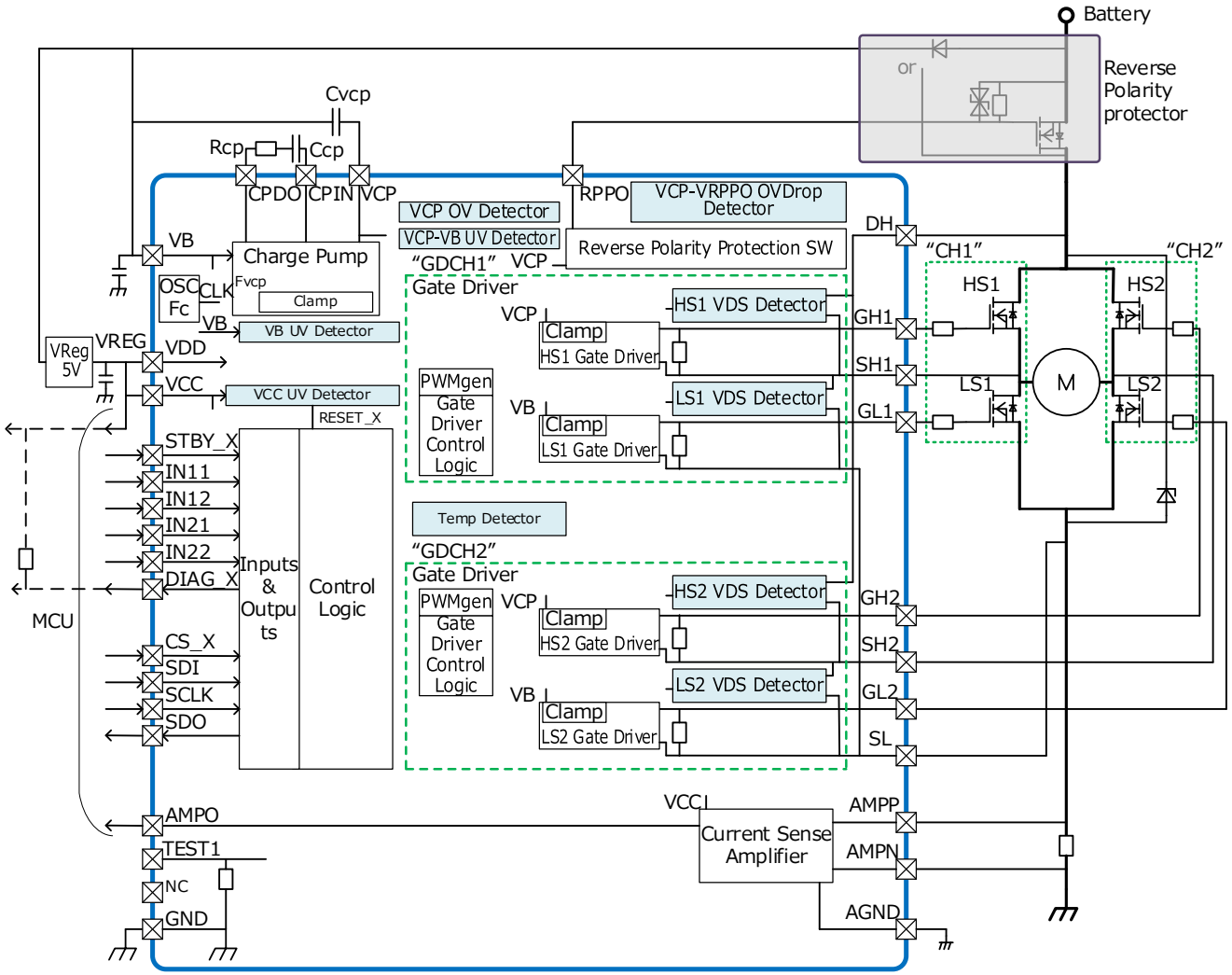


Fig. 4.1 Block Diagram

Note: The above figure is simplified and abbreviated to explain the functions and operations of the IC. Additionally, the external circuits and constants are examples and do not guarantee operation. Please consider the usage environment and make decisions after thorough evaluation and confirmation.

5. Pin Assignments

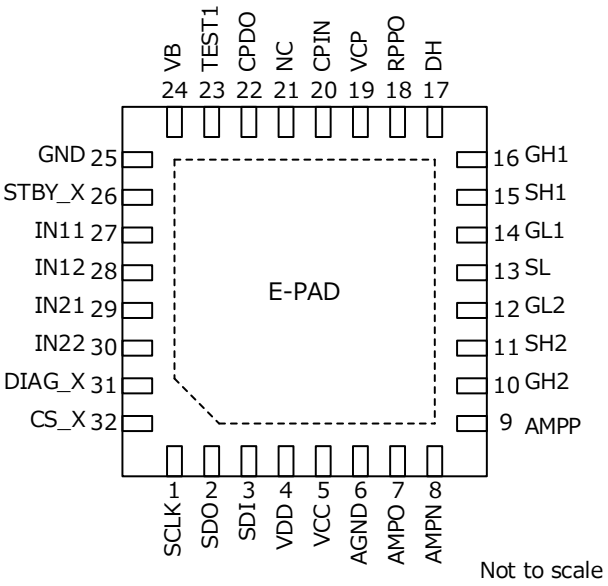


Fig. 5.1 Pin Assignments (Top View)

6. Pin Description

Table 6.1 Pin Description

Pin NO.	Symbol	Input / Output	Description
1	SCLK	Input	SPI: Serial clock input pin, Built-in pull-down resistor
2	SDO	Output	SPI: Serial data output pin, 3 state out
3	SDI	Input	SPI: Serial data input pin Built-in pull-down resistor
4	VDD	Power Input	Digital Circuit Power Input pin Please connect the VCC terminal and the VDD terminal to the same power supply.
5	VCC	Power Input	Analog circuit power input terminal, IC initialization signal generation at low voltage, built-in Low pass filter Please connect the VCC terminal and the VDD terminal to the same power supply.
6	AGND	Ground	Current Sense Amplifier: ground pin
7	AMPO	Analog Output	Current Sense Amplifier: Output pin
8	AMPN	Analog Input	Current Sense Amplifier: Input pin (negative)
9	AMPP	Analog Input	Current Sense Amplifier: Input pin (positive)
10	GH2	Output	Gate Driver GDCH2: Driving the gate of an high-side nMOSFET
11	SH2	Bidirectional	Gate Driver GDCH2: Connecting to the source of an high-side nMOSFET
12	GL2	Output	Gate Driver GDCH2: Driving the gate of an low-side nMOSFET
13	SL	Bidirectional	Connecting the source of low-side nMOSFETs
14	GL1	Output	Gate Driver GDCH1: Driving the gate of an low-side nMOSFET
15	SH1	Bidirectional	Gate Driver GDCH1: Connecting to the source of an high-side nMOSFET
16	GH1	Output	Gate Driver GDCH1: Driving the gate of an high-side nMOSFET
17	DH	Input	Connecting to the drain of high-side nMOSFETs
18	RPPO	Power Output	power supply for battery reverse connection prevention circuit
19	VCP	Bidirectional	Charge pump section smooth capacitor connection pin
20	CPIN	Bidirectional	Charge pump section boost input terminal
21	NC	-	Non-Connection Please do not connect to anything.
22	CPDO	Output	Charge pump section drive output terminal
23	TEST1	Test terminal	Test signal terminal: Do not connect to anything. Built-in pull-down resistor
24	VB	Power Input	Power supply pin
25	GND	Ground	Ground pin
26	STBY_X	Input	Standby instruction input terminal (negative logic) Built-in pull-down resistor Built-in Low pass filter
27	IN11	Input	Control input 1 for gate driver 1, Built-in pull-down resistor
28	IN12	Input	Control input 2 for gate driver 1, Built-in pull-down resistor
29	IN21	Input	Control input 1 for gate driver 2, Built-in pull-down resistor
30	IN22	Input	Control input 2 for gate driver 2, Built-in pull-down resistor
31	DIAG_X	Output	Abnormal condition detection notification Output terminal (negative logic) Normal high impedance / Abnormal low output
32	CS_X	Input	SPI: Chip select (negative logic) Built-in pull-up resistor

7. Functional Description

7.1. Operating condition

The TB9104FTG has three operating states: standby state, reset state, and normal operation state. In the standby state, power is turned off or operation is stopped for all circuits to reduce power consumption. In the reset state, each circuit is stopped, and the registers are initialized, but some circuits are on standby to transition to the normal state. In the normal operation state, each circuit operates, waiting for instructions from the MCU to drive the gate of the external n-type MOSFET. Additionally, in the normal operation state, each circuit stops in response to any abnormalities. The operating states are shown in Table 7.1.1.

The actions to be taken when an abnormality is detected must be pre-configured by the user via SPI. If multiple abnormalities occur simultaneously, the stop instructions for each abnormality are combined. The recovery procedure after the abnormal state is resolved can also be pre-selected via SPI. The types of abnormal states are shown in Table 7.1.2.

Please connect the VDD pin and the VCC pin to the same power supply. The voltage of the VCC pin is related to the generation of the reset signal.

The reset is released when the voltage of the VCC pin exceeds the low voltage detection recovery voltage VvccUr and the STBY_X pin is above VinpH. Before releasing the reset, ensure that the voltage of the VB pin, which is the power supply for the charge pump circuit and the low-side gate driver section, is at VvbRNG.

Fig. 7.1.1 shows the transitions for VDD, VCC, and STBY_X, among others. Additionally, Fig. 7.2.1 shows the transition waveform to normal operation, including VB, VCC, VDD, and STBY_X.

Table 7.1.1 Operating condition

No.	IC operating status	VB voltage , VCC voltage , VDD voltage	STBY_X pin	IN11, IN12, IN21, IN22 pin	OSC	Control logic , registers, GetStart-bit	Charge pump , CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	DIAG_X pin
1	Reset state	VvbRNG , (VCC=VDD) < VvccUd	Do not care	Do not care	-	Stop , Initial value, 0(L)	Stop, Z	Z	RL, RL, RL, RL	Z
2	Stand by state	VvbRNG , VvccRNG , VvddRNG	L	Do not care	Stop	Stop , Initial value, 0(L)	Stop, Z	Z	RL, RL, RL, RL	Z
3	Normal operation Before the operation starts.	VvbRNG , VvccRNG , VvddRNG	H	Do not care	Oscill ation	Operate, Operate, 0(L)	Operate	VCP voltage	L, L, L, L	L
4	Normal operation When no anomalies are detected.	VvbRNG , VvccRNG , VvddRNG	H	Input instru ctions	Oscill ation	Operate, Operate, 1(H)	Operate	VCP voltage	H/L, H/L, H/L, H/L See 7.17	Z

Explanation of symbols: RL = Resistive low H = High L = Low Z = High-impedance

Table 7.1.2 Types of detectable anomalies

No.	Content of the anomaly	Explanation
1	The VCC pin voltage is low.	Initialized due to low VCC voltage.
2	The VB pin voltage is low.	There is a possibility that the gate drive voltage may become insufficient.
3	The VCP pin voltage is high.	There is a possibility of exceeding the voltage withstand of the VCP pin.
4	The voltage between VCP and VB is low.	The boost from the charge pump is insufficient. There is a possibility that the gate drive voltage may become insufficient.
5	The voltage between VCP and RPPO is high.	There is a ground fault or other abnormality outside the RPPO terminal.
6	SPI abnormal	The communication format is incorrect. Accessed a prohibited area.
7	Tj is a high temperature	Exceeding the upper limit of the operating temperature range.
8	The Vdson of HS1 is high voltage.	An excessive current is flowing through the external n-type MOSFET "HS1" that is turned on.
9	The Vdson of LS1 is high voltage.	An excessive current is flowing through the external n-type MOSFET "LS1" that is turned on.
10	The Vdson of HS2 is high voltage.	An excessive current is flowing through the external n-type MOSFET "HS2" that is turned on.
11	The Vdson of LS2 is high voltage.	An excessive current is flowing through the external n-type MOSFET "LS2" that is turned on.

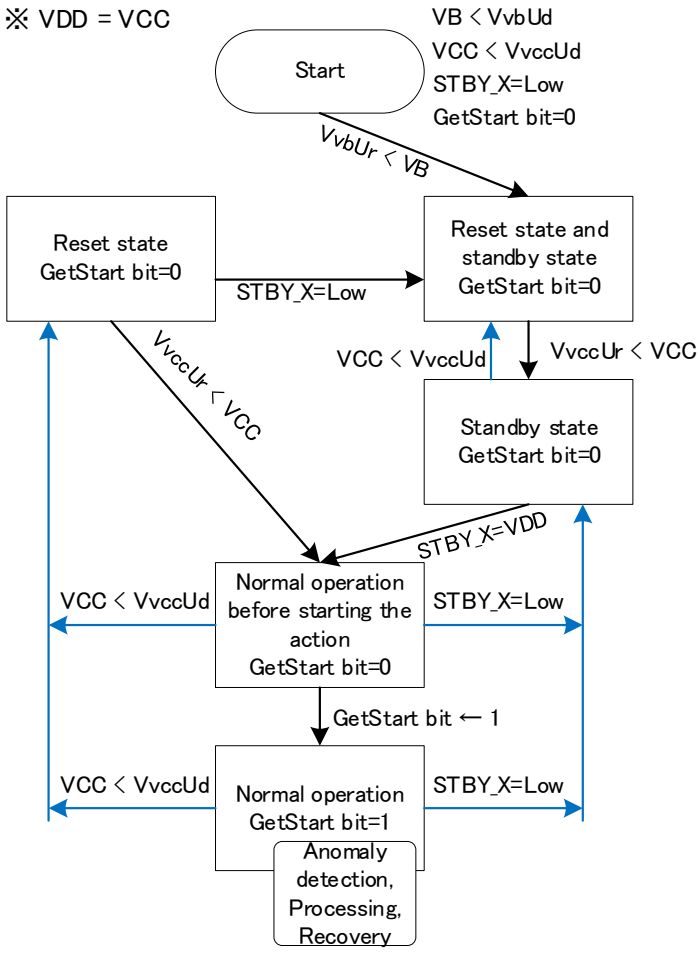


Fig. 7.1.1 State transition diagram

7.2. Start command (Getting Started Command) and procedure

GetStart Command/Status: Initial value 0

This is a register to inform the MCU that initialization occurred due to low VCC voltage while using TB9104FTG.

When starting to use TB9104FTG, first write 1 in the GetStart register. If this register is 0, none of the registers can be written to from the MCU. However, it is possible to read it. Regardless of the state of this command, the internal circuits are operational, and the error status will be rewritten according to the settings and state.

After writing 1 to the GetStart register, set the values for each register according to the desired operation. In particular, the settings for the actions to be taken when an abnormality is detected—VB_UV_op[2:0], VCPVB_UV_op[2:0], VCPRPPO_ODV_op[2:0], TJ_OT_op[2:0], VDS1H_OV_op[2:0], VDS1L_OV_op[2:0], VDS2H_OV_op[2:0], VDS2L_OV_op[2:0]—should be configured promptly after transitioning to the normal operation state.

The abnormality detection circuit immediately starts operating according to the settings, and if the error status is 1, writing to the corresponding register is not possible. Please ensure these settings are configured at least before executing the gate drive.

Table 7.2.1 Example of operation procedure after initialization.

Procedure	IC operating state , Instructions from MCU	VB voltage , VCC voltage , VDD voltage	STBY_X pin	IN11, IN12, IN21, IN22 pins	Oscillator	Control logic , registers, GetStart-bit	Charge pump , CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	DIAG_X pin
1	Reset state, STBY_X=L	VvbRNG , The VCC voltage falls below VvccUd.	L	Do not care	Stop	Stop, Initial value, 0(L)	Stop, Z	Z	RL, RL, RL, RL	Z
2	Standby state, STBY_X=L	VvbRNG , VvccRNG , VvddRNG	L	Do not care	Stop	Stop, Initial value, 0(L)	Stop, Z	Z	RL, RL, RL, RL	Z
3	Normal operation state (Abnormality not detected), STBY_X: L to H	VvbRNG , VvccRNG , VvddRNG	H	Do not care	Oscillation	Operating after Twakespi, Operating after Twakespi, 0(L)	Operating (during voltage increase), Operating	Same voltage as VCP.	Twake period, L, L, L, L	L
4	Normal operation state. (Abnormality not detected) , Write a 1 to a GetStart-bit.	VvbRNG , VvccRNG , VvddRNG	H	Do not care (L,L,L,L)	Oscillation	Operating, Operating, 1(H)	Operating (during voltage increase), Operating	Same voltage as VCP.	Twake period,, L, L, L, L	Z
5	Normal operation state. Charge pump boosting. Twake period. , Set to each register	VvbRNG , VvccRNG , VvddRNG	H	Do not care (L,L,L,L)	Oscillation	Operating, Operating, 1(H)	Operating (during voltage increase), Operating	Same voltage as VCP.	Twake period, L, L, L, L	Z
6	Normal operation state. Charge pump boost completed. , Confirm wkupsts=0.	VvbRNG , VvccRNG , VvddRNG	H	L,L,L,L	Oscillation	Operating, Operating, 1(H)	Operating, Operating	Same voltage as VCP.	L, L, L, L	Z
7	Normal operation state. (Abnormality not detected) , Instructing actions.	VvbRNG , VvccRNG , VvddRNG	H	Instructing actions.	Oscillation	Operating, Operating, 1(H)	Operating, Operating	Same voltage as VCP.	Drive according to the action instructions. (H/L) Refer to 7.17	Z

Explanation of symbols: RL = Resistive low H = High L = Low Z = High-impedance

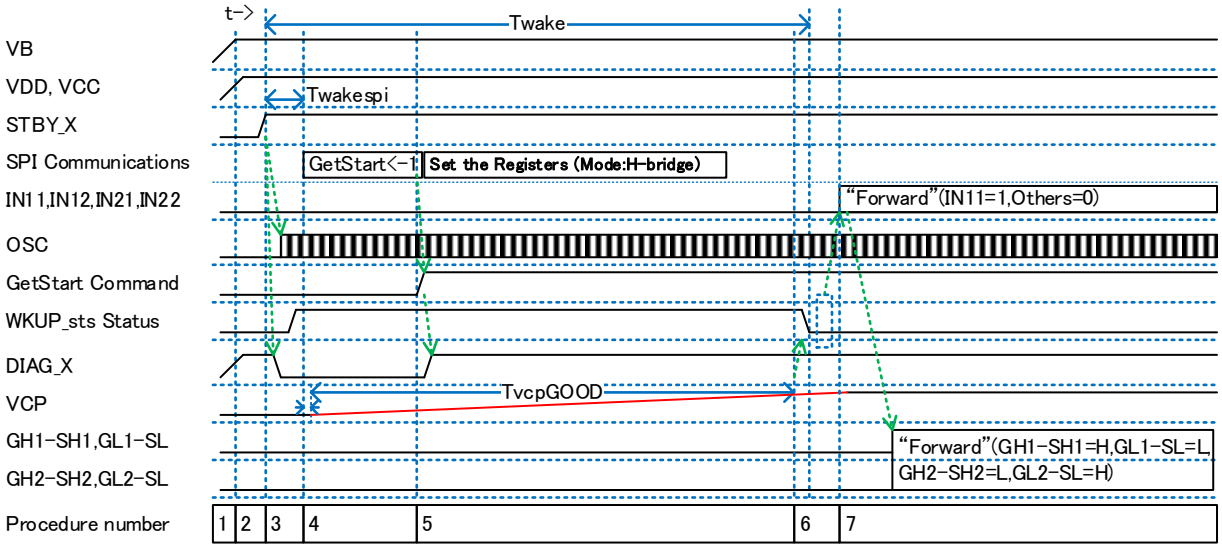


Fig. 7.2.1 Example of starting operation procedure. (Table 7.2.1)

7.3. VDD pin, VCC pin, VCC low voltage detection circuit

Please connect the VCC terminal and the VDD terminal to the same power supply. VDD is the power supply for the circuits related to STBY_X, IN11, IN12, IN21, IN22, and SPI. VCC is the power supply for the analog circuits.

When the voltage at the VCC terminal (VCC voltage) is below VvccUd, the TB9104FTG stops operating and each part returns to its initial state. This is referred to as the reset state. When the VCC voltage is above VvccUr, the TB9104FTG operates according to the instructions of STBY_X, IN11, IN12, IN21, IN22, and SPI.

The comparator that compares the VCC voltage has a hysteresis voltage VvccUhys to eliminate glitches caused by noise superimposed on the VCC terminal voltage. Additionally, it is equipped with an analog Low Pass Filter (hereafter LPF) to utilize only signals that exceed the width of TvccUpw.

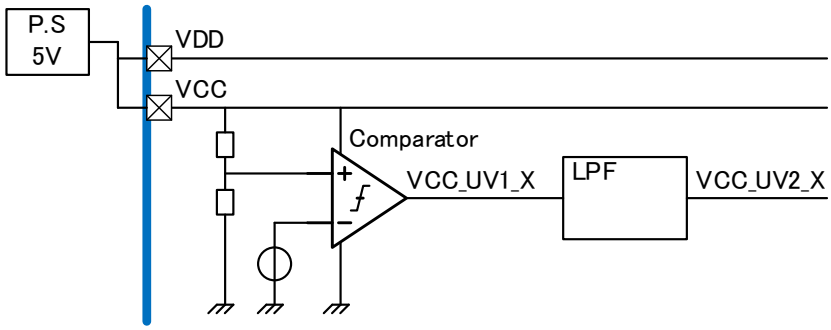


Fig. 7.3.1 VDD pin, VCC pin, VCC low voltage detection circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.4. STBY_X pin, standby circuit

The STBY_X pin can put the TB9104FTG into a low power consumption state.

In any operational state, reducing the voltage at the STBY_X pin (STBY_X voltage) below VinpL will cause the internal circuit to turn off or stop operating. The register settings will also return to their initial values, a condition referred to as standby mode. TB9104FTG can transition to standby mode even while gate driving, and in such cases, neither abnormality detection nor gate control can be performed. If you use it in this manner, please thoroughly verify it. Typically, to avoid unnecessary trouble, turn off the gate drive before entering standby mode.

When the STBY_X voltage exceeds VinpH, it transitions to either a reset state or normal operating state depending on the VCC voltage. The STBY_X pin is pulled down to GND with a 50kΩ resistor to prevent the TB9104FTG from entering its normal operating state when the terminal is open.

The input buffer of the STBY_X pin has the hysteresis voltage (VinpHYS) to eliminate glitches caused by noise superimposed on the signal. Furthermore, it is equipped with an analog LPF in the later stage, utilizing only signals with a width exceeding Tstby_xPW.

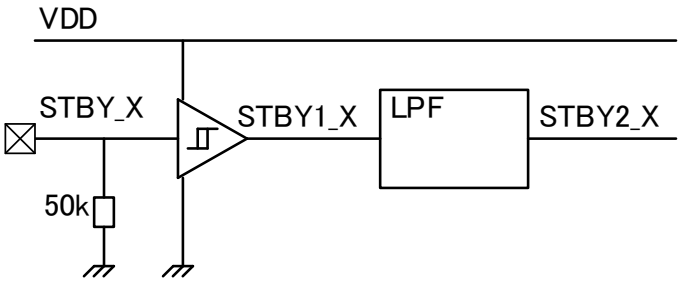


Fig. 7.4.1 STBY_X pin, LPF

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.5. Oscillator circuit

The TB9104FTG has a built-in oscillation circuit with a typical oscillation frequency of 4MHz. This circuit supplies a clock with sufficient pulse width and amplitude, free from glitches, from the start to the stop of oscillation to prevent malfunction of logic components. The oscillation circuit ceases oscillation during the reset and standby periods.

7.6. VB pin, VB low voltage detection circuit

If the voltage at the VB pin is below VvbUd, the TB9104FTG determines it to be abnormal. If the voltage at the VB pin is above VvbUr, the TB9104FTG determines it to be normal. The comparator at the VB pin has the hysteresis voltage (VvbUhys) to eliminate glitches caused by noise superimposed on the voltage at the VB terminal. Furthermore, it is equipped with a LPF in the later stage, utilizing only signals with a width exceeding TvbUpw. The operation when detecting low VB voltage can be selected by the operation setting command VB_UV_op[2:0] from SPI.

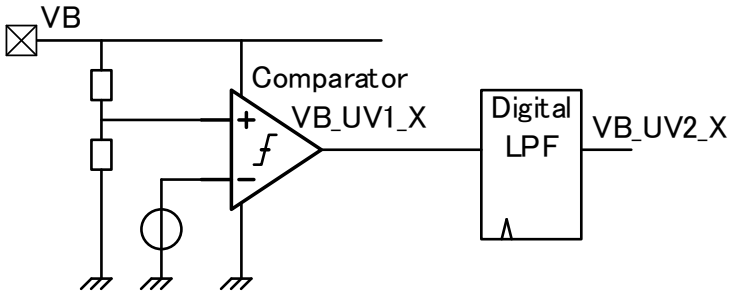


Fig. 7.6.1 VB pin, VB low voltage detection circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Table 7.6.1 Operation during VB low voltage detection(Overview)

Action setting command VB_UV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VB_UV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VB_UV=1. Then, set the clear command VB_UV_cl to 1, which will reset VB_UV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	Detected	R: Set the status register VB_UV to 1. G: Stop all gate drives. C: It does not influence the operation.
	Recovered	R: Maintain VB_UV=1. Then, set the clear command VB_UV_cl to 1, which will reset VB_UV to 0. G: Quickly resume gate drive. C: It does not influence the operation.
“011”	Detected	R: Set the status register VB_UV to 1. G: Stop all gate drives. C: It does not influence the operation.
	Recovered	R: Maintain VB_UV=1. Then, set the clear command VB_UV_cl to 1, which will reset VB_UV to 0. G: Keep the gate drive stopped. Then, set VB_UV_cl to 1 to resume. C: It does not influence the operation.
“100”	Detected	R: Set the status register VB_UV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VB_UV=1. Then, set the clear command VB_UV_cl to 1, which will reset VB_UV to 0. G: Quickly resume gate drive. C: Quickly resume the charge pump.
“101”	Detected	R: Set the status register VB_UV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VB_UV=1. Then, set the clear command VB_UV_cl to 1, which will reset VB_UV to 0. G: Keep the gate drive stopped. Then, set VB_UV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VB_UV_cl to1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note: Please do not use the setting marked as 'Reserved'.

Table 7.6.2 Operation during VB low voltage detection(details)

Action setting command VB_UV_op [2:0] 7.18.13	Detection transition	IN11, IN12, IN21, IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	VB_UV status
"000"	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0
"001"	Detected	INST(H,L)	Operating	Operating	VCP	Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0 after clearing
"010"	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume	0 after clearing
"011"	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clearing	0 after clearing
"100"	Detected	Do not care	Stop	Z	VCP	RL, RL, RL, RL	1
	Recovered	INST(H,L)	Resume	Resume	VCP	Resume	0 after clearing
"101"	Detected	Do not care	Stop	Z	VCP	RL, RL, RL, RL	1
	Recovered	INST(H,L)	Resume after clearing	Resume after clearing	VCP	Resume after clearing	0 after clearing

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

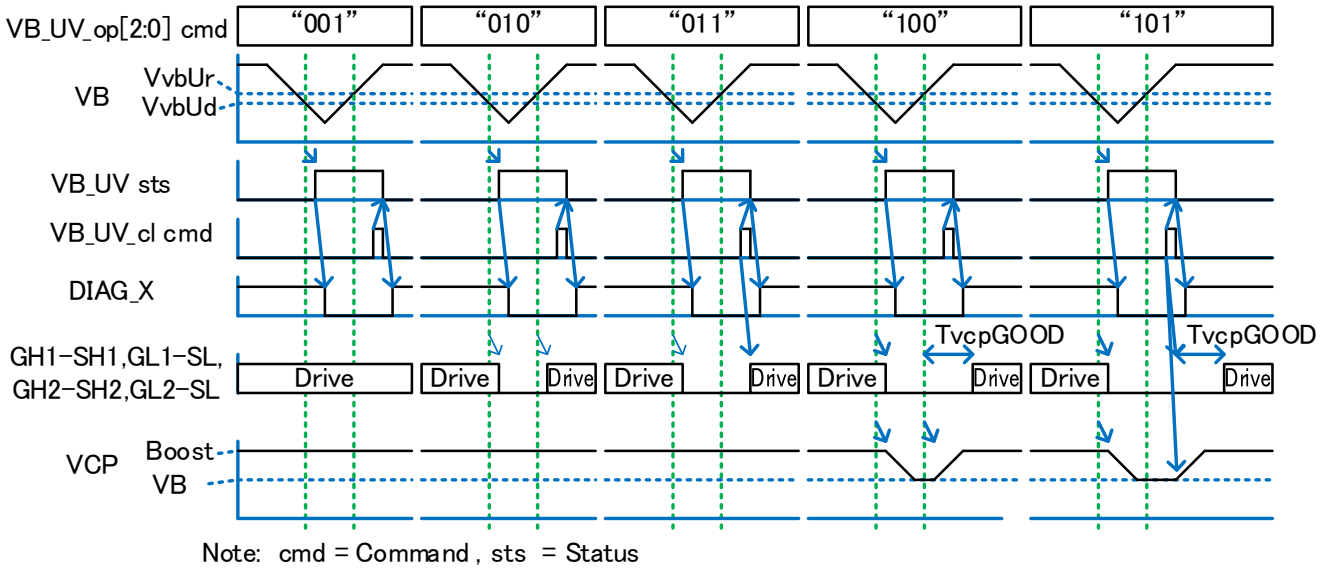


Fig. 7.9.1.2 Operation during VB low voltage detection

7.7. Gate driver instruction input pin

The IN11, IN12, IN21, and IN22 terminals receive instructions from the MCU for the gate driver section. Each IN terminal is pulled down to GND with a 50kΩ resistor to prevent unintended operation when the terminal is open. The input buffer of each IN terminal has a hysteresis voltage (VinpHYS) to eliminate glitches caused by noise superimposed on the signal. The signal then enters the digital circuit area and is immediately synchronized with the built-in clock. Additionally, it is equipped with a LPF that only allows signals that are continuous for a certain period of time to pass through. Therefore, when driving each IN terminal with PWM, there is an upper limit to the driving frequency.

By setting the INspiSEL command to 1, you can issue instructions from the INspi11, INspi12, INspi21, and INspi22 commands instead of the IN11, IN12, IN21, and IN22 terminals.

Please complete the settings in the command register before issuing the instruction to turn on the gate driver. While settings can be made while it is on, doing so may result in unexpected behavior.

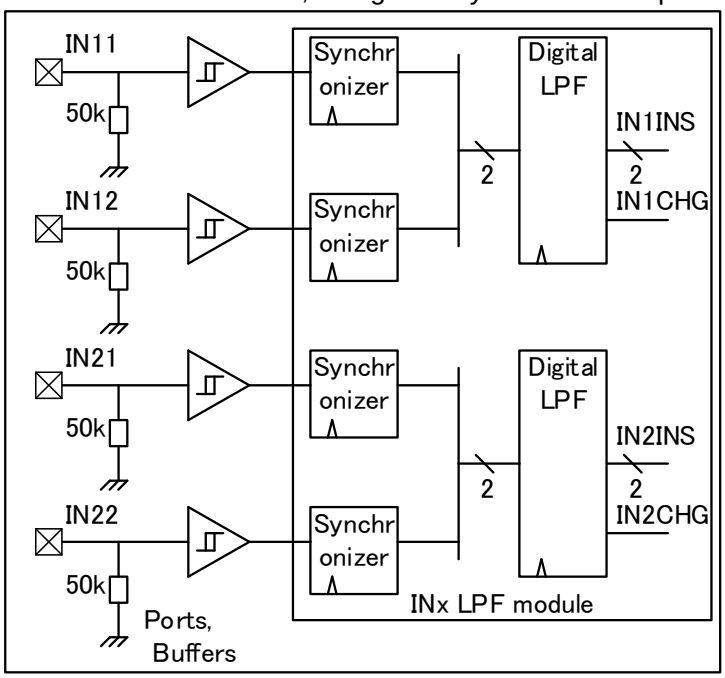


Fig. 7.7.1 IN11, IN12, IN21, IN22 pins and digital LPF

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.8. DIAG_X pin

The DIAG_X terminal indicates the diagnostic results of the internal operation status of the TB9104FTG. It outputs Low when an abnormality is detected and becomes high impedance when no abnormality is detected. The DIAG_X terminal must be connected to the power supply of the connection destination via an external resistor. The DIAG_X terminal can withstand short circuits to VDD level or ground without damage, regardless of the output level.

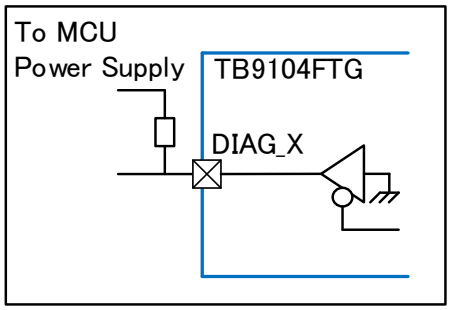


Fig. 7.8.1 DIAG_X pin

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.9. SPI pin, SPI circuit

Each input terminal of the SPI is pulled up or pulled down with a 50kΩ resistor to prevent unintended operation when the terminal is open. The CS_X terminal is pulled up to VDD. The SDI and SCLK terminals are pulled down to GND. The SDO terminal is driven by a three-state buffer. When the CS_X terminal is High, the SDO terminal becomes high impedance. To communicate, the CS_X terminal must be set to Low. The SDO terminal has the capability to withstand short circuits to VDD level or ground without damage, regardless of the output level.

The SPI (Serial Peripheral Interface) mode of the TB9104FTG is SPI Mode 1 (CPOL=Low, CPHA=High). In SPI Mode 1, the level of the SDI terminal is captured on the falling edge of SCLK. Bits are shifted out from the SDO terminal on the rising edge of SCLK.

The SPI module does not operate in reset or standby states. Additionally, the values set in the registers return to their default values. After the falling edge of the CS_X signal, a wait time Tcs_xsclk is required until the rising edge of the SCLK signal. Additionally, after that, TsdoDLY is needed for the SDO signal to transition from high impedance to valid data.

On the rising edge of the SCLK signal, the MCU outputs data to the SDI signal. On the next falling edge of the SCLK signal, the TB9104FTG captures data from the SDI signal. Note that the data on the SDI signal requires a setup time TsdiSET and a hold time TsdiHLD relative to the falling edge of the SCLK signal. On the rising edge of the SCLK signal, the TB9104FTG outputs data to the SDO signal. On the next falling edge of the SCLK signal, the MCU captures data from the SDO signal.

A wait time Tsclkcs_x is required from the last falling edge of the SCLK clock to the rising edge of the CS_X signal. Additionally, Tsdocs_xDLY is needed for the SDO signal to become high impedance after that. A wait time Tcs_xH is required from the rising edge to the next falling edge of the CS_X signal.

Please refer to Fig. 10.4.1 for these timings. Data on the SDI signal is expected to be sent in the order from MSB to LSB. Data on the SDO signal is sent in the order from MSB to LSB.

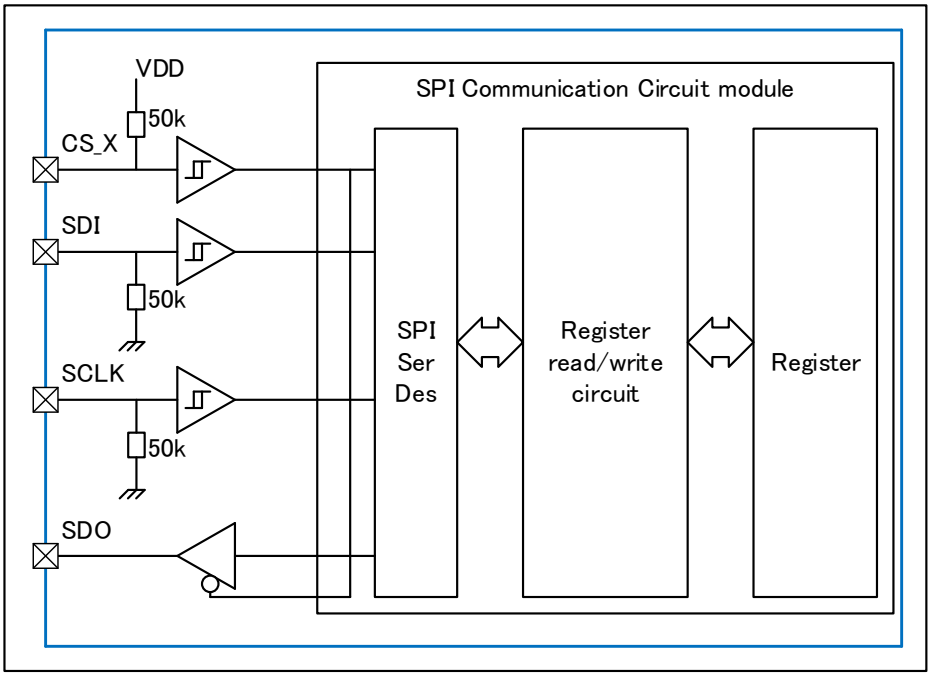


Fig. 7.9.1 SPI each pin and SPI circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.9.1. SPI communication operation

The frame length is 16 bits. The frame consists of address bits A[3:0], read/write bit RD+/WR-, data bits D[9:0], and an even parity bit EvenP for data checking on the SDI signal. There are two functions: read operation and write operation, which are selected by the read/write bit RD+/WR-. The frame structure is shown in Fig. 7.9.1.1.

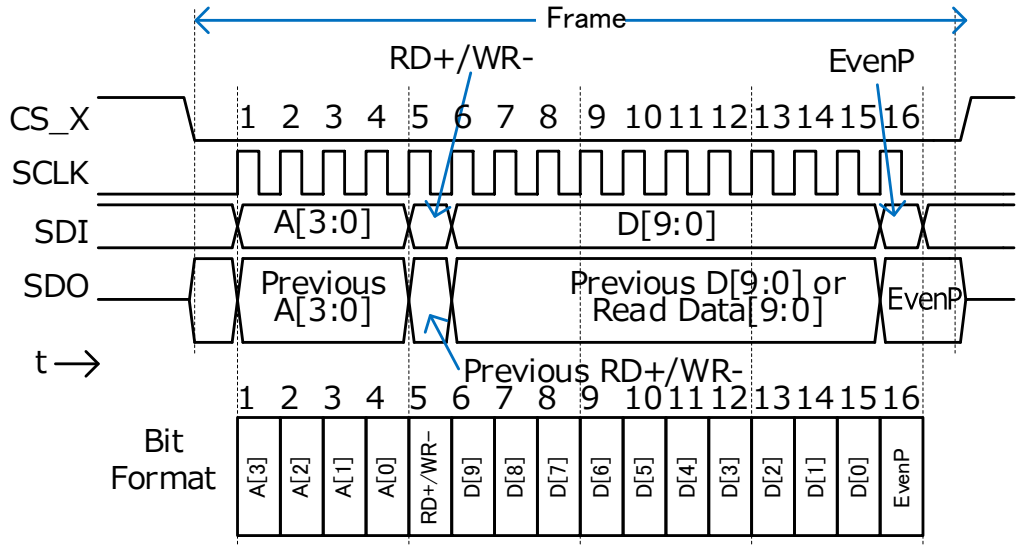


Fig. 7.9.1.1 Frame format

When performing a write operation, refer to Table 7.18.1 to find the address of the register you want to write to and prepare the data to be written. Next, access each terminal of the TB9104FTG as shown in Fig. 7.9.1.1. For the SDI terminal, input the address from MSB to LSB, the “RD+/WR-” bit as 0, and the write data from MSB to LSB in sequence. Finally, input even parity for all bits from the address to the "RD+/WR-" bit 0 and the write data.

When performing a read operation, refer to Table 7.18.1 to find the address of the register you want to read. Next, access each terminal of the TB9104FTG as shown in Fig. 7.9.1.1. For the SDI terminal, input the address from MSB to LSB, the "RD+/WR-" bit as 1, and "0" as the write data. Finally, input even parity generated for all bits up to this point. The read data is output from the SDO terminal in the next frame. The bit order is the same as for the write operation. A dummy frame (write or read to the NOP register) can also be used as the next frame to retrieve the read data.

An example of SPI communication is shown in Fig. 7.9.1.2.

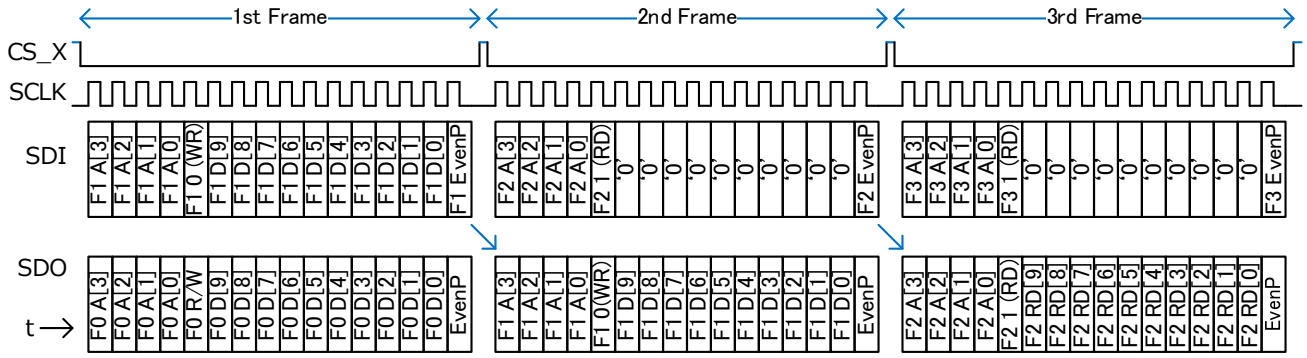


Fig. 7.9.1.2 Example of SPI communication transmission and reception.

7.9.2. SPI Errors

An SPI Error occurs under the following conditions:

- The frame length of the serial communication is not 16 SCLK.
- Accessing an address not provided in the register map or writing to a read-only address.
- Writing a prohibited combination in commands with bit widths.
- Parity error.

A frame length error occurs if the number of SCLKs is less than 16; the error is detected at the rising edge of CS_X. If there are 17 or more SCLKs, the SDO terminal outputs 0 (Low), and the error is detected at the rising edge of CS_X.

A parity error occurs if the number of bits set to 1 in the 16-bit data is odd. Note that parity errors cannot be accurately detected if there are two or more bit errors.

When any of the above conditions occur, the TB9104FTG sets the SPIError register to 1. When SPIError is set to 1, the DIAG_X terminal outputs Low. After detecting an error, normal communication may not be possible, but you should continue to access until recovery. After detecting an error, during the first normal communication, the TB9104FTG returns the previous address 4 bits and “RD+/WR-” bit, followed by 10 bits of 0 and an intentionally incorrect parity bit from the SDO terminal. It is expected that the parity bit will return to normal in subsequent communications.

After normal communication is possible, writing 1 to the SPIError_cl register will reset the SPIError register to 0. After normal communication is restored, please check that the various settings within the TB9104FTG are the same as before the error occurred.

7.10. Charge pump circuit

The TB9104FTG incorporates a charge pump circuit to drive the gate of the high-side external n-type MOSFET. It provides a 2x voltage boost. The charge pump circuit stops operating during the reset and standby states. During the Twake period immediately after transitioning to the normal operating state and the TvcpGOOD period after the charge pump starts, the voltage boost is insufficient. Therefore, the gate drive is turned off, and low voltage detection abnormalities between VCP and VB, as well as high voltage detection abnormalities between VCP and RPPO, are not determined.

During operation, if the VCP voltage exceeds the clamp voltage VCPCL1d, the charge pump circuit immediately stops boosting and resumes when it falls below, maintaining a constant VCP voltage. The CPDO terminal oscillates between GND voltage and VB voltage according to the driving frequency. The driving frequency is 200kHz (typical), which is lower than the medium wave band of radio. The CPDO terminal is at GND voltage when stopped. The CPDO terminal is at GND level when stopped.

The CPIN terminal is the input terminal for the boosted voltage.
The VCP terminal is for connecting a smoothing capacitor to stabilize the boosted voltage.
If the charge pump operation continues to stop, the VCP voltage gradually transitions to the VB voltage.
Do not apply external voltage to the VCP terminal.

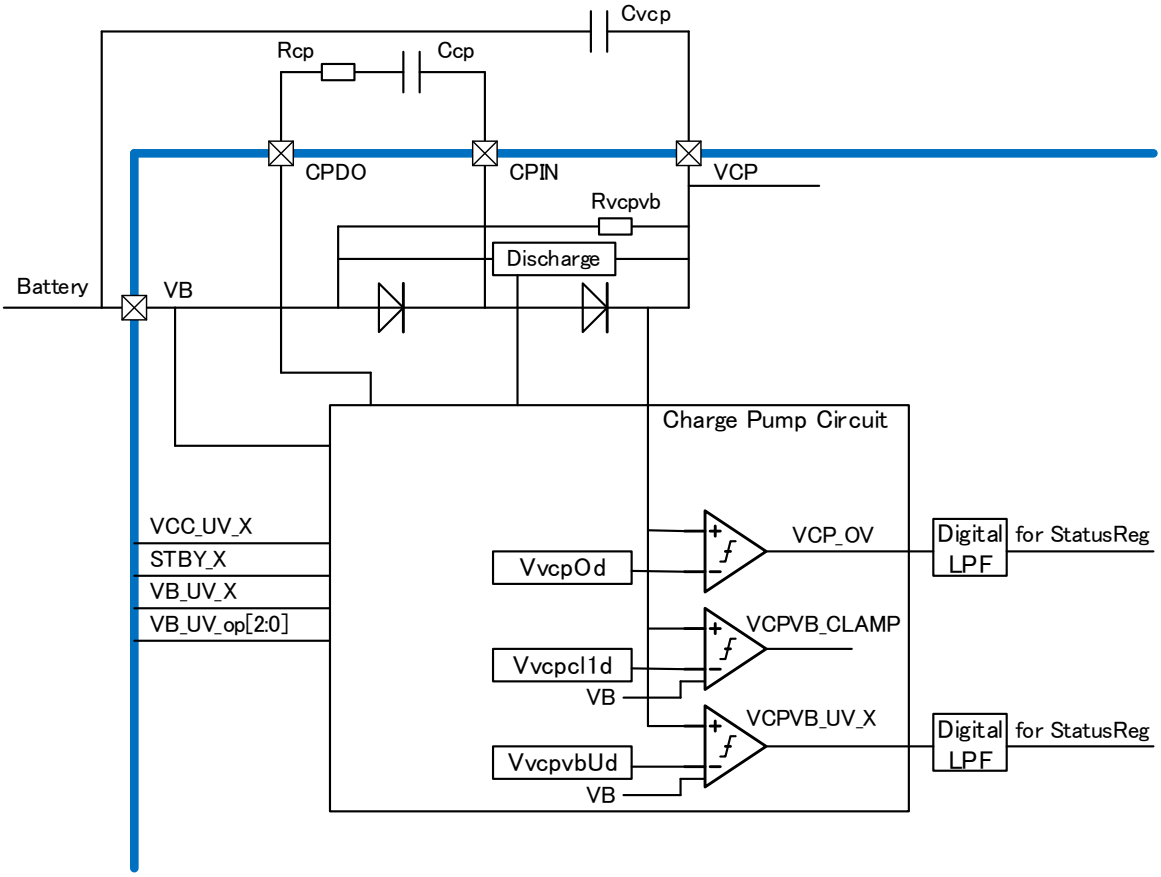


Fig. 7.10.1 Charge pump circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.10.1. VCP high voltage detection circuit and abnormal processing

The VCP overvoltage detection circuit monitors the voltage at the VCP terminal and detects overvoltage. If the voltage at the VCP terminal is equal to or greater than VvcpOd, the TB9104FTG determines it as an abnormal condition. If the voltage at the VCP terminal is equal to or less than VvcpOr, the TB9104FTG determines it as a normal condition.

The comparator at the VCP terminal has a hysteresis voltage VvcpOhys to eliminate glitches caused by noise superimposed on the voltage at the VCP terminal.

To prevent exceeding the voltage tolerance of the VCP terminal, the charge pump controller circuit immediately stops the boosting operation of the charge pump circuit and activates the discharge circuit upon receiving an overvoltage notification from the VCP overvoltage detection circuit. Furthermore, it is equipped with a LPF after the comparator, allowing only signals with a width exceeding TvcpOpw to pass through. When this signal indicates an abnormal condition, the status register VCP_OV is set to 1, stopping the boosting operation of the charge pump circuit and the gate drive.

Recovery occurs when the voltage at the VCP terminal is determined to be normal, by setting the clear command VCP_OV_cl to 1, which resets the VCP_OV status to 0. Simultaneously, the charge pump circuit resumes boosting, and after TvcpGOOD, the gate drive operation also resumes.

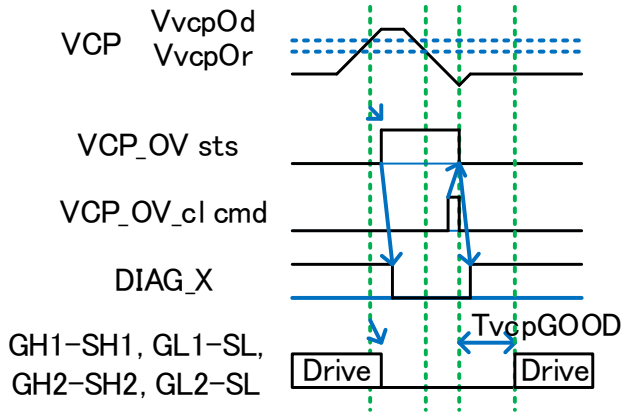
Table 7.10.1.1 Operating settings for VCP high voltage detection (Overview)

Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
Detected	R: Set the status register VCP_OV to 1 G: Stop all gate drives. C: Stop the charge pump.
Recovered	R: Maintain VCP_OV =1. Then, set the clear command VCP_OV_cl to 1, which will reset VCP_OV to 0. G: Keep the gate drive stopped. Then, set VCP_OV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VCP_OV_cl to 1 to resume.

Table 7.10.1.2 Operating settings for VCP high voltage detection (details)

Detection transition	IN11,IN12, IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	VCP_OV status
Detected	Do not care	Stop	Z	VCP	RL, RL, RL, RL	1
Recovered	INST(H,L)	Resume after clearing	Resume after clearing	VCP	Resume after clearing	0 after clearing

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance



Note cmd = Command , sts = Status

Fig. 7.10.1.1 Operation during VCP high voltage detection

7.10.2. VCP-VB low voltage detection circuit and abnormal processing

The VCP-VB low voltage detection circuit monitors the voltage at the VCP terminal and detects insufficient voltage boost. When the voltage boost is insufficient, the gate drive can be stopped.

Immediately after transitioning to normal operation, during the Twake period and the TvcpGOOD period after the charge pump starts, the voltage boost is insufficient, so it is not determined as a VCP-VB undervoltage detection abnormality. If the voltage between the VCP and VB terminals is equal to or less than VvcpvbUd, the TB9104FTG determines it to be an abnormal condition. If the voltage between the VCP and VB terminals is equal to or greater than VvcpvbUr, the TB9104FTG determines it to be a normal condition.

The comparator that compares the voltage between the VCP and VB terminals has a hysteresis voltage, VvcpvbUhys, to eliminate glitches caused by noise superimposed on the voltage between the VCP and VB terminals. Additionally, an LPF is provided after the comparator to utilize only signals with a width exceeding TvcpvbUpw. The operation when VCP-VB undervoltage is detected can be selected by the operation setting command VCPVB_UV_op[2:0] from the SPI.

Table 7.10.2.1 Operating settings for VCP-VB low voltage detection (Overview)

Action setting command VCPVB_UV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VCPVB_UV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VCPVB_UV =1. Then, set the clear command VCPVB_UV_cl to 1, which will reset VCPVB_UV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	Detected	R: Set the status register VCPVB_UV to 1. G: Stop all gate drives. C: It does not influence the operation.
	Recovered	R: Maintain VCPVB_UV =1. Then, set the clear command VCPVB_UV_cl to 1, which will reset VCPVB_UV to 0. G: Quickly resume gate drive. C: It does not influence the operation.
“011”	Detected	R: Set the status register VB_UV to 1. G: Stop all gate drives. C: It does not influence the operation.
	Recovered	R: Maintain VCPVB_UV =1. Then, set the clear command VCPVB_UV_cl to 1, which will reset VCPVB_UV to 0. G: Keep the gate drive stopped. Then, set VCPVB_UV_cl to 1 to resume. C: It does not influence the operation.
“100”	-	Reserved. Unable to set "100". It results in a SPI error.
“101”	-	Reserved. Unable to set "101". It results in a SPI error.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note: Please do not use the setting marked as 'Reserved'.

Table 7.10.2.2 Operating settings for VCP-VB low voltage detection (details)

Action setting command VCPVB_UV_op [2:0] 7.18.14	Detection transition	IN11,IN12, IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	VCPVB_UV status
“000”	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0
“001”	Detected	INST(H,L)	Operating	Operating	VCP	Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0 after clearing
“010”	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume	0 after clearing
“011”	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clearing	0 after clearing

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

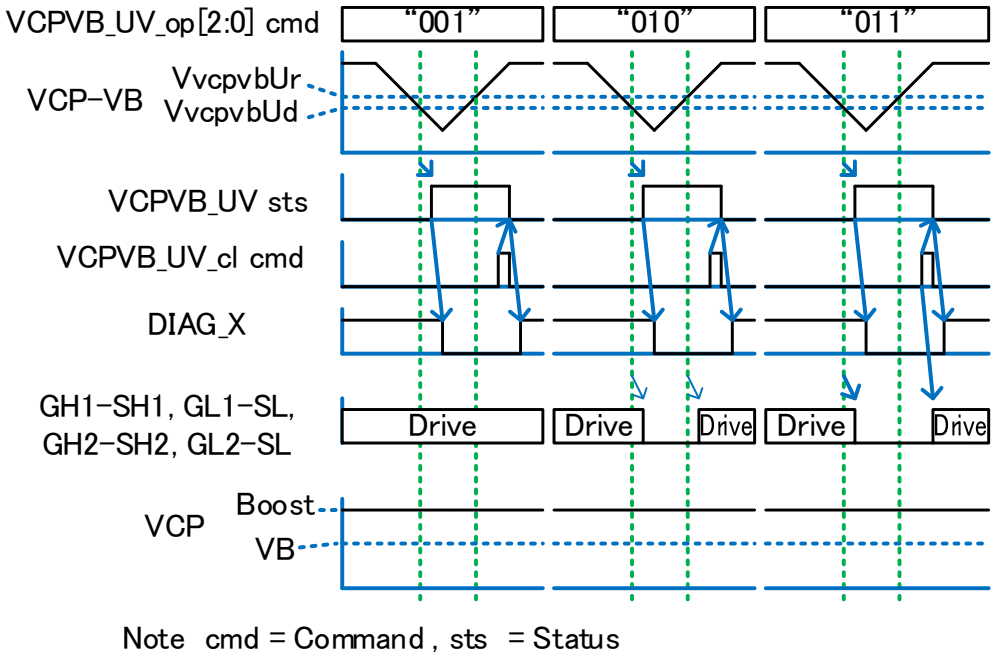


Fig. 7.10.2.1 Operation during VCP-VB low voltage detection.

7.11. Gate driver circuit for reverse polarity protection circuit

The gate driver circuit for reverse polarity protection circuit is a circuit that drives an external n-type MOSFET (hereafter referred to as the reverse polarity protection FET) for reverse connection protection, placed between the battery and the bridge circuit composed of external n-type MOSFETs. When the battery is connected with reverse polarity, the gate driver circuit for reverse polarity protection circuit turns off the reverse polarity protection FET. When the battery is connected with the correct polarity, the reverse polarity protection FET is always on while the charge pump circuit is operating. Even if the reverse polarity protection FET is off, current is supplied to the bridge circuit through the body diode.

The gate driver circuit for reverse polarity protection circuit is designed to prevent backflow to the RPPO terminal through any path when the battery is connected in reverse. The gate driver circuit for reverse polarity protection circuit cuts off current from the RPPO terminal in reset or standby states.

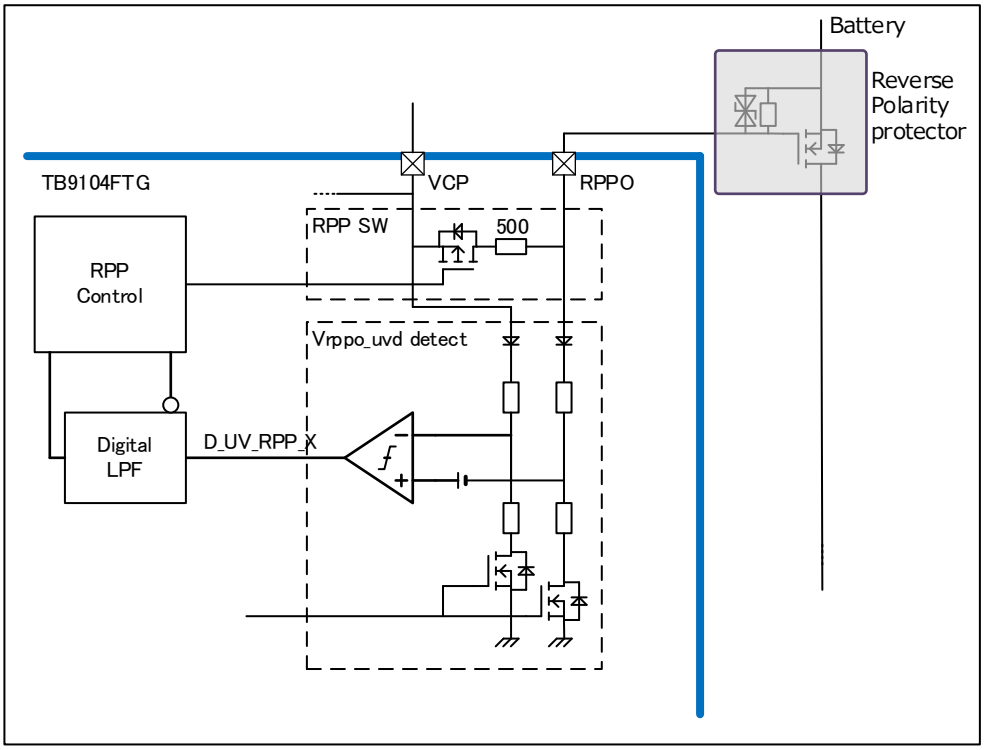


Fig. 7.11.1 Gate driver circuit for reverse polarity protection circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.11.1. VCP-RPPO high voltage detection circuit and anomaly processing

The VCP-RPPO high voltage detection circuit monitors the voltage between the VCP and RPPO terminals to detect overcurrent at the RPPO terminal. During the Twake period, immediately after transitioning to normal operation, and the TvcpGOOD period, after the charge pump starts, the boost is insufficient. Therefore, it does not determine a high voltage detection abnormality between the VCP and RPPO terminals.

If the voltage between the VCP and RPPO terminals is equal to or greater than VvcprppoOd, the TB9104FTG determines it as an abnormal condition. If the voltage between the VCP and RPPO terminals is equal to or less than VvcprppoOr, the TB9104FTG determines it as a normal condition.

The comparator has a hysteresis voltage VvcprppoOhys to eliminate glitches caused by noise superimposed on the voltage between the terminals. Additionally, an LPF is provided after the comparator to utilize only signals with a width exceeding TvcprppoOpw.

The operation when VCP-RPPO overvoltage is detected can be selected by the operation setting command VCPRPPO_ODV_op[2:0] from the SPI.

Table 7.11.1.1 Operating settings for high voltage detection in VCP-RPPO (Overview)

Action setting command VCPRPPO_ODV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump, P=RPP switch
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation. P: Supply voltage to the RPPO terminal.
“001”	Detected	R: Set the status register VCPRPPO_ODV to 1. G: It does not influence the operation. C: It does not influence the operation. P: Supply voltage to the RPPO terminal.
	Recovered	R: Maintain VCPRPPO_ODV =1. Then, set the clear command VCPRPPO_ODV_cl to 1, which will reset VCPRPPO_ODV to 0. G: It does not influence the operation. C: It does not influence the operation. P: Supply voltage to the RPPO terminal.
“010”	-	Reserved. Unable to set "010". It results in a SPI error.
“011”	-	Reserved. Unable to set "011". It results in a SPI error.
“100”	-	Reserved. (Note4)
“101”	Detected	R: Set the status register VCPRPPO_ODV to 1. G: Stop all gate drives. C: Stop the charge pump. P: Stop supplying VCP voltage to the RPPO terminal.
	Recovered (Note1)	R: Maintain VCPRPPO_ODV =1. Then, set the clear command VCPRPPO_ODV_cl to 1, which will reset VCPRPPO_ODV to 0. G: Keep the gate drive stopped. Then, set VCPRPPO_ODV _cl to 1 to resume. C: Keep the charge pump stopped. Then, set VCPRPPO_ODV _cl to1 to resume. P: Keep supplying voltage to the RPPO terminal stopped. Then, set VCPRPPO_ODV_cl to 1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	Detected	R: Set the status register VCPRPPO_ODV to 1. G: It does not influence the operation. C: It does not influence the operation. P: Stop supplying VCP voltage to the RPPO terminal.
	Recovered (Note2)	R: Keep VCPRPPO_ODV =1. G: It does not influence the operation.. C: It does not influence the operation.. P: Keep supplying voltage to the RPPO terminal stopped.

Note1: When an abnormality is detected and the charge pump stops, the VCP terminal becomes the VB voltage. If the supply of VCP voltage to the RPPO terminal is stopped, the voltage at the RPPO terminal depends on the external circuit and may not recover. To force recovery, you need to issue the REGreset command or set the STBY_X terminal to Low to initialize.

Note2: Even if an abnormality is detected, the charge pump continues to operate, and the VCP voltage may remain above VB, preventing recovery. To forcibly restart the operation, you need to issue the REGreset command or set the STBY_X terminal to Low to initialize all operations.

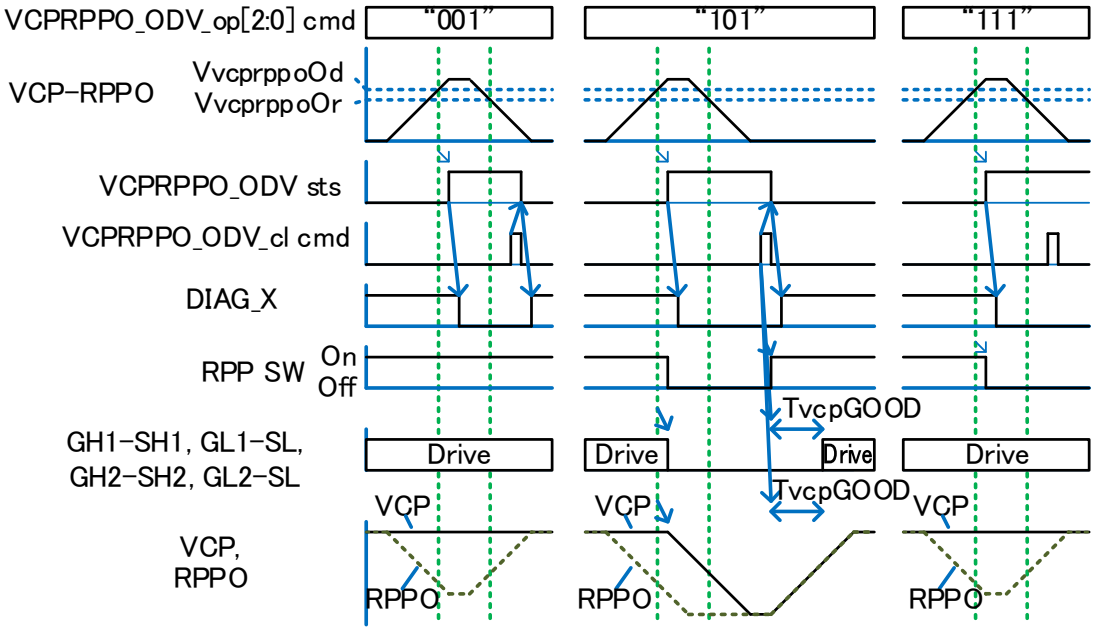
Note3: Please do not use the setting marked as 'Reserved'.

Note4: When “110” is set for VCPRPPO_ODV_op, the gate drive and charge pump stop upon detection of an abnormal condition. However, because the potential difference between the VCP and RPPO pins is eliminated, the device may subsequently be recognized as having returned to a normal state and resume operation. For this reason, the use of this setting is not recommended, as it may repeatedly alternate between stopping and resuming operation.

Table 7.11.1.2 Operating settings for VCP-RPPO during high voltage detection (details)

Action setting command VCPRPPO_ODV_op [2:0] 7.18.15	Detection transition	IN11,IN12, IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	VCPRPPO_ODV status
"000"	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0
"001"	Detected	INST(H,L)	Operating	Operating	VCP	Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0 after clearing
"101"	Detected	Do not care	Stop	Z	Stop	RL, RL, RL, RL	1
	Recovered	INST(H,L)	Resume after clearing	Resume after clearing	Resume after clearing	Resume after clearing	0 after clearing
"111"	Detected	INST(H,L)	Operating	Operating	Stop	Operating	1
	Recovered	INST(H,L)	Operating	Operating	Stop	Operating	1

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance



Note cmd = Command , sts = Status

Fig. 7.11.1.1 Operation during high voltage detection of VCP-RPPO

7.12. Gate driver circuit

The gate driver circuit uses VCP as the power supply for the high side. The gate driver circuit can set the external n-type MOSFET to three states: on, off, and high impedance.

When turning on, to prevent exceeding the gate-source breakdown voltage, the upper limit of the gate-source voltage is restricted based on the voltage at the source terminal. When turning off, the built-in MOSFET shunts the gate-source. In the high impedance state, to protect the gate of the external n-type MOSFET, the gate-source is shunted through a 50kΩ resistor.

During the Twake period immediately after transitioning to normal operation and the TvcpGOOD period after the charge pump starts, the boost is insufficient, so the gate drive is stopped.

The GH1, GL1, GH2, and GL2 terminals will not be damaged even if shorted to ground or each other.

The high side and low side drives limit the current to Igs_lmth and Igs_lmtl after the turn on, turn off times, and the time set by the t_ilim command have elapsed. For details, refer to Fig. 7.17.1.4.1.

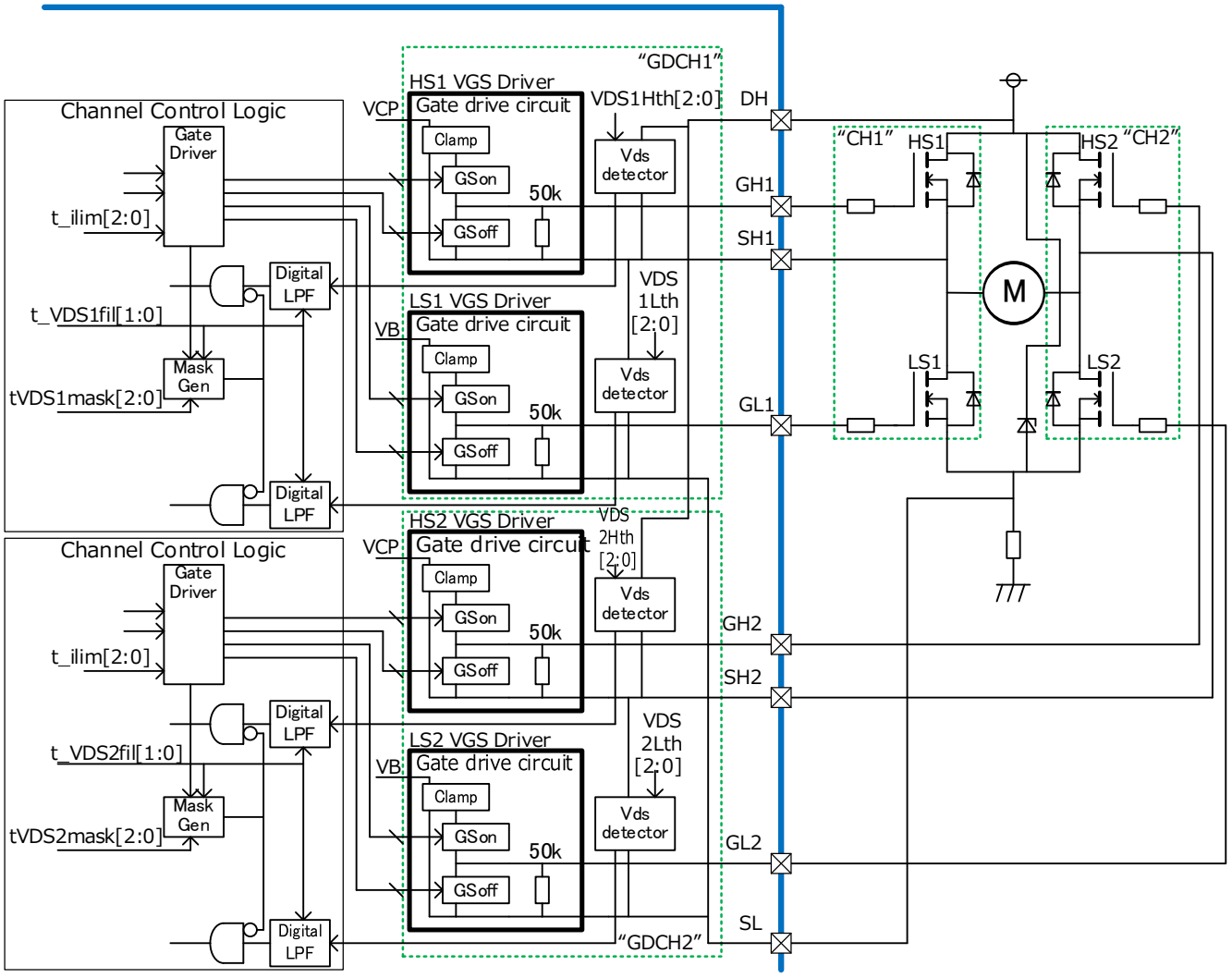


Fig. 7.12.1 Gate driver circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.13. Vdson high voltage detection circuit and abnormal processing

The TB9104FTG monitors whether the drain-source voltage (Vds) of the external n-type MOSFET is in a normal state, which is lower than the voltages set by VDS1Hth[2:0], VDS1Lth[2:0], VDS2Hth[2:0], and VDS2Lth[2:0] (VdhshOd0 to VdhshOd7, VshslOd0 to VshslOd7) while the gate is being driven.

If the voltage is higher than VdhshOd0 to VdhshOd7 or VshslOd0 to VshslOd7, it is determined to be an abnormal state with overcurrent.

The TB9104FTG has an LPF in the subsequent stage of the detection circuit and uses only signals that exceed the width set by t_VDS1fil[1:0] and t_VDS2fil[1:0].

If the drive command is changed by the IN11, IN12, IN21, or IN22 terminals, monitoring is suspended for the time set by SPI (Tvds1MASK[2:0], Tvds2MASK[2:0]) after the change.

In half-bridge mode, the channel determined to have a high VDSON voltage shuts down the drive of the external n-type MOSFET connected to its channel.

In H-bridge mode, if any channel is determined to have a high VDSON voltage, all four external FETs that form the bridge are shut down.

Please ensure that the Vds high voltage detection voltage, digital LPF cutoff pulse width (TvdsOpw), and mask time during command changes (TvdsMASK) mentioned here are thoroughly verified and set in the external circuit used.

Table 7.13.1 Operation settings for high voltage detection in HS1 Vdson (Overview)

Action setting command VDS1H_OV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VDSHS1_OV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VDSHS1_OV. Then, set the clear command VDS1_OV_cl = 1, which will reset VDSHS1_OV to 0 and VDSLS1_OV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	-	Reserved. (Note2)
“011”	Detected	R: Set the status register VDSHS1_OV to 1. G: Half-bridge: Stop GDCH1 gate drivers. H-bridge: Stop all gate drivers. C: It does not influence the operation.
	Recovered	R: Maintain VDSHS1_OV. Then, set the clear command VDS1_OV_cl = 1, which will reset VDSHS1_OV to 0 and VDSLS1_OV to 0. G: Keep the gate drive stopped. Then, set VDS1_OV_cl to 1 to resume. C: It does not influence the operation.
“100”	-	Reserved. (Note2)
“101”	Detected	R: Set the status register VDSHS1_OV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VDSHS1_OV. Then, set the clear command VDS1_OV_cl = 1, which will reset VDSHS1_OV to 0 and VDSLS1_OV to 0. G: Keep the gate drive stopped. Then, set VDS1_OV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VDS1_OV_cl to1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note1: Please do not use the setting marked as 'Reserved'.

Note2: If you set VDS1H_OV_op to "010" or "100", the gate drive will stop when an abnormality is detected, but there is a phenomenon where operation resumes if it is judged that the voltage between the drain and source has returned to normal.

Table 7.13.2 Operation settings for high voltage detection in HS1 Vdson (details)

Action setting command VDS1H_OV _op[2:0] 7.18.17	Detection transition	IN11,IN12 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL	VDSHS1_OV status
"000"	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0
"001"	Detected	INST(H,L)	Operating	Operating	VCP	Operating, Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0 after clearing.
"011"	Detected	Do not care	Operating	Operating	VCP	L, L In H-Bridge mode, GH2, GL2 are also L, L.	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clearing.	0 after clearing.
"101"	Detected	Do not care	Stop	Z	VCP	Set all gate drives to RL.	1
	Recovered	INST(H,L)	Resume after clearing.	Resume after clearing.	VCP	Resume after clearing.	0 after clearing.

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

Table 7.13.3 LS1 Vdson operating settings during high voltage detection (Overview)

Action setting command VDS1L_OV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VDSLS1_OV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VDSLS1_OV =1. Then, set the clear command VDSLS1_OV _cl to 1, which will reset VDSLS1_OV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	-	Reserved. (Note2)
“011”	Detected	R: Set the status register VDSLS1_OV to 1. G: Half-bridge: Stop GDCH1 gate drivers. H-bridge: Stop all gate drivers. C: It does not influence the operation.
	Recovered	R: Maintain VDSLS1_OV. Then, set the clear command VDS1_OV_cl = 1, which will reset VDSHS1_OV to 0 and VDSLS1_OV to 0. G: Keep the gate drive stopped. Then, set VDS1_OV_cl to 1 to resume. C: It does not influence the operation.
“100”	-	Reserved. (Note2)
“101”	Detected	R: Set the status register VDSLS1_OV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VDSLS1_OV. Then, set the clear command VDS1_OV_cl = 1, which will reset VDSHS1_OV to 0 and VDSLS1_OV to 0. G: Keep the gate drive stopped. Then, set VDS1_OV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VDS1_OV_cl to1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note1: Please do not use the setting marked as 'Reserved'.

Note2: If you set VDS1L_OV_op to "010" or "100", the gate drive will stop when an abnormality is detected, but there is a phenomenon where operation resumes if it is judged that the voltage between the drain and source has returned to normal.

Table 7.13.4 LS1 Vdson operating settings during high voltage detection (details)

Action setting command VDS1L_OV _op[2:0] 7.18.18	Detection transition	IN11,IN12 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL	VDSLS1_OV status
“000”	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0
“001”	Detected	INST(H,L)	Operating	Operating	VCP	Operating, Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0 after clearing.
“011”	Detected	Do not care	Operating	Operating	VCP	L, L In H-Bridge mode, GH2, GL2 are also L, L.	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clearing.	0 after clearing.
“101”	Detected	Do not care	Stop	Z	VCP	Set all gate drives to RL.	1
	Recovered	INST(H,L)	Resume after clearing.	Resume after clearing.	VCP	Resume after clearing.	0 after clearing.

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

Table 7.13.5 Operation settings for HS2 Vdson high voltage detection (overview)

Action setting command VDS2H_OV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VDSHS2_OV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VDSHS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	-	Reserved. (Note2)
“011”	Detected	R: Set the status register VDSHS2_OV to 1. G: Half-bridge: Stop GDCH2 gate drivers. H-bridge: Stop all gate drivers. C: It does not influence the operation.
	Recovered	R: Maintain VDSHS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: Keep the gate drive stopped. Then, set VDS2_OV_cl to 1 to resume. C: It does not influence the operation.
“100”	-	Reserved. (Note2)
“101”	Detected	R: Set the status register VDSHS2_OV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VDSHS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: Keep the gate drive stopped. Then, set VDS2_OV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VDS2_OV_cl to1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note1: Please do not use the setting marked as 'Reserved'.

Note2: If you set VDS2H_OV_op to "010" or "100", the gate drive will stop when an abnormality is detected, but there is a phenomenon where operation resumes if it is judged that the voltage between the drain and source has returned to normal.

Table 7.13.6 Operation settings for HS2 Vdson high voltage detection (details)

Action setting command VDS2H_OV _op[2:0] 7.18.23	Detection transition	IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH2 - SH2, GL2 - SL	VDSHS2_OV status
“000”	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0
“001”	Detected	INST(H,L)	Operating	Operating	VCP	Operating, Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0 after clearing.
“011”	Detected	Do not care	Operating	Operating	VCP	L, L In H-Bridge mode, GH1, GL1 are also L, L.	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clear.	0 after clearing.
“101”	Detected	Do not care	Stop	Z	VCP	Set all gate drives to RL.	1
	Recovered	INST(H,L)	Resume after clear.	Resume after clear.	VCP	Resume after clearing.	0 after clearing.

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

Table 7.13.7 Operating settings for LS2 Vdson high voltage detection (overview)

Action setting command VDS2L_OV_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation. G: It does not influence the operation. C: It does not influence the operation.
“001”	Detected	R: Set the status register VDSLS2_OV to 1. G: It does not influence the operation. C: It does not influence the operation.
	Recovered	R: Maintain VDSLS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: It does not influence the operation. C: It does not influence the operation.
“010”	-	Reserved. (Note2)
“011”	Detected	R: Set the status register VDSLS2_OV to 1. G: Half-bridge: Stop GDCH2 gate drivers. H-bridge: Stop all gate drivers. C: It does not influence the operation.
	Recovered	R: Maintain VDSLS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: Keep the gate drive stopped. Then, set VDS2_OV_cl to 1 to resume. C: It does not influence the operation.
“100”	-	Reserved. (Note2)
“101”	Detected	R: Set the status register VDSLS2_OV to 1. G: Stop all gate drives. C: Stop the charge pump.
	Recovered	R: Maintain VDSLS2_OV. Then, set the clear command VDS2_OV_cl = 1, which will reset VDSHS2_OV to 0 and VDSLS2_OV to 0. G: Keep the gate drive stopped. Then, set VDS2_OV_cl to 1 to resume. C: Keep the charge pump stopped. Then, set VDS2_OV_cl to1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note1: Please do not use the setting marked as 'Reserved'.

Note2: If you set VDS2L_OV_op to "010" or "100", the gate drive will stop when an abnormality is detected, but there is a phenomenon where operation resumes if it is judged that the voltage between the drain and source has returned to normal.

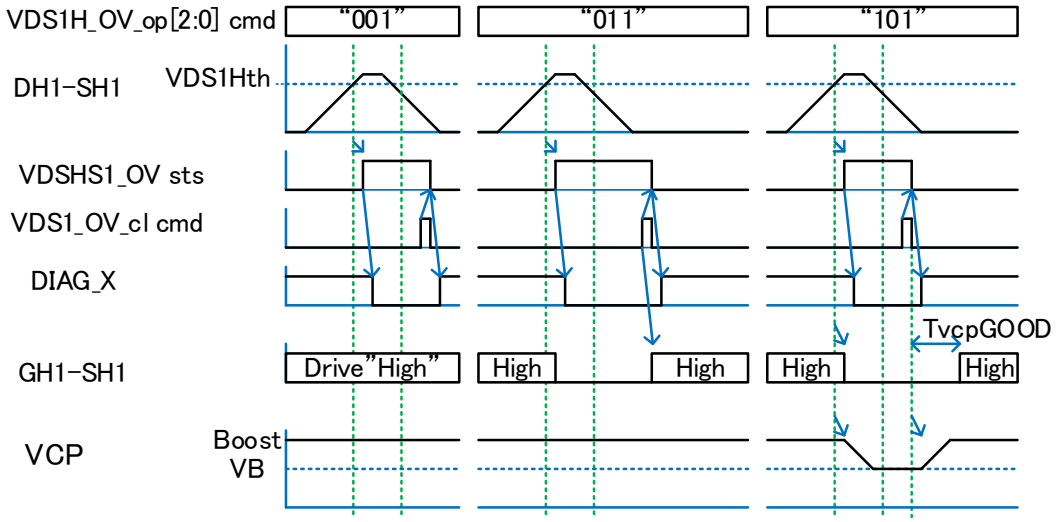
Table 7.13.8 Operation settings for LS2 Vdson high voltage detection (details)

Action setting VDS2L_OV _op[2:0] 7.18.24	Detection transition	IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH2 - SH2, GL2 - SL	VDSLS2_OV status
“000”	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0
“001”	Detected	INST(H,L)	Operating	Operating	VCP	Operating, Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating, Operating	0 after clearing.
“011”	Detected	Do not care	Operating	Operating	VCP	L, L In H-Bridge mode, GH1, GL1 are also L, L.	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clearing.	0 after clearing.
“101”	Detected	Do not care	Stop	Z	VCP	Set all gate drives to RL.	1
	Recovered	INST(H,L)	Resume after clearing.	Resume after clearing.	VCP	Resume after clearing.	0 after clearing.

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance

HS1	LS1
VDS1H_OV_op[2:0] cmd	VDS1L_OV_op[2:0] cmd
DH-SH1	SH1-SL
VDS1Hth[2:0] cmd	VDS1Lth[2:0] cmd
VDSHS1_OV sts	VDSLS1_OV sts
VDS1_OV_cl cmd	
GH1-SH1	GL1-SL

HS2	LS2
VDS2H_OV_op[2:0] cmd	VDS2L_OV_op[2:0] cmd
DH-SH2	SH2-SL
VDS2Hth[2:0] cmd	VDS2Lth[2:0] cmd
VDSHS2_OV sts	VDSLS2_OV sts
VDS2_OV_cl cmd	
GH2-SH2	GL2-SL



Note cmd = Command , sts = Status

Fig. 7.13.1 Operation during high voltage detection of HS1 Vdson.

Fig. 7.13.1 shows the detection of abnormal voltage between the drain and source of the external n-type MOSFET 'HS1' and the recovery behavior for each operation setting. For 'LS1', 'HS2', and 'LS2', please refer to the terminal names, command names, and status names in the table.

7.14. SH1 pin, SH2 pin status detection

The TB9104FTG has a function to detect disconnection of the motor or wiring connected between the SH1 and SH2 terminals using the GDTESTen command.

During this test (GDTESTen=1), the overvoltage detection function during Vds on is also active. Beforehand, set the operation setting commands VDS1H_OV_op, VDS1L_OV_op, VDS2H_OV_op, and VDS2L_OV_op to '011' to stop the gate drive in case of overvoltage, and appropriately set VDS1Hth, VDS1Lth, VDS2Hth, VDS2Lth, t_VDS1fil, t_VDS2fil, tVDS1mask, and tVDS2mask.

Next, when the GDTESTen command is set to 1, the gate driver will turn on one external n-type MOSFET according to the instructions of the GDTEST[1:0] command.

If normal, SH1 and SH2 will change to the battery voltage VB or ground voltage (0V) by the external n-type MOSFET turned on, as shown in Fig. 7.14.1. The voltage of the SH1 and SH2 terminals at this time is measured by the Vds detection comparator. The measured results can be seen in the VDS1Hsts, VDS1Lsts, VDS2Hsts, and VDS2Lsts registers. If there is any abnormality such as disconnection, it may not be as shown in Fig. 7.14.1.

Not only during this test but also at the start of normal operation, if there is a short circuit around the external n-type MOSFET, a large current may flow, causing damage or burning. The TB9104FTG does not have a function to detect short circuits. Please consider taking external measures separately.

Also, the Vds detection results when all external n-type MOSFETs are off vary depending on the external circuit and components of the TB9104FTG. It is recommended to record the Vds detection results when normal and compare them at the start of use.

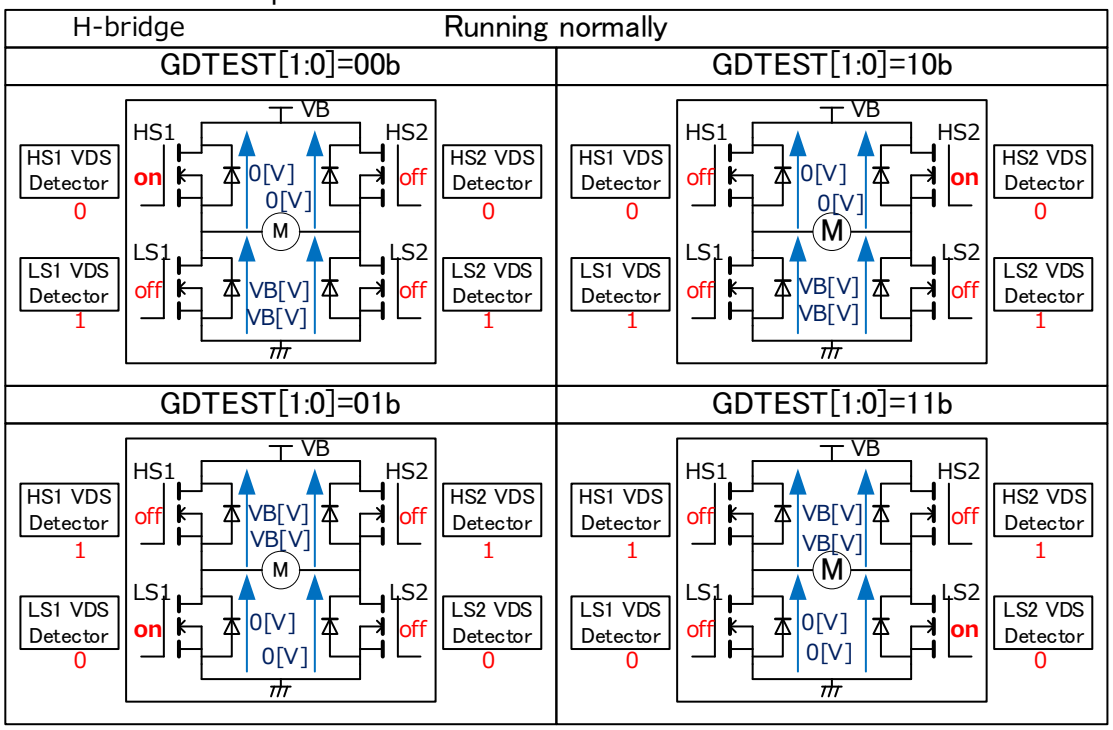


Fig. 7.14.1 SH1 pin, SH2 pin status detection

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.15. Overheating detection circuit

The overheat detection sensor monitors the chip's temperature and detects any temperature rise. If the chip's temperature exceeds the overheat detection temperature TjunctOd, the TB9104FTG determines it as abnormal. If the chip's temperature is lower than TjunctOr, the TB9104FTG determines it as normal.

The overheat detection circuit has a hysteresis TjunctOhys. Additionally, it is equipped with an LPF that only uses signals exceeding the width of TjunctOpw. The operation when overheat is detected can be selected using the operation setting command TJ_OT_op[2:0].

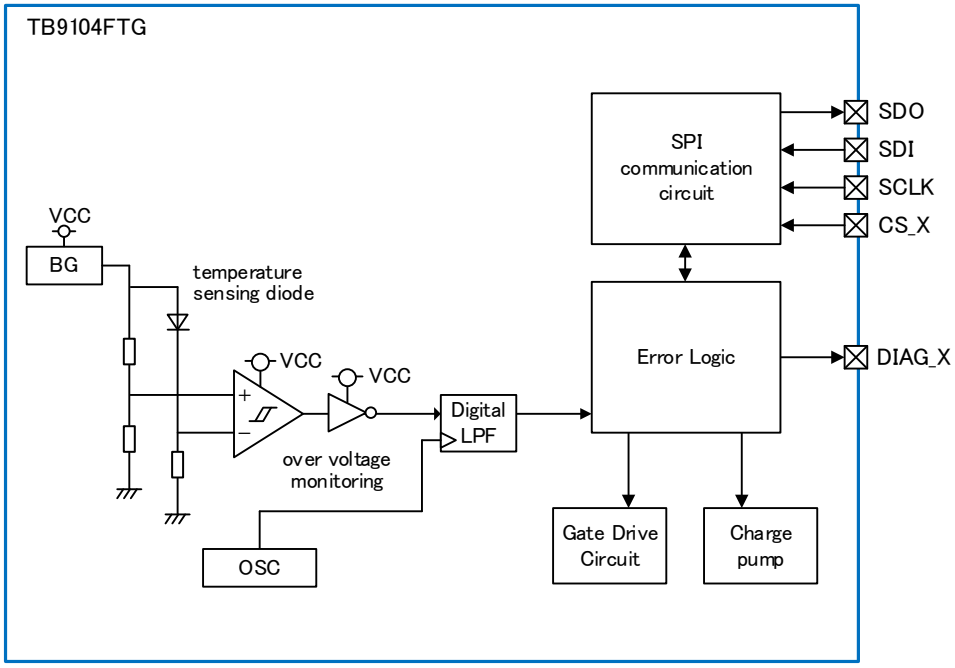


Fig. 7.15.1 Overheating detection circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Table 7.15.1 Operating settings during overheating detection (overview)

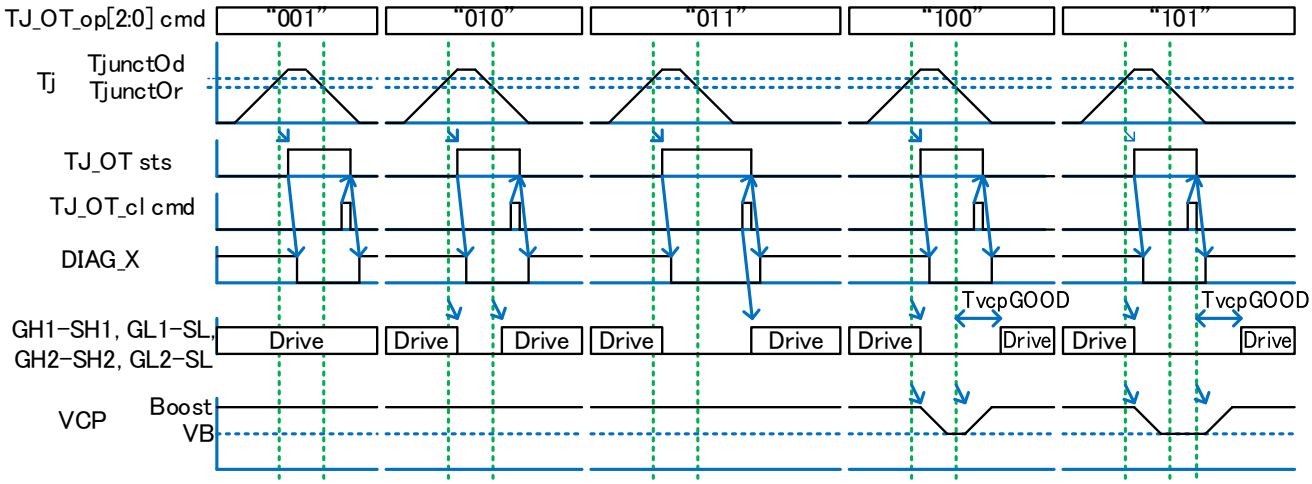
Action setting command TJ_OT_op[2:0]	Detection transition	Operation overview R=Status registers, G=Gate driver, C=Charge pump
“000”	Detected, Recovered	R: It does not influence the operation., G: It does not influence the operation., C: It does not influence the operation.
“001”	Detected	R: Set the status register TJ_OT to 1. , G: It does not influence the operation., C: It does not influence the operation.
	Recovered	R: Maintain TJ_OT = 1. Then set the clear command TJ_OT_cl to 1, which will reset TJ_OT to 0. G: It does not influence the operation., C: It does not influence the operation.
“010”	Detected	R: Set the status register TJ_OT to 1. , G: Stop all gate drivers. , C: It does not influence the operation.
	Recovered	R: Maintain TJ_OT = 1. Then set the clear command TJ_OT_cl to 1, which will reset TJ_OT to 0. G: Quickly Resume gate drive. , C: It does not influence the operation..
“011”	Detected	R: Set the status register TJ_OT to 1. , G: Stop all gate drivers. , C: It does not influence the operation.
	Recovered	R: Maintain TJ_OT = 1. Then set the clear command TJ_OT_cl to 1, which will reset TJ_OT to 0. G: Keep the gate drive stopped. Then, set TJ_OT_cl to 1 to resume. , C: It does not influence the operation..
“100”	Detected	R: Set the status register TJ_OT to 1. , G: Stop all gate drivers. , C: Stop the charge pump.
	Recovered	R: Maintain TJ_OT = 1. Then set the clear command TJ_OT_cl to 1, which will reset TJ_OT to 0. G: Quickly resume gate drive. , C: Quickly resume the charge pump.
“101”	Detected	R: Set the status register TJ_OT to 1. , G: Stop all gate drivers. , C: Stop the charge pump.
	Recovered	R: Maintain TJ_OT = 1. Then set the clear command TJ_OT_cl to 1, which will reset TJ_OT to 0. G: Keep the gate drive stopped. Then, set TJ_OT_cl to 1 to resume. C: Keep the charge pump stopped. Then, set TJ_OT_cl to 1 to resume.
“110”	-	Reserved. Unable to set "110". It results in a SPI error.
“111”	-	Reserved. Unable to set "111". It results in a SPI error.

Note: Please do not use the setting marked as 'Reserved'.

Table 7.15.2 Operating settings during overheating detection (details)

Action setting command TJ_OT_op [2:0] 7.18.16	Detection transition	IN11,IN12, IN21,IN22 pins	Charge Pump	CPDO pin	RPPO pin	GH1-SH1, GL1-SL, GH2-SH2, GL2-SL	TJ_OT status
"000"	Detected, Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0
"001"	Detected	INST(H,L)	Operating	Operating	VCP	Operating	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Operating	0 after clear
"010"	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume	0 after clear
"011"	Detected	Do not care	Operating	Operating	VCP	L, L, L, L	1
	Recovered	INST(H,L)	Operating	Operating	VCP	Resume after clear	0 after clear
"100"	Detected	Do not care	Stop	Z	VCP	RL, RL, RL, RL	1
	Recovered	INST(H,L)	Resume	Resume	VCP	Resume	0 after clear
"101"	Detected	Do not care	Stop	Z	VCP	RL, RL, RL, RL	1
	Recovered	INST(H,L)	Resume after clear	Resume after clear	VCP	Resume after clear	0 after clear

Explanation of symbols: INST=Instructing actions RL = Resistive low H = High L = Low
Z = High-impedance



Note cmd = Command , sts = Status

Fig. 7.15.2 Operation during overheating detection.

7.16. Current sensing circuit

7.16.1. Composition

The TB9104FTG incorporates a reference voltage generation amplifier and a motor current sensing amplifier. The reference voltage generation amplifier generates a reference voltage based on the voltage at the VCC terminal. The motor current sensing amplifier amplifies the differential voltage generated by the current flowing through the shunt resistor connected to the GND side of the external motor drive section. This amplified voltage is output in the direction from the reference voltage to VCC. Note that the motor current that can be sensed is only in the direction from the power supply to GND. The gain can be set via SPI communication. The amplified voltage is output from the AMPO terminal. It is recommended to connect a low-pass filter to the AMPO terminal for noise removal.

By performing calibration when no current is flowing through the motor and correcting the offset variation for each unit, the accuracy of the output voltage can be improved. This expected improvement in accuracy is based on the voltage operating point of the shunt resistor under normal conditions. Connecting resistors to the input terminals may introduce new gain errors. Additionally, it has specified resistance to noise from the VCC power supply and around the shunt resistor.

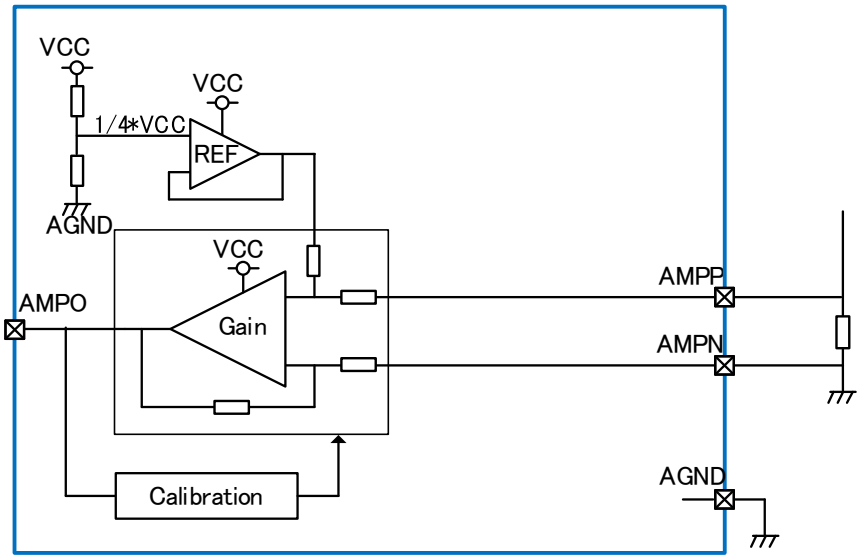


Fig. 7.16.1.1 Current sensing circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.16.2. Offset calibration

Before using the current sense circuit of the TB9104FTG, please perform offset calibration. To ensure proper calibration, set the input differential voltage between the AMPP and AMPN terminals to 0[V] when performing offset calibration. Note that the TB9104FTG does not have a function to automatically connect the AMPP and AMPN terminals.

To execute the calibration, start by setting the CSAcalSTART command to "1" from the SPI. The CSAcalSTART command will automatically return to "0". At this point, the CSAcalibrating status will be set to "1" and the CSAresult status will be "0". Additionally, the gain will be fixed at 30 times. During calibration, the offset correction value CAL_DAT is varied while comparing the amplifier output with one-eighth of the voltage at the VCC terminal to find the optimal value.

When the calibration is complete, set the CSAcalibrating status to "0" and set the calibration result to the CSAresult status. If the CSAresult status is "1", the CAL_DAT is retained and used as the adjustment value. If the CSAresult status is "0", the CAL_DAT is discarded and reset to the initial value.

Setting the CSAresult_cl command to "1" allows you to set the CSAresult status to "0" at any time, but the CAL_DAT is retained. During the period when the CSAcalibrating status is "1", indicating that calibration is in progress, setting the CSAcalSTART command to "1" will be invalid.

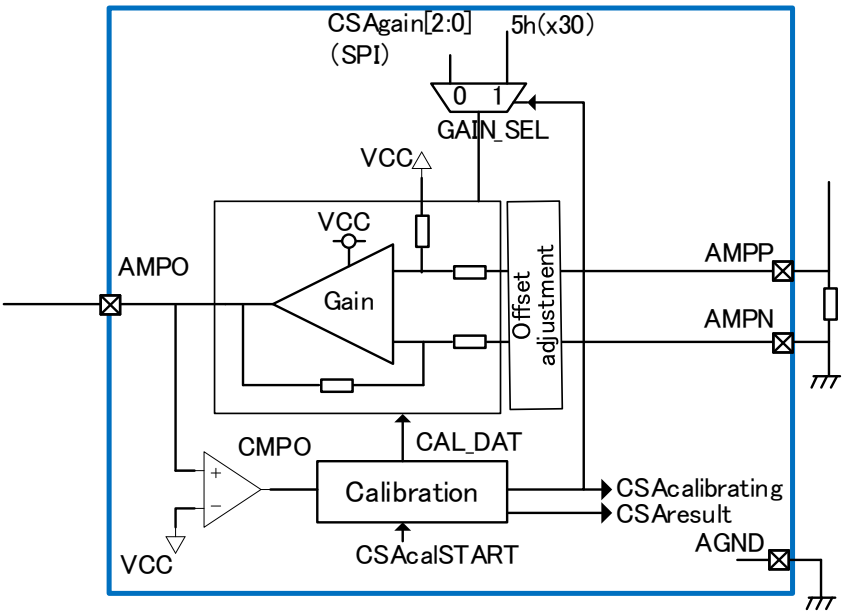


Fig. 7.16.2.1 Current sense amplifier, offset calibration circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

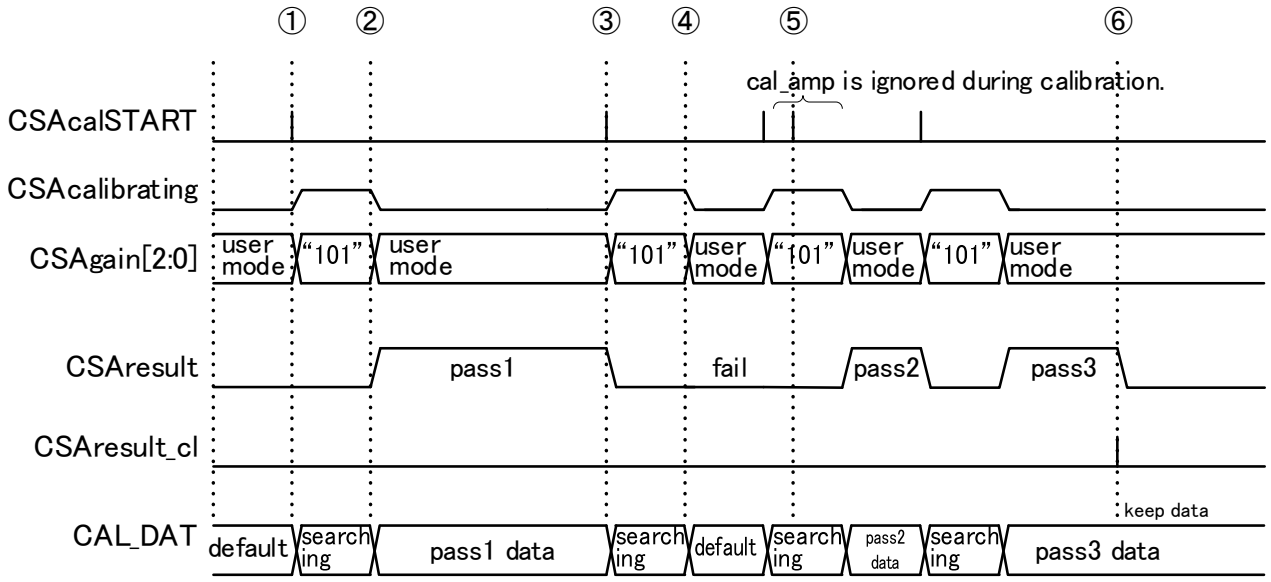


Fig. 7.16.2.2 Current sense amplifier offset calibration waveform

Note: The TB9104FTG does not have a function to automatically connect both the AMPP and AMPN terminals to AGND.

7.17. Control Logic circuit

7.17.1. Half-bridge mode

7.17.1.1. Action description

The TB9104FTG operates as two independent channels in half-bridge mode.

The first half-bridge gate driver GDCH1 is controlled by the signals at the IN11 and IN12 terminals. In half-bridge mode, to prevent the external high-side n-type MOSFET HS1 and low-side n-type MOSFET LS1 from turning on simultaneously, a dead time Tdead (Tdead0 to 7) is automatically inserted when the drive instructions from the IN11 and IN12 terminals are changed, turning off both FETs. To ensure that HS1 and LS1 are not overcurrent, the FET that is turned on monitors the drain-source voltage, excluding the mask time.

The second half-bridge gate driver GDCH2 is controlled by the signals at the IN21 and IN22 terminals. In half-bridge mode, to prevent the external high-side n-type MOSFET HS2 and low-side n-type MOSFET LS2 from turning on simultaneously, a dead time Tdead (Tdead0 to 7) is automatically inserted when the drive instructions from the IN21 and IN22 terminals are changed, turning off both FETs. To ensure that HS2 and LS2 are not overcurrent, the FET that is turned on monitors the drain-source voltage, excluding the mask time.

For unused channels, set the IN terminals to Low. Complete the settings before issuing the on command to the gate driver. Although you can write to the setting registers even while it is on, unexpected behavior may occur in such cases.

7.17.1.2. Truth table

The operating states in half-bridge mode are shown in Table 7.17.1.2.1 and Table 7.17.1.2.2. If the voltage between GH1 and SH1 is RL or Low, the external n-type MOSFET ‘HS1’ is off, and if it is High, it is on. If the voltage between GL1 and SL is RL or Low, the external n-type MOSFET ‘LS1’ is off, and if it is High, it is on. If the voltage between GH2 and SH2 is RL or Low, the external n-type MOSFET ‘HS2’ is off, and if it is High, it is on. If the voltage between GL2 and SL is RL or Low, the external n-type MOSFET ‘LS2’ is off, and if it is High, it is on.

Table 7.17.1.2.1 Truth table for the first half-bridge gate driver GDCH1.

IC internal	Inputs			Outputs		Explanation
Operating state	STBY_X Pin	IN11 Pin	IN12 Pin	GH1- SH1	GL1- SL	
Standby	Low	X	X	RL	RL	TB9104FTG is in the standby state. The drive state is “High-Z”.
Reset	High	X	X	RL	RL	TB9104FTG is in the initial state. The drive state is “High-Z”
Normal operation	High	Low	Low	Low	Low	The drive state is “High-Z”
Normal operation	High	High	Low	High	Low	The drive state is “High”
Normal operation	High	Low	High	Low	High	The drive state is ”Low”
Normal operation	High	High	High	Low	Low	The drive state is “High-Z”

Explanation of symbols:
X = Do not care RL = Resistive low H = High L = Low High-Z = High-impedance

Table 7.17.1.2.2 Truth table for the second half-bridge gate driver GDCH2.

IC internal	Inputs			Outputs		Explanation
Operating state	STBY_X Pin	IN11 Pin	IN12 Pin	GH2- SH2	GL2- SL	
Standby	Low	X	X	RL	RL	TB9104FTG is in the standby state. The drive state is “High-Z”.
Reset	High	X	X	RL	RL	TB9104FTG is in the initial state. The drive state is “High-Z”
Normal operation	High	Low	Low	Low	Low	The drive state is “High-Z”
Normal operation	High	High	Low	High	Low	The drive state is “High”
Normal operation	High	Low	High	Low	High	The drive state is ”Low”
Normal operation	High	High	High	Low	Low	The drive state is “High-Z”

Explanation of symbols:
X = Do not care RL = Resistive low H = High L = Low High-Z = High-impedance

7.17.1.3. Current Path

In the TB9104FTG, the current path of the external n-type MOSFET used in half-bridge mode is shown in Fig. 7.17.1.3.1. The solid line indicates the current path during drive operation. The dotted line indicates the path of the regenerative current.

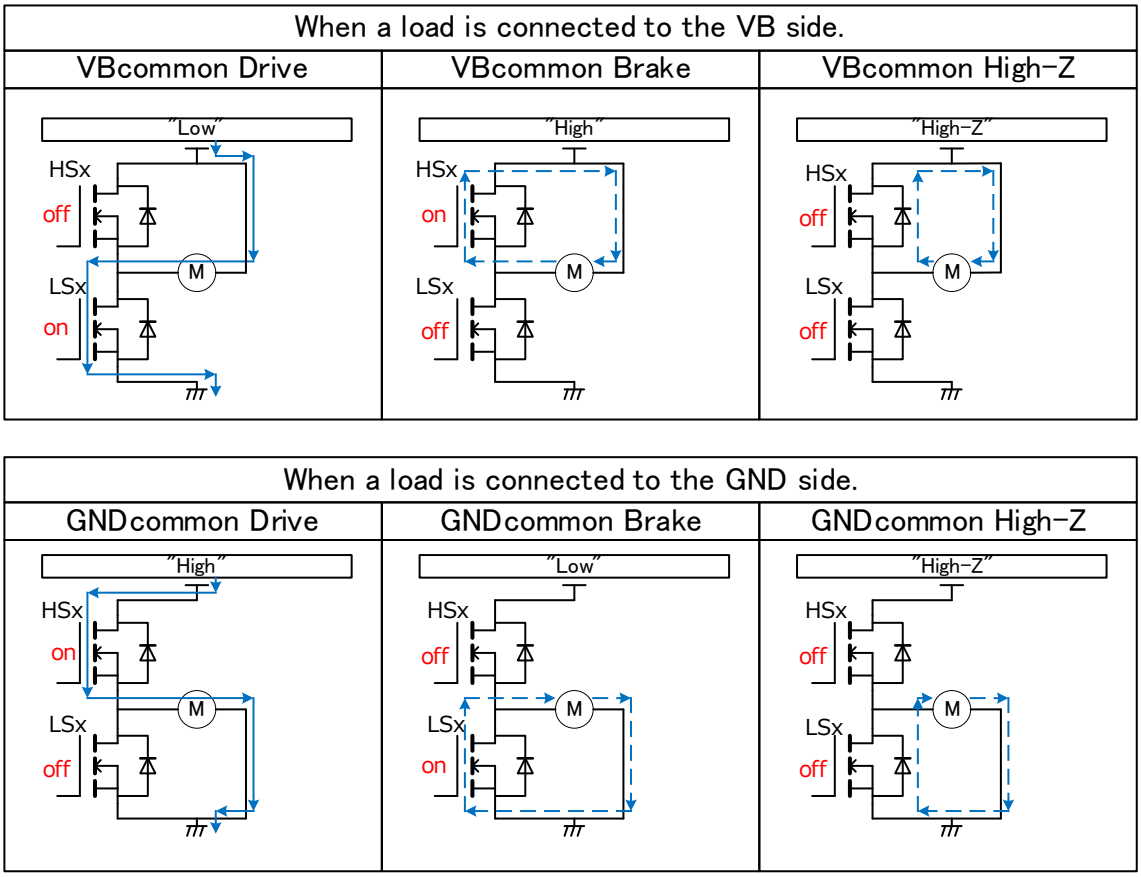


Fig. 7.17.1.3.1 Current path in half-bridge mode

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.17.1.4. Drive Control Flowchart

The drive control flowchart in half-bridge mode is shown in Fig. 7.17.1.4.1. Additionally, the combinations of drive control not described in Fig. 7.17.1.4.1 are shown in Fig. 7.17.1.4.2.

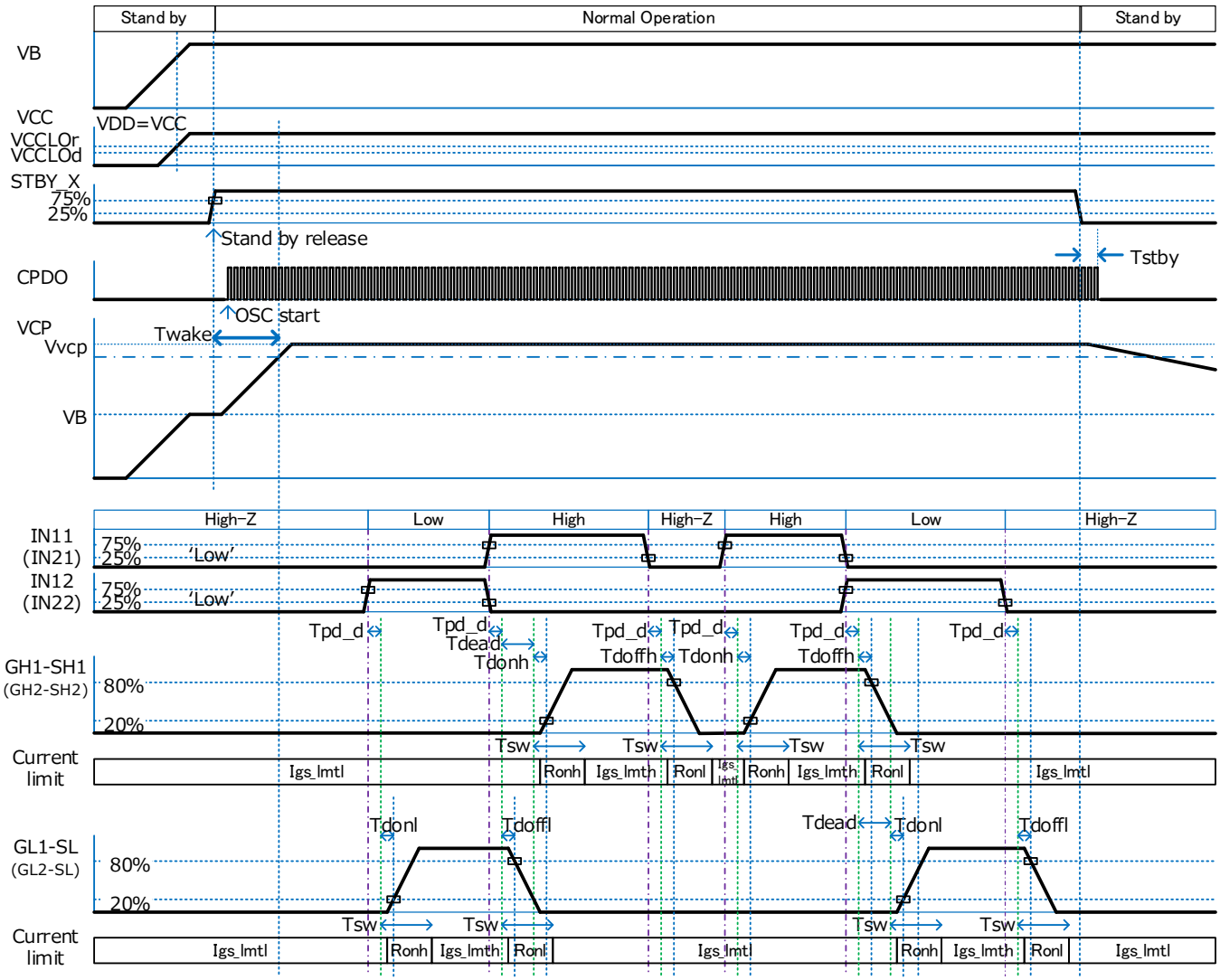


Fig. 7.17.1.4.1 Half Bridge Flowchart 1 (per channel)

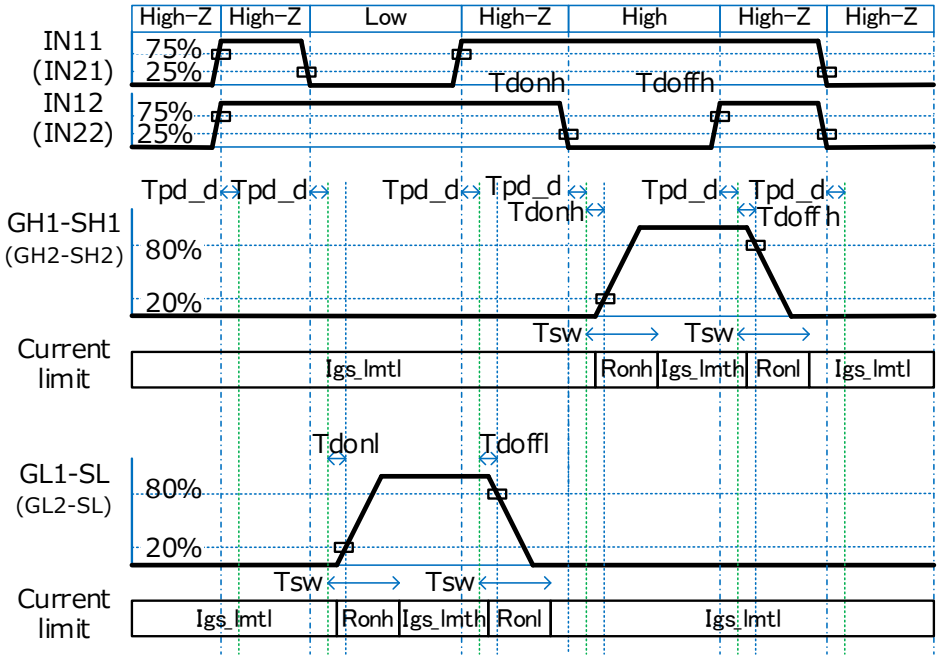


Fig. 7.17.1.4.2 Half-bridge flowchart 2 other drive control combinations

7.17.2. H-bridge mode

7.17.2.1. Action description

In H-Bridge mode, the TB9104FTG operates as a single-channel H-Bridge. Control is performed via the IN11 and IN12 terminals. It is desirable to connect the IN21 and IN22 terminals to GND. In H-bridge mode, dead time is automatically inserted when the drive instructions via the IN11 and IN12 terminals are changed to prevent HS1 and LS1, and HS2 and LS2 from being simultaneously turned on and causing shoot-through current.

To ensure that HS1 and LS1 are not overcurrent, the FET that is turned on monitors the drain-source voltage, excluding the mask time.

Complete the settings before issuing the on command to the gate driver. Although you can write to the setting registers even while it is on, unexpected behavior may occur in such cases.

7.17.2.2. Truth table

The operating states in H-Bridge mode are shown in Table 7.17.2.2.1. If the voltage between GH1 and SH1 is RL or Low, the external n-type MOSFET ‘HS1’ is off, and if it is High, it is on. If the voltage between GL1 and SL is RL or Low, the external n-type MOSFET ‘LS1’ is off, and if it is High, it is on. If the voltage between GH2 and SH2 is RL or Low, the external n-type MOSFET ‘HS2’ is off, and if it is High, it is on. If the voltage between GL2 and SL is RL or Low, the external n-type MOSFET ‘LS2’ is off, and if it is High, it is on.

Table 7.17.2.2.1 H-bridge mode truth table

IC internal	Inputs			Outputs				Explanation
Operation state	STBY_X	IN11	IN12	GH1 - SH1	GL1 - SL	GH2 - SH2	GL2 - SL	
Standby	Low	X	X	RL	RL	RL	RL	TB9104FTG is in the standby state. The drive state is “High-Z” .
Reset	High	X	X	RL	RL	RL	RL	TB9104FTG is in the initial state. The drive state is “High-Z” .
Normal operation	High	Low	Low	Low	Low	Low	Low	The drive state is “High-Z” .
Normal operation	High	High	Low	High	Low	Low	High	The drive state is ”Forward drive(SH1 to SH2)” .
Normal operation	High	Low	High	Low	High	High	Low	The drive state is ”Reverse drive(SH2 to SH1)” .
Normal operation	High	High	High	Low	High	Low	High	The drive state is ”Brake” .

Explanation of symbols:
X = Do not care RL = Resistive low H = High L = Low High-Z = High-impedance

7.17.2.3. Current Path

In H-Bridge mode, the current path of the external n-type MOSFETs used in the TB9104FTG is shown in Fig. 7.17.2.3.1. The red solid lines indicate the current path during forward drive, and the blue solid lines indicate the current path during reverse drive. Additionally, the dotted lines indicate the path of the regenerative current during forward drive, and the double-dashed lines indicate the current path during reverse drive.

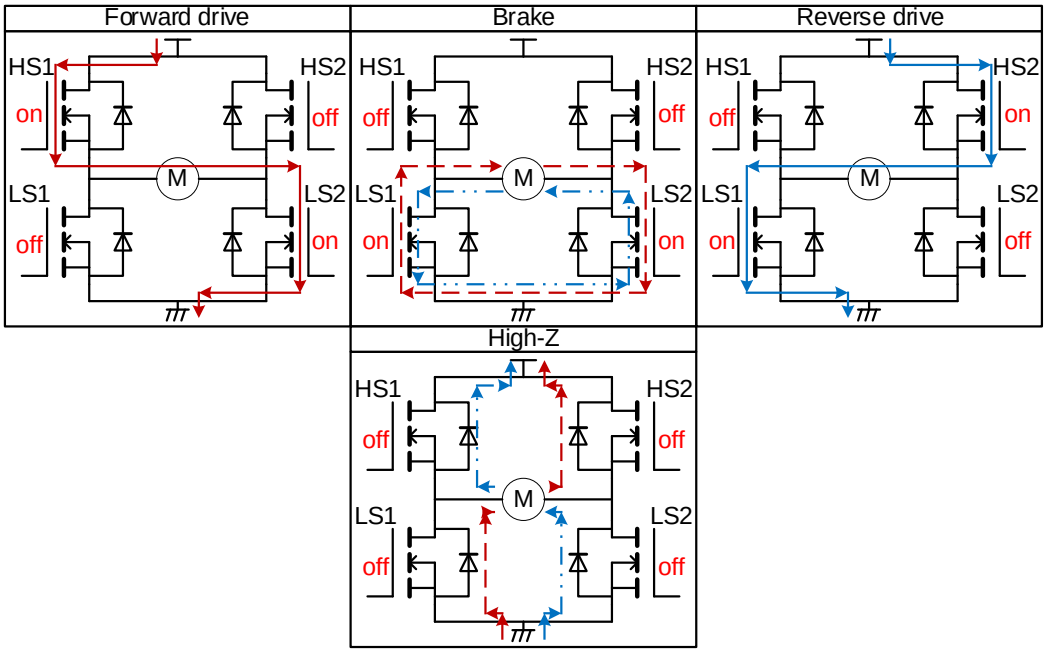


Fig. 7.17.2.3.1 Current path in H-bridge mode

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.17.2.4. Drive Control Flowchart

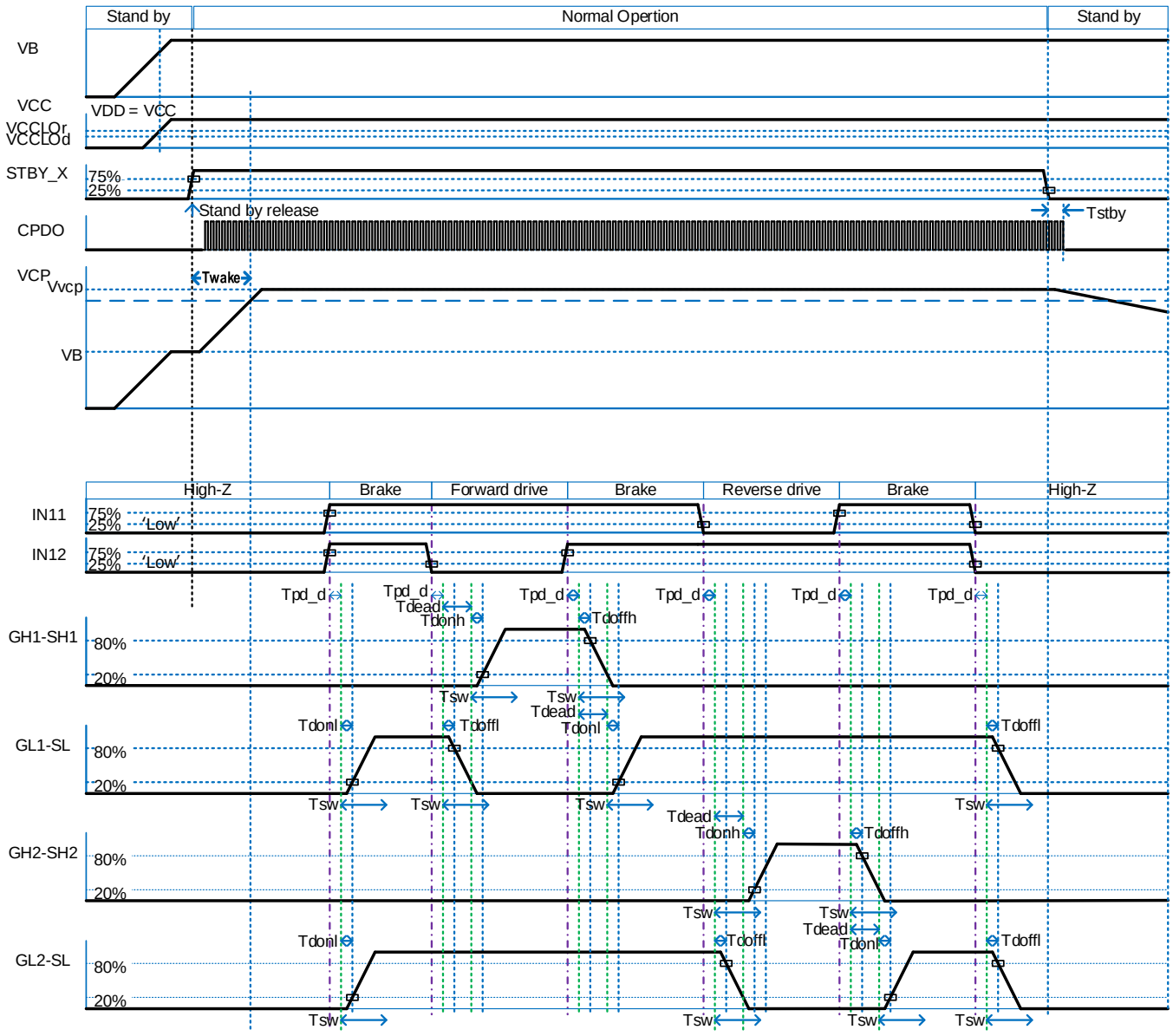


Fig. 7.17.2.4.1 H Bridge Flowchart 1

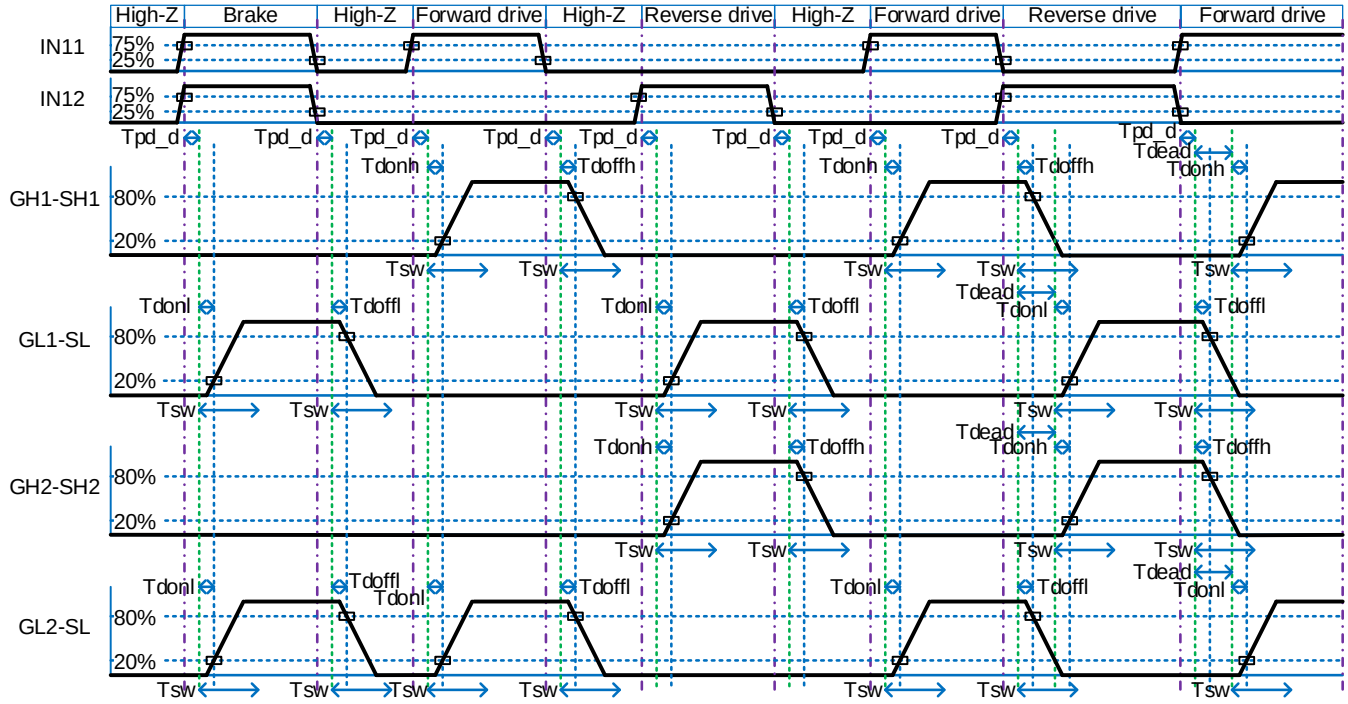


Fig. 7.17.2.4.2 H-bridge flowchart 2 other drive control combinations

7.17.3. Fault processing

The TB9104FTG is equipped with various abnormality detection functions. If you select an option other than ‘Do not detect’ for the handling method when an abnormality is detected, the DIAG_X terminal will be set to Low when an abnormality occurs. The DIAG_X terminal goes Low if any of the abnormality detection flag registers have a value of 1 (High). Additionally, depending on the operation setting commands for each abnormality detection, it will handle stopping the gate drive and stopping the charge pump.

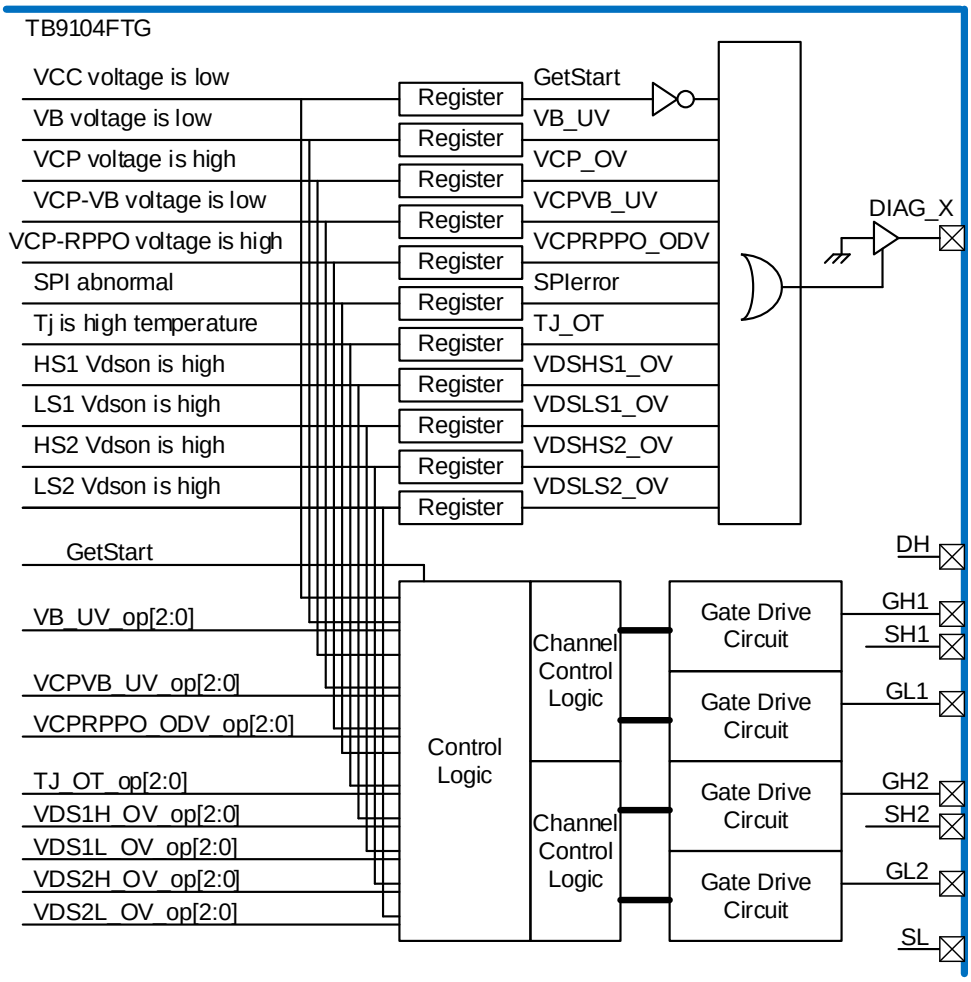


Fig. 7.17.3.1 Fault processing and diagnostics

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

7.18. SPI Register Maps

Table 7.18.1 Register Maps

	Bit15	Bit14	Bit13	Bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Register name	**A[3]**	**A[2]**	**A[1]**	**A[0]**	**RD+ /WR-**	**D[9]**	**D[8]**	**D[7]**	**D[6]**	**D[5]**	**D[4]**	**D[3]**	**D[2]**	**D[1]**	**D[0]**	**EvenP**
FAULT STATUS	0000b				Write	GetStart	VB_UV_cl	0	VCP_OV_cl	VCPVB_UV_cl	VCPRPPO_ODV_cl	SPIerror_cl	TJ_OT_cl	0	0	
					Read	GetStart	VB_UV	0	VCP_OV	VCPVB_UV	VCPRPPO_ODV	SPIerror	TJ_OT	0	WKUP_sts	
					Init Value	0	0	0	0	0	0	0	0	0	0	
FAULT VDS	0001b				Write	VDS1_OV_cl	0	VDS2_OV_cl	0	0	0	0	0	0	0	
					Read	VDSHS1_OV	VDSLS1_OV	VDSHS2_OV	VDSLS2_OV	0	0	0	0	0	0	
					Init Value	0	0	0	0	0	0	0	0	0	0	
SET1	0010b				Write	VB_UV_op[2:0]			0	0	0	0	0	0	0	
					Read	VB_UV_op[2:0]			0	0	0	0	0	0	0	
					Init Value	100b			0	0	0	0	0	0	0	
SET2	0011b				Write	VCPVB_UV_op[2:0]			VCPRPPO_ODV_op[2:0]			TJ_OT_op[2:0]			0	
					Read	VCPVB_UV_op[2:0]			VCPRPPO_ODV_op[2:0]			TJ_OT_op[2:0]			0	
					Init Value	010b			101b			101b			0	
SET VDS1_1	0100b				Write	VDS1H_OV_op[2:0]			VDS1L_OV_op[2:0]			tVDS1mask[2:0]			0	
					Read	VDS1H_OV_op[2:0]			VDS1L_OV_op[2:0]			tVDS1mask[2:0]			0	
					Init Value	011b			011b			001b			0	
SET VDS1_2	0101b				Write	VDS1Hth[2:0]			VDS1Lth[2:0]			t_VDS1fil[1:0]		0	0	
					Read	VDS1Hth[2:0]			VDS1Lth[2:0]			t_VDS1fil[1:0]		0	0	
					Init Value	011b			011b			11b		0	0	
SET VDS2_1	0110b				Write	VDS2H_OV_op[2:0]			VDS2L_OV_op[2:0]			tVDS2mask[2:0]			0	
					Read	VDS2H_OV_op[2:0]			VDS2L_OV_op[2:0]			tVDS2mask[2:0]			0	

		Init Value	011b			011b			001b			0		
SET VDS2_2	0111b	Write	VDS2Hth[2:0]			VDS2Lth[2:0]			t_VDS2fil[1:0]		0	0		
		Read	VDS2Hth[2:0]			VDS2Lth[2:0]			t_VDS2fil[1:0]		0	0		
		Init Value	011b			011b			11b		0	0		
SETtime	1000b	Write	t_ilim[2:0]			0	0	0	t_deadt[2:0]			0		
		Read	t_ilim[2:0]			0	0	0	t_deadt[2:0]			0		
		Init Value	110b			0	0	0	010b			0		
CSA_1	1001b	Write	CSAgain[2:0]			CSAcalSTART	CSAresult_cl	0	0	0	0	0		
		Read	CSAgain[2:0]			CSAcalibratng	CSAresult	0	0	0	0	0		
		Init Value	011b			0	0	0	0	0	0	0		
RESET	1010b	Write	REGreset	0	0	0	0	0	0	0	0	0		
		Read	0	0	0	0	0	0	0	0	0	0		
		Init Value	0	0	0	0	0	0	0	0	0	0		
GD_TEST	1011b	Write	GDTESTen	GDTEST[1:0]		0	0	0	0	0	0	0		
		Read	GDTESTen	GDTEST[1:0]		VDS1Hsts	VDS1Lsts	VDS2Hsts	VDS2Lsts	0	0	0		
		Init Value	0	00b		VDS1Hsts	VDS1Lsts	VDS2Hsts	VDS2Lsts	0	0	0		
INspi	1100b	Write	INspiSEL	INspi11	INspi12	INspi21	INspi22	PWMEN	0	0	0	Half-bridge mode		
		Read	INspiSEL	INspi11	INspi12	INspi21	INspi22	PWMEN	0	0	0	Half-bridge mode		
		Init Value	0	0	0	0	0	0	0	0	0	0		
PWMCNT	1101b	Write	PWMCNT[9:0]											
		Read	PWMCNT[9:0]											
		Init Value	00_1100_0111b											
PWMDT	1110b	Write	PWMDT[9:0]											
		Read	PWMDT[9:0]											
		Init Value	00_0110_0011b											
NOP	1111b	Write	Do not care(0 or 1)											
		Read	00_0000_0000b											
		Init Value	00_0000_0000b											

Note: Unassigned bits will be discarded if written to. When read, they will return 0.

7.18.1. Address=0000b, D[9] “GetStart”

Write	GetStart	Writing a 1 will set it to 1. Writing a 0 will have no effect.
Read	GetStart	Initial value=0

GetStart=0: This indicates that it has just been initialized. Except for this register, all other registers cannot be written to. They can be read. The gate driver will be in the off state.

GetStart=1: This indicates normal operating conditions. You can write to and read from each register. Writing a 0 to this register has no effect. Writing a 1 to the REGreset register will set this register to 0.

7.18.2. Address=0000b, D[8] “VB_UV_cl”, “VB_UV”

Write	VB_UV_cl	When VvbUr < Vvb, writing a 1 will set VB_UV to 0. Writing a 0 will have no effect.
Read	VB_UV	Initial value=0

VB_UV_cl register. Write-only. When the voltage at the VB terminal is greater than or equal to VvbUr, writing a 1 will set the VB_UV register to 0. This command will then return to 0 by itself after a short time.

VB_UV register. Read-only. VB_UV = 1 indicates that the voltage at the VB terminal has fallen below VvbUd.

7.18.3. Address=0000b, D[6] “VCP_OV_cl”, “VCP_OV”

Write	VCP_OV_cl	When Vvcp < VvcpOr, writing a 1 will set VCP_OV to 0. Writing a 0 will have no effect.
Read	VCP_OV	Initial value=0

VCP_OV_cl register. Write-only. When the voltage at the VCP terminal is less than or equal to VvcpOr, writing a 1 will set the VCP_OV register to 0. This command will then return to 0 by itself after a short time.

VCP_OV register. Read-only. VCP_OV = 1 indicates that the voltage at the VCP terminal has exceeded VvcpOd.

7.18.4. Address=0000b, D[5] “VCPVB_UV_cl”, “VCPVB_UV”

Write	VCPVB_UV_cl	When VvcpvbUr < (Vvcp - Vvb), writing a 1 will set VCPVB_UV to 0. Writing a 0 will have no effect.
Read	VCPVB_UV	Initial value=0

VCPVB_UV_cl register. Write-only. When the voltage between the VCP and VB terminals is greater than or equal to VvcpvbUr, writing a 1 will set the VCPVB_UV register to 0. This command will then return to 0 by itself after a short time.

VCPVB_UV register. Read-only. VCPVB_UV = 1 indicates that the voltage between the VCP and VB terminals has fallen below VvcpvbUd.

7.18.5. Address=0000b D[4] “VCPRPPO_ODV_cl”, “VCPRPPO_ODV”

Write	VCPRPPO_ODV_cl	When (Vvcp - Vrppo) < VvcprppoOr, writing a 1 will set VCPRPPO_ODV to 0. Writing a 0 will have no effect.
Read	VCPRPPO_ODV	Initial value=0

VCPRPPO_ODV_cl register. Write-only. When the voltage between the VCP and RPPO terminals is less than or equal to VvcprppoOr, writing a 1 will set the VCPRPPO_ODV register to 0. This command will then return to 0 by itself after a short time.

VCPRPPO_ODV register. Read-only. VCPRPPO_ODV = 1 indicates that the voltage between the VCP and RPPO terminals has exceeded VvcprppoOd.

7.18.6. Address=0000b D[3] “SPIerror_cl”, “SPIerror”

Write	SPIerror_cl	Writing a 1 will set SPIerror to 0. Writing a 0 will have no effect.
Read	SPIerror	Initial value=0

SPIerror_cl register. Write-only. Writing a 1 during normal SPI communication will set the SPIerror register to 0. This command will then return to 0 by itself after a short time.

SPIerror register. Read-only. SPIerror = 1 indicates that there was abnormal SPI communication in the

past.

7.18.7. Address=0000b D[2] “TJ_OT_cl”, “TJ_OT”

Write	TJ_OT_cl	When Tj<TjunctOr, writing a 1 will set TJ_OT to 0. Writing a 0 will have no effect.
Read	TJ_OT	Initial value=0

"TJ_OT_cl" register. Write only. When the junction temperature of TB9104FTG is below TjunctOr, writing a 1 will set the "TJ_OT" register to 0. This command will then return to 0 by itself after a short time.

"TJ_OT" register. Read only. "TJ_OT" = 1 indicates that the temperature of TB9104FTG has exceeded TjunctOd.

7.18.8. Address=0000b D[0] “WKUP_sts”

Write	0	-
Read	WKUP_sts	Initial value=0

The ‘WKUP_sts’ register is read-only. It indicates that the TB9104FTG is in the wake-up period (Twake period and TvcpGOOD period) and cannot drive the gate.

7.18.9. Address=0001b D[9] “VDS1_OV_cl”, “VDSHS1_OV”

Write	VDS1_OV_cl	When the Vdson of the external MOSFETs HS1 and LS1 is normal, writing a 1 will sets VDSHS1_OV and VDSLS1_OV to 0. Writing a 0 will have no effort.
Read	VDSHS1_OV	Initial value=0

“VDS1_OV_cl” Register: Write-only. When there is no abnormality in the drain-source voltage of the external n-type MOSFETs HS1 and LS1 when they are on, writing 1 will set the “VDSHS1_OV” and “VDSLS1_OV” registers to 0. It will then return to 0 by itself after a short time.

“VDSHS1_OV” Register: Read-only. “VDSHS1_OV” = 1 indicates that the drain-source voltage of the external n-type MOSFET HS1 exceeded the set value when it was turned on.

7.18.10. Address=0001b D[8] “VDSLS1_OV”

Write	0	-
Read	VDSLS1_OV	Initial value=0

“VDSLS1_OV” Register: This is a read-only register. “VDSLS1_OV” = 1 indicates that the drain-source voltage of the external n-type MOSFET LS1 exceeded the set value when it was turned on.

7.18.11. Address=0001b D[7] “VDS2_OV_cl”, “VDSHS2_OV”

Write	VDS2_OV_cl	When the Vdson of the external n-type MOSFETs HS2 and LS2 is normal, writing 1 sets VDSHS2_OV to 0 and VDSLS2_OV. Writing 0 does nothing.
Read	VDSHS2_OV	Initial value=0

“VDS2_OV_cl” Register: This is a write-only register. When there is no abnormality in the drain-source voltage of the external n-type MOSFETs HS2 and LS2 when they are on, writing 1 sets the “VDSHS2_OV” and “VDSLS2_OV” registers to 0. They will then return to 0 on their own after a short period.

“VDSHS2_OV” Register: This is a read-only register. “VDSHS2_OV” = 1 indicates that the drain-source voltage of the external n-type MOSFET HS2 exceeded the set value when it was turned on.

7.18.12. Address=0001b D[6] “VDSLS2_OV”

Write	0	-
Read	VDSLS2_OV	Initial value=0

“VDSLS2_OV” Register: This is a read-only register. “VDSLS2_OV” = 1 indicates that the drain-source voltage of the external n-type MOSFET LS2 exceeded the set value when it was turned on.

7.18.13. Address=0010b D[9:7] “VB_UV_op[2:0]”

Write	VB_UV_op[2:0]	Table 7.6.1Table 7.6.2
Read	VB_UV_op[2:0]	Initial value=100b

“VB_UV_op[2:0]” Register: This register sets the operation when a low voltage is detected at the VB terminal. For details, refer to Table 7.6.1.

7.18.14. Address=0011b D[9:7] “VCPVB_UV_op[2:0]”

Write	VCPVB_UV_op[2:0]	Table 7.10.2.1 and Table 7.10.2.2
Read	VCPVB_UV_op[2:0]	Initial value=010b

“VCPVB_UV_op[2:0]” Register: This register sets the operation when a low voltage is detected between the VCP terminal and the VB terminal. For details, refer to Table 7.10.2.1 and Table 7.10.2.2.

7.18.15. Address=0011b D[6:4] “VCPRPPO_ODV_op[2:0]”

Write	VCPRPPO_ODV_op[2:0]	Table 7.11.1.1 and Table 7.11.1.2
Read	VCPRPPO_ODV_op[2:0]	Initial value=101b

“VCPRPPO_ODV_op[2:0]” Register: This register sets the operation when a high voltage is detected between the VCP terminal and the RPPO terminal. For details, refer to Table 7.11.1.1 and Table 7.11.1.2.

7.18.16. Address=0011b D[3:1] “TJ_OT_op[2:0]”

Write	TJ_OT_op[2:0]	Table 7.15.1 and Table 7.15.2
Read	TJ_OT_op[2:0]	Initial value=101b

“TJ_OT_op[2:0]” Register: This register sets the operation when a high junction temperature is detected in the TB9104FTG. For details, refer to Table 7.15.1 and Table 7.15.2.

7.18.17. Address=0100b D[9:7] “VDS1H_OV_op[2:0]”

Write	VDS1H_OV_op[2:0]	Table 7.13.1 and Table 7.13.2
Read	VDS1H_OV_op[2:0]	Initial value=011b

“VDS1H_OV_op[2:0]” Register: This register sets the operation when a high voltage is detected between the DH terminal and the SH1 terminal while the external n-type MOSFET connected to the GH1 terminal is on. For details, refer to Table 7.13.1 and Table 7.13.2.

7.18.18. Address=0100b D[6:4] “VDS1L_OV_op[2:0]”

Write	VDS1L_OV_op[2:0]	Table 7.13.3 and Table 7.13.4
Read	VDS1L_OV_op[2:0]	Initial value=011b

“VDS1L_OV_op[2:0]” Register: This register sets the operation when a high voltage is detected between the SH1 terminal and the SL terminal while the external n-type MOSFET connected to the GL1 terminal is on. For details, refer to Table 7.13.3 and Table 7.13.4.

7.18.19. Address=0100b D[3:1] “tVDS1mask[2:0]”

Write	tVDS1mask[2:0]	Refer to the table below.
Read	tVDS1mask[2:0]	Initial value=001b

“tVDS1mask[2:0]” Register: This register sets the time during which high voltage detection of Vds on is temporarily disabled until stable output is achieved when the gate drive command is changed in channel 1.

-	t_VDS1fil[1:0] = 00b (1µs)	t_VDS1fil[1:0] = 01b (2µs)	t_VDS1fil[1:0] = 10b (4µs)	t_VDS1fil[1:0] = 11b (8µs)
tVDS1mask[2:0]	**Mask time**	**Mask time**	**Mask time**	**Mask time**
000b	7µs	8µs	10µs	14µs
001b	8µs	9µs	11µs	15µs
010b	9µs	10µs	12µs	16µs
011b	10µs	11µs	13µs	17µs
100b	11µs	12µs	14µs	18µs
101b	12µs	13µs	15µs	19µs
110b	14µs	15µs	17µs	21µs
111b	16µs	17µs	19µs	23µs

7.18.20. Address=0101b D[9:7] “VDS1Hth[2:0]”

Write	VDS1Hth[2:0]	Refer to the table below.
Read	VDS1Hth[2:0]	Initial value=011b

“VDS1Hth[2:0]” Register: This register sets the threshold voltage of the voltage detection comparator between the DH terminal and the SH1 terminal.

VDS1Hth[2:0]	Threshold voltage
000b	0.1V
001b	0.3V
010b	0.5V
011b	0.7V
100b	0.9V
101b	1.1V
110b	1.3V
111b	1.5V

7.18.21. Address=0101b D[6:4] “VDS1Lth[2:0]”

Write	VDS1Lth[2:0]	Refer to the table below.
Read	VDS1Lth[2:0]	Initial value=011b

“VDS1Lth[2:0]” Register: This register sets the threshold voltage of the voltage detection comparator between the SH1 terminal and the SL terminal.

VDS1Lth[2:0]	Threshold voltage
000b	0.1V
001b	0.3V
010b	0.5V
011b	0.7V
100b	0.9V
101b	1.1V
110b	1.3V
111b	1.5V

7.18.22. Address=0101b D[3:2] “t_VDS1fil[1:0]”

Write	t_VDS1fil[1:0]	Refer to the table below.
Read	t_VDS1fil[1:0]	Initial value=11b

“t_VDS1fil[1:0]” Register: This register sets the cutoff pulse width for the LPF of the output signal from the voltage detection comparator between the DH terminal and the SH1 terminal, as well as the LPF of the output signal from the voltage detection comparator between the SH1 terminal and the SL terminal.

t_VDS1fil[1:0]	Cut-off pulse width
00b	1μs
01b	2μs
10b	4μs
11b	8μs

7.18.23. Address=0110b D[9:7] “VDS2H_OV_op[2:0]”

Write	VDS2H_OV_op[2:0]	Table 7.13.5 and Table 7.13.6
Read	VDS2H_OV_op[2:0]	Initial value=011b

“VDS2H_OV_op[2:0]” Register: This register sets the operation when a high voltage is detected between the DH terminal and the SH2 terminal while the external n-type MOSFET connected to the GH2 terminal is on. For details, refer to Table 7.13.5 and Table 7.13.6.

7.18.24. Address=0110b D[6:4] “VDS2L_OV_op[2:0]”

Write	VDS2L_OV_op[2:0]	Table 7.13.7 and Table 7.13.8
Read	VDS2L_OV_op[2:0]	Initial value=011b

“VDS2L_OV_op[2:0]” Register: This register sets the operation when a high voltage is detected between the SH2 terminal and the SL terminal while the external n-type MOSFET connected to the GL2 terminal is on. For details, refer to Table 7.13.7 and Table 7.13.8.

7.18.25. Address=0110b D[3:1] “tVDS2mask[2:0]”

Write	tVDS2mask[2:0]	Refer to the table below.
Read	tVDS2mask[2:0]	Initial value=001b

“tVDS2mask[2:0]” Register: This register sets the time during which high voltage detection of Vds on is temporarily disabled until stable output is achieved when the gate drive command is changed in channel 2.

-	t_VDS2fil[1:0] = 00b (1µs)	t_VDS2fil[1:0] = 01b (2µs)	t_VDS2fil[1:0] = 10b (4µs)	t_VDS2fil[1:0] = 11b (8µs)
tVDS2mask[2:0]	**Mask time**	**Mask time**	**Mask time**	**Mask time**
000b	7µs	8µs	10µs	14µs
001b	8µs	9µs	11µs	15µs
010b	9µs	10µs	12µs	16µs
011b	10µs	11µs	13µs	17µs
100b	11µs	12µs	14µs	18µs
101b	12µs	13µs	15µs	19µs
110b	14µs	15µs	17µs	21µs
111b	16µs	17µs	19µs	23µs

7.18.26. Address=0111b D[9:7] “VDS2Hth[2:0]”

Write	VDS2Hth[2:0]	Refer to the table below.
Read	VDS2Hth[2:0]	Initial value=011b

“VDS2Hth[2:0]” Register: This register sets the threshold voltage of the voltage detection comparator between the DH terminal and the SH2 terminal.

VDS2Hth[2:0]	Threshold voltage
000b	0.1V
001b	0.3V
010b	0.5V
011b	0.7V
100b	0.9V
101b	1.1V
110b	1.3V
111b	1.5V

7.18.27. Address=0111b D[6:4] “VDS2Lth[2:0]”

Write	VDS2Lth[2:0]	Refer to the table below.
Read	VDS2Lth[2:0]	Initial value=011b

“VDS2Lth[2:0]” Register: This register sets the threshold voltage of the voltage detection comparator between the SH2 terminal and the SL terminal.

VDS2Lth[2:0]	Threshold voltage
000b	0.1V
001b	0.3V
010b	0.5V
011b	0.7V
100b	0.9V
101b	1.1V
110b	1.3V
111b	1.5V

7.18.28. Address=0111b D[3:2] “t_VDS2fil[1:0]”

Write	t_VDS2fil[1:0]	Refer to the table below.
Read	t_VDS2fil[1:0]	Initial value=11b

“t_VDS2fil[1:0]” Register: This register sets the cutoff pulse width for the LPF of the output signal from the voltage detection comparator between the DH terminal and the SH2 terminal, as well as the LPF of the output signal from the voltage detection comparator between the SH2 terminal and the SL terminal.

t_VDS2fil[1:0]	Cut-off pulse width
00b	1μs
01b	2μs
10b	4μs
11b	8μs

7.18.29. Address=1000b D[9:7] “t_ilim[2:0]”

Write	t_ilim[2:0]	Refer to the table below.
Read	t_ilim[2:0]	Initial value=110b

“t_ilim[2:0]” Register: This register sets the time at which the gate driver’s output current begins to be limited.

t_ilim[2:0]	current limit start time
000b	6μs
001b	8μs
010b	10μs
011b	12μs
100b	16μs
101b	32μs
110b	64μs
111b	Do not start

7.18.30. Address=1000b D[3:1] “t_deadt[2:0]”

Write	t_deadt[2:0]	Refer to the table below.
Read	t_deadt[2:0]	Initial value=010b

“t_deadt[2:0]” Register: This command sets a time delay to prevent shoot-through current between the high-side and low-side in external n-type MOSFETs.

t_deadt[2:0]	dead time
000b	1 clock
001b	2 clocks
010b	3 clocks
011b	4 clocks
100b	5 clocks
101b	6 clocks
110b	7 clocks
111b	8 clocks

7.18.31. Address=1001b D[9:7] “CSAgain[2:0]”

Write	CSAgain[2:0]	Refer to the table below.
Read	CSAgain[2:0]	Initial value=011b

“CSAgain[2:0]” Register: This register sets the gain of the current sensing amplifier.

CSAgain[2:0]	Gain
000b	7.5 times
001b	10 times
010b	12.5 times
011b	15 times
100b	20 times
101b	30 times
110b	40 times
111b	40 times

7.18.32. Address=1001b D[6] “CSAcalSTART”

Write	CSAcalSTART	-
Read	CSAcalibrating	Initial value=0

“CSAcalSTART” Register: This is a write-only register. It starts the calibration of the amplifier. It automatically returns to '0' in a short time.

“CSAcalibrating” Register: This is a read-only register. CSAcalibrating = 1 indicates that the amplifier calibration is in progress. It returns to 0 when the calibration is complete.

7.18.33. Address=1001b D[5] “CSAresult_cl”

Write	CSAresult_cl	-
Read	CSAresult	Initial value=0

“CSAresult_cl” Register: This is a write-only register. When CSAcalibrating = 0, writing 1 sets the CSAresult register to 0. It automatically returns to '0' in a short time.

“CSAresult” Register: This is a read-only register. It indicates the calibration result of the amplifier. CSAresult = 1 indicates a pass.

7.18.34. Address=1010b D[9] “REGreset”

Write	REGreset	-
Read	0	0

“REGreset” Register: This is a write-only register. Writing 1 initializes all registers.

7.18.35. Address=1011b D[9] “GDTESTen”

Write	GDTESTen	-
Read	GDTESTen	Initial value=0

The "GDTESTen" register is a command to check for abnormalities at the SH1 and SH2 terminals. Setting GDTESTen=1 stops the normal gate drive operation and switches to a mode where external n-type MOSFETs are turned on one by one according to the GDTEST[1:0] command to check for abnormalities.

7.18.36. Address=1011b D[8:7] “GDTEST[1:0]”

Write	GDTEST[1:0]	Refer to the table below.
Read	GDTEST[1:0]	Initial value=00b

The "GDTEST[1:0]" register. Together with the GDTESTen command, it turns on external n-type MOSFETs one by one.

GDTEST[1:0]	Action
00b	Turn on HS1.
01b	Turn on LS1.
10b	Turn on HS2.
11b	Turn on LS2.

7.18.37. Address=1011b D[6] “VDS1Hsts”, D[5] “VDS1Lsts”, D[4] “VDS2Hsts”, D[3] “VDS2Lsts”

The "VDS1Hsts" register, "VDS1Lsts" register, "VDS2Hsts" register, and "VDS2Lsts" register. The output of the Vds comparator can always be read regardless of the GDTESTen command. This is the result of comparing the drain-source voltage of each external n-type MOSFET with the threshold voltage, regardless of whether the MOSFET is on or off.

Write	0	-
Read	VDS1Hsts	Initial value= 0

Write	0	-
Read	VDS1Lsts	Initial value= 0

Write	0	-
Read	VDS2Hsts	Initial value= 0

Write	0	-
Read	VDS2Lsts	Initial value= 0

Note: The initial value will be immediately affected by the external circuit after deinitialization, and will become either 0 or 1.

7.18.38. Address=1100b D[9] “INspiSEL”

Write	INspiSEL	-
Read	INspiSEL	Initial value=0

The "INspiSEL" register. It directs the gate drive from the SPI instead of the IN11, IN12, IN21, and IN22 terminals. INspiSEL=1 is the mode where the gate drive is controlled from the SPI. INspiSEL=0 is the mode where the gate drive is controlled from the IN11, IN12, IN21, and IN22 terminals.

7.18.39. Address=1100b D[8] “INspi11”, D[7] “INspi12”, D[6] “INspi21”, D[5] “INspi22”

Write	INspi11	-
Read	INspi11	Initial value=0

The "INspi11" register. When INspiSEL=1, the gate drive is directed by the value of this register instead of the IN11 terminal.

Write	INspi12	-
Read	INspi12	Initial value=0

The "INspi12" register. When INspiSEL=1, the gate drive is directed by the value of this register instead of the IN12 terminal.

Write	INspi21	-
Read	INspi21	Initial value=0

The "INspi21" register. When INspiSEL=1, the gate drive is directed by the value of this register instead of the IN21 terminal.

Write	INspi22	-
Read	INspi22	Initial value=0

The "INspi22" register. When INspiSEL=1, the gate drive is directed by the value of this register instead of the IN22 terminal.

7.18.40. Address=1100b D[4] “PWMEN”

Write	PWMEN	-
Read	PWMEN	Initial value=0

The "PWMEN" register. When PWMEN=1 in H-bridge mode, the "Forward" command is replaced with "Forward" + "Brake", and the "Reverse" command is replaced with "Reverse" + "Brake", limiting the motor drive. Writing to this register is immediately reflected in the PWM circuit. Please write when the drive command is "Brake" or "High-Z". Changing the value during "Forward" or "Reverse" commands may result in unintended behavior. Please verify thoroughly.

7.18.41. Address=1100b D[0] “Half-bridge mode”

Write	Half-bridge mode	-
Read	Half-bridge mode	Initial value=0

The half-bridge mode register. When this command is set to 1, it operates in half-bridge mode. When set to 0, it operates in H-bridge mode.

7.18.42. Address=1101b D[9:0] “PWMCNT[9:0]”

Write	PWMCNT[9:0]	-
Read	PWMCNT[9:0]	Initial value=00_1100_0111b(0C7h)

The PWMCNT[9:0] register. This command sets the period of the PWM waveform when PWMEN=1 in H-bridge mode. The value represents the count of the internal clock. Each increment of the value extends the period by approximately 250 ns.

The range of writable values and the corresponding periods are shown below:

Writable value range: 00Fh to 3FFh. Values outside this range cannot be written and will result in an SPI error.

Maximum count: 3FFh = 1023. 250 * 1024 = 256,000 ns. 3,906 Hz

Minimum count: 00Fh = 15. 250 * 16 = 4,000 ns. 250 kHz

Initial count: 0C7h = 199. 250 * 200 = 50,000 ns. 20 kHz

Simply writing to this register will not change the operation from the previously set value. The value of this register is reflected in the PWM circuit after writing to the PWMDT[9:0] register and when the PWM counter value reaches zero.

7.18.43. Address=1110b D[9:0] “PWMDT[9:0]”

Write	PWMDT[9:0]	-
Read	PWMDT[9:0]	Initial value=00_0110_0011b(063h)

The PWMDT[9:0] register. This command sets the duty cycle of the PWM waveform when PWMEN=1 in H-bridge mode. During PWM operation, the PWM counter repeatedly counts from 0 to PWMCNT[9:0]. PWMDT[9:0] is compared with the counter value, and when they match, the command changes from "Forward" or "Reverse" to "Brake". Adjust the values of PWMCNT[9:0] and PWMDT[9:0] according to the external n-type MOSFETs and motor being used.

When writing to this register, it operates with the previously set value. The value of this register is reflected in the PWM circuit only when the PWM counter value is zero.

Writable value range: 00Fh to 3FFh. Values outside this range cannot be written and will result in an SPI error.

If PWMCNT[9:0] ≤ PWMDT[9:0], the duty cycle will be 100%.

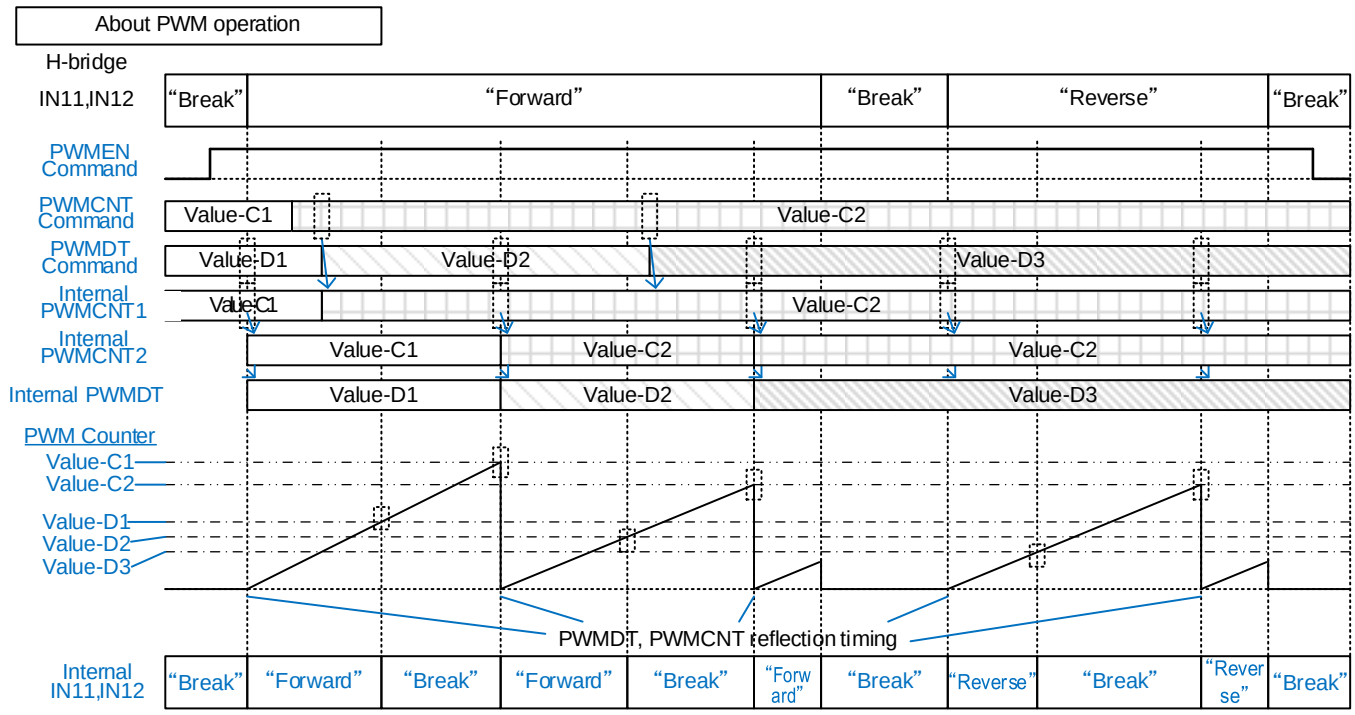


Fig. 7.18.43.1 Operation of PWM counter

7.18.44. Address=1111b D[9:0] “NOP[9:0]”

Write	NOP[9:0]	-
Read	NOP[9:0]	Initial value=00_0000_0000b

The "NOP[9:0]" register. In the SPI of the TB9104FTG, the read operation allows you to obtain the value of the desired register in the next communication. You can use a write or read to the NOP register as the next communication.

Writing any value to the NOP register does nothing. The data from the originally desired address is output from the SDO pin.

In the communication following the NOP register access, the SDO pin outputs the address 1111b, the Read/Write bit from the NOP register access, and all zeros as data.

8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings

Unless otherwise specified, Ta= -40 to 125°C, voltage is based on GND, and the direction of current flowing into the pin is positive.

Spec. No.	Characteristics	Terminal	Symbol	Condition	Rating			Unit
8.1	Power supply VB voltage 1	VB	Vvb1a	Slew Rate: <8V/μs	-0.3	to	Vvcp1a+0.3, 18 Whichever is lower	V
8.2	Power supply VB voltage 2	VB	Vvb2a	≤1s	18	to	Vvcp2a+0.3, 40 Whichever is lower	V
8.3	Power supply VCC voltage	VCC	Vvcc1a	Slew Rate: <0.3V/μs	-0.3	to	6.0	V
8.4	Power supply VDD voltage	VDD	Vvdd1a	Slew Rate: <0.3V/μs	-0.3	to	6.0	V
8.5	Charge pump voltage 1	CPDO	Vcpdo1a	-	-0.3	to	Vvb1a+0.3, 18 Whichever is lower	V
8.6	Charge pump voltage 2	CPDO	Vcpdo2a	≤1s	18	to	Vvb2a+0.3 40 Whichever is lower	V
8.7	Charge pump voltage 3	CPIN	Vcpin1a	-	-0.3	to	Vvcp1a+0.3, 32.5 Whichever is lower	V
8.8	Charge pump voltage 4	CPIN	Vcpin2a	≤1s	32.5	to	Vvcp2a+0.3 40 Whichever is lower	V
8.9	Charge pump voltage 5	VCP	Vvcp1a	-	-0.3	to	32.5	V
8.10	Charge pump voltage 6	VCP	Vvcp2a	≤1s	32.5	to	40	V
8.11	Charge pump voltage 7	RPPO	Vrppo1a	-	-0.3	to	Vvcp1a+0.3, 32.5 Whichever is lower	V
8.12	Charge pump voltage 8	RPPO	Vrppo2a	≤1s	32.5	to	Vvcp2a+0.3 40 Whichever is lower	V
8.13	Charge pump voltage 9	RPPO	Vrppo3a	-18V is assumed for reverse battery connection. AGND=GND=0V, VB=VCC=VDD=Open	-18	to	0	V
8.14	High-side drain pin voltage 1	DH	Vdh1a	-	-0.3	to	18	V

Spec. No.	Characteristics	Terminal	Symbol	Condition	Rating			Unit
8.15	High-side drain pin voltage 2	DH	Vdh2a	≤1s	18	to	40	V
8.16	High-side gate pin voltage 1	GH1, GH2	Vgh1a	≤1μs , 20kHz	-14	to	-7	V
8.17	High-side gate pin voltage 2	GH1, GH2	Vgh2a	-	-7	to	Vvcp1a+0.3, 32.5 Whichever is lower	V
8.18	High-side gate pin voltage 3	GH1, GH2	Vgh3a	≤1s	32.5	to	Vvcp2a+0.3 40 Whichever is lower	V
8.19	High-side source pin voltage 1	SH1, SH2	Vsh1a	≤1μs , 20kHz	-14	to	-7	V
8.20	High-side source pin voltage 2	SH1, SH2	Vsh2a	-	-7	to	Vvcp1a+0.3, 32.5 Whichever is lower	V
8.21	High-side source pin voltage 3	SH1, SH2	Vsh3a	≤1s	32.5	to	Vvcp2a+0.3, 40 Whichever is lower	V
8.22	Low-side gate pin voltage 1	GL1, GL2	Vgl1a	≤1μs , 20kHz	-10	to	-7	V
8.23	Low-side gate pin voltage 2	GL1, GL2	Vgl2a	-	-7	to	Vvb1a+0.3, 32.5 Whichever is lower	V
8.24	Low-side gate pin voltage 3	GL1, GL2	Vgl3a	≤1s	32.5	to	Vvb2a+0.3, 40 Whichever is lower	V
8.25	Low-side source pin voltage 1	SL	Vsl1a	≤1μs , 20kHz	-10	to	-7	V
8.26	Low-side source pin voltage 2	SL	Vsl2a	-	-7	to	Vvb1a+0,3, 32.5 Whichever is lower	V
8.27	Low-side source pin voltage 3	SL	Vsl3a	≤1s	32.5	to	Vvb2a+0,3, 40 Whichever is lower	V
8.28	Differential voltage 1	VB-DH	Vvbdh1a	-	-2	to	2	V
8.29	Differential voltage 2	AGND-GND	Vagndgnd1a	-	-0.3	to	0.3	V
8.30	Input pin voltage 1	STBY_X, IN11, IN12, IN21, IN22, CS_X, SDI, SCLK	Vinp1a	-	-0.3	to	Vvdd1a+0.3, 6 Whichever is lower	V

Spec. No.	Characteristics	Terminal	Symbol	Condition	Rating			Unit
8.31	Input pin voltage 2	TEST1	Vinp2a	-	-0.3	to	Vvcp1a+0.3, 32.5 Whichever is lower	V
8.32	Input pin voltage 3	AMPP, AMPN	Vamppn1a	≤1μs , 20kHz	-10	to	-7	V
8.33	Input pin voltage 4	AMPP, AMPN	Vamppn2a	-	-7	to	18	V
8.34	Input pin voltage 5	AMPP, AMPN	Vamppn3a	≤1s	18	to	40	V
8.35	Output pin voltage 1	DIAG_X, SDO	Vout1a	-	-0.3	to	Vvdd1a+0.3, 6 Whichever is lower	V
8.36	Output pin voltage 2	AMPO	Vampo1a	-	-0.3	to	Vvcc1a+0.3, 6 Whichever is lower	V
8.37	Output pin current	DIAG_X	Idiag_x1a	-	-10	to	10	mA
8.38	Ambient temperature	-	Ta	-	-40	to	125	°C
8.39	Junction temperature	-	Tj	-	-40	to	150	°C
8.40	Storage temperature	-	Tstg	-	-55	to	150	°C
8.41	Allowable loss	-	PD	-		to	(0.6)	W

The absolute maximum ratings are standard values that must not be exceeded even momentarily.

When any absolute maximum rating is exceeded, it may cause destruction, degradation, or damage to the IC and/or other parts. Design systems so that absolute maximum ratings are not exceeded in any operating condition. Please use this IC within the operating ranges described above. he values in parentheses in Table 8.1 are design guarantees.

8.1. Power Dissipation

Fig. 8.1.1 Power Dissipation

9. Operating Ranges

Table 9.1 Operating Ranges

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
9.1	Operating power supply voltage1	VvbRNG	-	5.7	12	18	V
9.2	Operating power supply voltage2	VvccRNG	-	4.5	5.0	5.5	V
9.3	Operating power supply voltage3	VvddRNG	-	4.5	5.0	5.5	V
9.4	Operating junction temperature	TjRNG	-	-40	-	150	°C

Note: Please connect the VCC terminal and the VDD terminal to the same power supply.

10. Electrical Characteristics

10.1. Power

Table 10.1.1 Current consumption

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.1.1	Operating power supply current (VB)	Ivb	STBY_X=H fPG1=20kHz RloadG=10Ω CloadG=6100pF Rrppo=150kΩ	7.0	14.3	20	mA
10.1.2	Operating power supply current (VCC)	Ivcc	STBY_X=H	2.7	4.9	7.5	mA
10.1.3	Operating power supply current (VDD)	Ivdd	STBY_X=H	-	0.8	1.4	mA
10.1.4	Power supply current in standby mode (VB)	IvbSTBY	STBY_X=L	-	0.1	1.0	μA
10.1.5	Power supply current in standby mode (VCC)	IvccSTBY	STBY_X=L	-	1.6	4.5	μA
10.1.6	Power supply current in standby mode (VDD)	IvddSTBY	STBY_X=L	-	0.1	6.5	μA

10.2. Clock

Table 10.2.1 Oscillator circuit

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.2.1	Internal oscillator oscillation frequency	Fc	-	2.6	4.0	5.4	MHz

10.3. Input and output pins

Table 10.3.1 Input and output pins

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.3.1	Low level input voltage STBY_X,IN11,IN12, IN21,IN22,CS_X,SDI,SCLK	VinpL	-	-	-	0.25×VDD	V
10.3.2	High level input voltage STBY_X,IN11,IN12, IN21,IN22,CS_X,SDI,SCLK	VinpH	-	0.75×VDD	-	-	V
10.3.3	Low level input current STBY_X,IN11,IN12, IN21,IN22, SDI,SCLK	IinpL	VDD=5.0V, Vinput=GND	-5	-	5	μA
10.3.4	High level input current STBY_X,IN11,IN12, IN21,IN22, SDI,SCLK	IinpH	VDD=5.0V, Vinput=VDD	50	100	200	μA
10.3.5	Low level input current CS_X	Ics_xL	VDD=5.0V, CS_X=GND	-200	-100	-50	μA
10.3.6	High level input current CS_X	Ics_xH	VDD=5.0V, CS_X=VDD	-5	-	5	μA
10.3.7	analog LPF Cutoff pulse width STBY_X	Tstby_xPW	-	1	2.5	5	μs
10.3.8	Transition time from normal state to standby state	Tstby	STBY_X Fall to GHx, GLx=Off	-	-	500	μs
10.3.9	Transition time from standby state to normal state	Twake	STBY_X Rise to GHx, GLx=On	1.2	1.7	2.7	ms
10.3.10	Transition time from standby mode to enable SPI communication	Twakespi	STBY_X Rise to SDO H,L Out	-	-	150	μs
10.3.11	Low level output voltage DIAG_X	Vdiag_xL	Idiag_x=5mA	-	-	0.1×VDD	V
10.3.12	High impedance state current DIAG_X	Idiag_xZ	DIAG_X=VDD	-	-	10	μA
10.3.13	Low level output voltage SDO	VsdoL	Isdo= 5mA	-	-	0.1×VDD	V
10.3.14	High level output voltage SDO	VsdoH	Isdo= -5mA	0.9×VDD	-	-	V
10.3.15	High impedance state current SDO	IsdoZ	SDO=VDD	-	-	10	μA
10.3.16	Synchronization delay IN11,IN12,IN21,IN22	Tpd_d	Refer to Fig. 7.17.1.4.1, Fig. 7.17.2.4.1	-	1000	-	ns
10.3.17	Pull-down resistor TEST1	Rtest1PDR	-	25	50	100	kΩ

Note: Vinput refers to the voltage of the measured terminals STBY_X, IN11, IN12, IN21, IN22, CS_X, SDI, SCLK.

10.4. SPI

Table 10.4.1 SPI

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.4.1	CS_X fall to SDO delay time	Tcs_xsdo	Cload=100pF	-	-	100	ns
10.4.2	Effective wait time	Tcs_xsclk	Fop=2MHz	100	-	-	ns
10.4.3	Ineffective wait time	Tsclkcs_x	-	100	-	-	ns
10.4.4	SDI setup time	TsdiSET	-	50	-	-	ns
10.4.5	SDI hold time	TsdiHLD	-	50	-	-	ns
10.4.6	SDO delay time	TsdoDLY	Cload=100pF	-	-	100	ns
10.4.7	CS_X ineffective time	Tcs_xH	-	2	-	-	µs
10.4.8	SDO to CS_X rise delay time	Tsdocs_xDLY	Cload=100pF	-	-	100	ns
10.4.9	Communication frequency	Fop	-	-	-	2	MHz
10.4.10	SCLK high period	TsclkH	-	250	-	-	ns
10.4.11	SCLK low period	TsclkL	-	250	-	-	ns

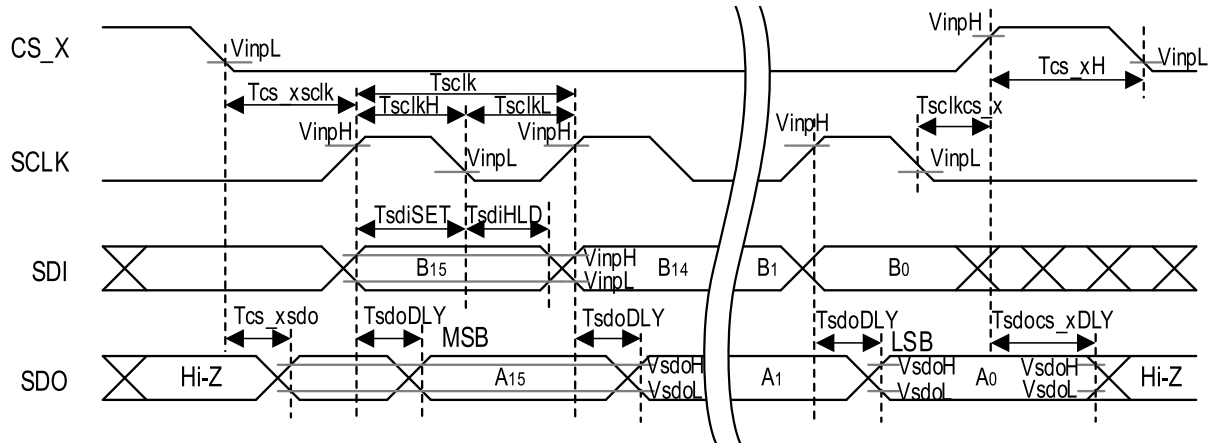


Fig. 10.4.1 SPI Timing Chart

10.5. Charge pump

Table 10.5.1 Charge pump

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Rcp≤7.5Ω,Ccp=,0.1μF, Cvcp=2.2μF IvcpLOAD= -8mA RPPO, GHx, GLx is unloaded

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.5.1	Charge pump voltage 1	Vvcp	VB=8 to 18V	VB+5.7	-	VB+14.5	V
10.5.2	Charge pump voltage 2	VvcpL	VB=5.7 to 8V	VB+4.3	-	VB+8	V
10.5.3	Charge pump switching frequency	Fvcp	-	130	200	270	kHz
10.5.4	Charge pump boot time	TvcpGOOD	After startup, until the VCP voltage reaches 90%.	-	-	1500	μs
10.5.5	Charge pump pull down register	Rvcpvb	VB=0, VCP=1V	300	600	900	kΩ

10.6. Gate driver circuit for reverse polarity protection

Table 10.6.1 Gate driver circuit for reverse polarity protection

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Rcp≤7.5Ω,Ccp=,0.1μF, Cvcp=2.2μF IvcpLOAD= -8mA GHx,GLx is unloaded.

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.6.1	RPP SW ON State Output Voltage	VrppoON	Iload= -110μA	VCP -0.2	-	VCP	V
10.6.2	RPP SW OFF State Leakage Current	IrppoLK	RPPO=VB	-5	0	5	μA
10.6.3	Reverse leakage current	IrppoRLK	RPPO= -18V, GND=AGND=0V, VB=VCC=VDD=Open Refer to Fig. 11.1	0	0.1	10	μA

10.7. gate driver

Table 10.7.1 gate driver

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.
Rcp≤7.5Ω,Ccp=,0.1μF, Cvcp=2.2μF

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.7.1	Driving voltage between high-side gate and source when on 1	VgsHSsrc1	SHx=VB, Iload= -100μA VB=8 to 18V GHx-SHx	4	-	12	V
10.7.2	Driving voltage between high-side gate and source when on 2	VgsHSsrc2	SHx=VB, Iload= -100μA VB=5.7 to 8V GHx-SHx	4	-	8	V
10.7.3	Shunt voltage between high-side gate and source when off	VgsHSsnk	SHx=VB, Iload=100μA GHx-SHx	-	-	0.2	V
10.7.4	Driving voltage between low-side gate and source when on 1	VgsLSsrc1	SL=GND, Iload= -100μA VB=8 to 18V GLx-SL	4	-	12	V
10.7.5	Driving voltage between low-side gate and source when on 2	VgsLSsrc2	SL=GND, Iload= -100μA VB=5.7 to 8V GLx-SL	4	-	8	V
10.7.6	Shunt voltage between low-side gate and source when off	VgsLSsnk	SL=GND, Iload=100μA GLx-SL	-	-	0.2	V
10.7.7	Output resistance 1	Ronh	The gate driver is on Iload= -50mA	-	10	20	Ω
10.7.8	Output resistance 2	Ronl	The gate driver is off Iload=50mA	-	3	6	Ω
10.7.9	Shunt resistance between gate and source	Rgsshunt	-	25	50	100	kΩ
10.7.10	After the time set by t_ilim following Vgsx rise	Igs_lmth	-	-	-10	-	mA
10.7.11	After the time set by t_ilim following Vgsx fall	Igs_lmtl	-	-	10	-	mA
10.7.12	Output current switching time t_ilim="000"	Tsw0	-	3.7	6	10.5	μs
10.7.13	Output current switching time t_ilim="001"	Tsw1	-	5	8	14	μs
10.7.14	Output current switching time t_ilim="010"	Tsw2	-	6.2	10	17.5	μs
10.7.15	Output current switching time t_ilim="011"	Tsw3	-	7.5	12	21	μs
10.7.16	Output current switching time t_ilim="100"	Tsw4	-	10	16	28	μs

Spec. No.	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
10.7.17	Output current switching time t_ilim="101"	Tsw5	-	20	32	56	µs
10.7.18	Output current switching time t_ilim="110"	Tsw6	-	40	64	112	µs
10.7.19	Input propagation delay time for high-side turn-on	Tdonh	Rload=10Ω,Cload=6100pF Refer to Fig. 7.17.1.4.1, Fig. 7.17.2.4.1	10	260	700	ns
10.7.20	Input propagation delay time for low-side turn-on	Tdonl	Rload=10Ω,Cload=6100pF Refer to Fig. 7.17.1.4.1, Fig. 7.17.2.4.1	10	260	700	ns
10.7.21	Input propagation delay time for high-side turn-off	Tdoffh	Rload=10Ω,Cload=6100pF Refer to Fig. 7.17.1.4.1, Fig. 7.17.2.4.1	10	210	700	ns
10.7.22	Input propagation delay time for low-side turn-off	Tdoffl	Rload=10Ω,Cload=6100pF Refer to Fig. 7.17.1.4.1, Fig. 7.17.2.4.1	10	210	700	ns
10.7.23	Propagation delay difference between high-side and low-side	Tdifhsls	Tdonh – Tdoffl , Tdonl – Tdoffh Rload=10Ω, Cload=6100pF	-250	-	250	ns
10.7.24	Dead time t_deadt="000"	Tdead0	-	185	250	385	ns
10.7.25	Dead time t_deadt="001"	Tdead1	-	370	500	770	ns
10.7.26	Dead time t_deadt="010"	Tdead2	-	555	750	1155	ns
10.7.27	Dead time t_deadt="011"	Tdead3	-	740	1000	1540	ns
10.7.28	Dead time t_deadt="100"	Tdead4	-	925	1250	1925	ns
10.7.29	Dead time t_deadt="101"	Tdead5	-	1110	1500	2310	ns
10.7.30	Dead time t_deadt="110"	Tdead6	-	1295	1750	2695	ns
10.7.31	Dead time t_deadt="111"	Tdead7	-	1480	2000	3080	ns

Note: GHx = { GH1 , GH2 } , GLx = { GL1 , GL2 } , SHx = { SH1 , SH2 }

10.8. Current sense amplifier

Table 10.8.1 Current sense amplifier

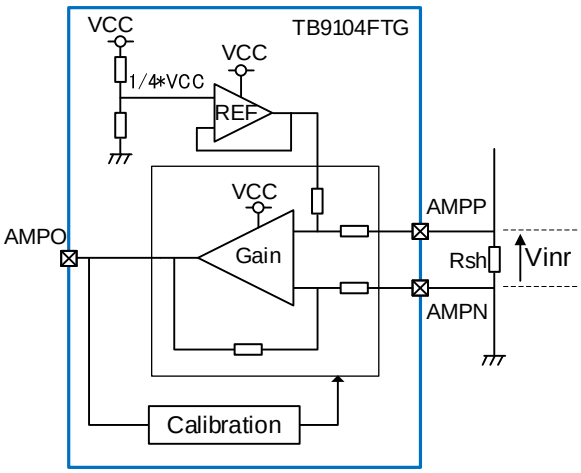
Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristis	Symbol	Condition	Min	Typ.	Max	Unit
10.8.1	Input offset voltage 1 for AMPP and AMPN	Voff1	After the calibration, Ta=25°C Gain=15(CSAgain='011") Comvin=0V Iload=0.5mA	-1	-	1	mV
10.8.2	Input offset voltage 2 for AMPP and AMPN	Voff2	After the calibration, Ta=25°C Gain=15(CSAgain ='011") Comvin=0V Iload=0.5mA	-7	-	7	mV
10.8.3	Temperature characteristic 1 of input offset voltage for AMPP and AMPN	VoffdT1	After the calibration, Gain=15(CSAgain='011") Comvin=0V Iload=0.5mA	(-20)	-	(20)	µV/°C
10.8.4	Temperature characteristic 2 of input offset voltage for AMPP and AMPN	VoffdT2	Before the calibration, Gain=15(CSAgain ='011") Comvin=0V Iload=0.5mA	(-20)	-	(20)	µV/°C
10.8.5	Input offset current 1 for AMPP and AMPN	Iin1	(AMPP,AMPN)= (-0.5V, -0.5V), (2V,2V) I(AMPP) – I(AMPN)	-5	-	5	µA
10.8.6	Input offset current 2 for AMPP and AMPN	Iin2	(AMPP,AMPN)= (2V, -0.5V) I(AMPP) – I(AMPN)	30	-	130	µA
10.8.7	Output voltage for AMPO	Vohop	Gain=15(CSAgain ='011") Vinr = 0.1×VCC Iload = -500µA	VCC-0.15	-	VCC	V
10.8.8	Reference voltage	Vref	-	(VCC/4)-9	VCC/4	(VCC/4)+9	mV
10.8.9	AMPP, AMPN GAIN 0	Gain0	CSAgain = "000" Vinr = (VCC×0.75 – 0.15)/7.5, Comvin=0V, Iload = no load	-1%	7.5	1%	-
10.8.10	AMPP, AMPN GAIN 1	Gain1	CSAgain = "001" Vinr = (VCC×0.75 – 0.15)/10, Comvin=0V, Iload = no load	-1%	10	1%	-
10.8.11	AMPP, AMPN GAIN 2	Gain2	CSAgain = "010" Vinr = (VCC×0.75 – 0.15)/12.5, Comvin=0V, Iload = no load	-1%	12.5	1%	-

Spec. No.	Characteristis	Symbol	Condition	Min	Typ.	Max	Unit
10.8.12	AMPP, AMPN GAIN 3	Gain3	CSAgain = “011” Vinr = (VCC×0.75 – 0.15)/15, Comvin=0V, Iload = no load	-1%	15	1%	-
10.8.13	AMPP, AMPN GAIN 4	Gain4	CSAgain = “100” Vinr = (VCC×0.75 – 0.15)/20, Comvin=0V, Iload = no load	-1%	20	1%	-
10.8.14	AMPP, AMPN GAIN 5	Gain5	CSAgain = “101” Vinr = (VCC×0.75 – 0.15)/30, Comvin=0V, Iload = no load	-1%	30	1%	-
10.8.15	AMPP, AMPN GAIN 6	Gain6	CSAgain = “110”, “111” Vinr = (VCC×0.75 – 0.15)/40, Comvin=0V, Iload = no load	-1.25%	40	1.25%	-
10.8.16	Slew rate 1 for AMPO	Sr1	VCC = 5.0V Gain=15(CSAgain =’011”) Rload = 1kΩ, Cload = 220pF Vinr = 0V to (VCC×0.75 – 0.15)/15 Vout = 2.25V to 4.0V	4.5	10	20	V/μs
10.8.17	Slew rate 2 for AMPO	Sr2	VCC = 5.0V Gain=15(CSAgain =’011”) Rload = 1kΩ, Cload = 220pF Vinr = (VCC×0.75 – 0.15)/15 to 0V Vout = 4.0V to 2.25V	-20	-10	-4.5	V/μs
10.8.18	Settling time for AMPO	Tset	Rload = 1kΩ, Cload = 220pF Time to settle within ±2% of output voltage	-	-	(1.5)	μs
10.8.19	Common-mode input range for AMPP and AMPN	Comvin	-	-0.5	-	2.0	V
10.8.20	VCC PSRR	Psrrop	Apply 1kHz to VCC, excluding the influence of Vref	-	60	-	dB
10.8.21	AMPP,AMPN CMRR	Cmrrop	VCC=5.0V Gain - 15(CSAGain =”011”) Comvin = 20mVp-p, 100kHz	-	100	-	dB
10.8.22	Offset calibration time	Tampofscal	-	-	-	122	μs

Note: Specifications indicated in parentheses are design values and have not been tested during shipment.

Note: Refer to Fig. 10.8.1 for the measurement circuit. The potential difference generated by the current flowing through Rsh towards GND is defined as Vinr.



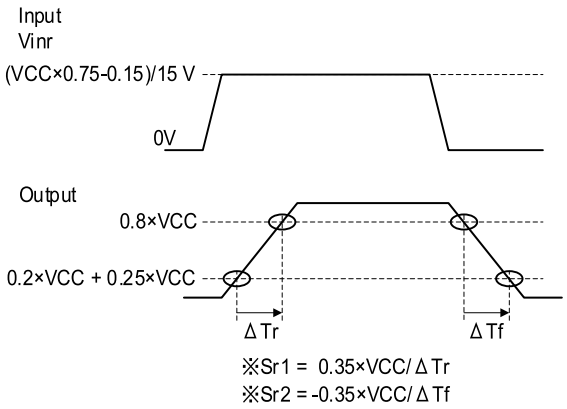


Fig. 10.8.1 Measurement circuit for CSA **Fig. 10.8.2 Through rate timing chart**

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

10.9. State detection

Table 10.9.1 State detection

Unless otherwise specified, VB = 5.7 to 18V, VCC = VDD = 4.5 to 5.5V (VB ≥ VDD), and Ta = -40 to 125°C. All voltages are referenced to GND, and the current direction flowing into the pin is positive.

Spec. No.	Characteristis	Symbol	Condition	Min	Typ.	Max	Unit
10.9.1	VB low voltage detection	VvbUd	-	4.8	5.1	5.4	V
10.9.2	Return after VB low voltage detection	VvbUr	-	5.1	5.4	5.7	V
10.9.3	VB low voltage detection hysteresis	VvbUhys	-	0.1	-	-	V
10.9.4	Cutoff pulse width for VB low voltage detection digital LPF	TvbUpw	-	5.92	8	12.31	µs
10.9.5	VCP high voltage detection	VvcpOd	-	33	36	39	V
10.9.6	Return after VCP high voltage detection	VvcpOr	-	30	33	36	V
10.9.7	VCP high voltage detection hysteresis	VvcpOhys	-	0.1	-	-	V
10.9.8	Cutoff pulse width for VCP high voltage detection digital LPF	TvcpUpw	-	5.92	8	12.31	µs
10.9.9	Low voltage detection between VCP and VB	VvcpvbUd	VCP-VB	3.2	3.6	4.0	V
10.9.10	Recovery after low voltage detection between VCP and VB	VvcpvbUr	VCP-VB	3.5	3.9	4.3	V
10.9.11	Hysteresis for low voltage detection between VCP and VB	VvcpvbUhys	VCP-VB	0.1	-	-	V
10.9.12	Cutoff pulse width for low voltage detection digital LPF between VCP and VB	TvcpvbUpw	-	5.92	8	12.31	µs
10.9.13	High voltage detection between VCP and RPPO	VvcprppoOd	VCP-RPPO	2	3	4	V
10.9.14	Recovery after high voltage detection between VCP and RPPO	VvcprppoOr	VCP-RPPO	1	2	3	V
10.9.15	High Voltage Detection Hysteresis between VCP and RPPO	VvcprppoOhys	VCP-RPPO	0.1	-	-	V
10.9.16	Cutoff Pulse Width of Digital LPF for High Voltage Detection between VCP and RPPO	TvcprppoOpw	-	5.92	8	12.31	µs
10.9.17	VCC low voltage detection	VvccUd	-	3.9	4.1	4.35	V
10.9.18	Return after VCC low voltage detection	VvccUr	-	4.05	4.3	4.5	V
10.9.19	VCC low voltage detection hysteresis	VvccUhys	-	0.1	-	-	V
10.9.20	Cutoff pulse width for VCC low voltage detection analog LPF	TvccUpw	-	1	10	20	µs
10.9.21	High Temperature Detection of Junction Temperature	TjunctOd	-	(155)	(175)	(195)	°C
10.9.22	Recovery after High Temperature Detection of Junction Temperature	TjunctOr	-	(145)	(165)	(185)	°C
10.9.23	High Temperature Detection Hysteresis of Junction Temperature	TjunctOhys	-	-	(10)	(15)	°C
10.9.24	Cutoff Pulse Width of Digital LPF for High Temperature Detection of Junction Temperature	TjunctOpw	-	1.48	2	3.08	µs
10.9.25	DH Input Current	Idh	DH = VB	45	95	150	µA
10.9.26	SHx Output Current 1 when Gate Drive is Off	Ishx1	VB=DH=12V SH1=SH2=12V	-650	-330	-200	µA
10.9.27	SHx Output Current 2 when Gate Drive is Off	Ishx2	VB=DH=12V	-650	-360	-200	µA

			SH1=SH2=0V				
10.9.28	SL Input Current	Isl	Gate drive is on SL=SH1=SH2 = -0.5 to 2V	-1200	-700	0	μA
10.9.29	Mask Time for High Voltage Detection of Vdson	TvdsMASK	-	Setting value × 0.74	Setting value Refer to 7.18.19 7.18.25	Setting value × 1.54	μs
10.9.30	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "000"	VdhshOd0	SL= -0.5 to 1.2V	0.01	0.1	0.19	V
10.9.31	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "001"	VdhshOd1	SL= -0.5 to 1.2V	0.2	0.3	0.4	V
10.9.32	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "010"	VdhshOd2	SL= -0.5 to 1.2V	0.4	0.5	0.6	V
10.9.33	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "011"	VdhshOd3	SL= -0.5 to 1.2V	0.6	0.7	0.8	V
10.9.34	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "100"	VdhshOd4	SL= -0.5 to 1.2V	0.8	0.9	1.0	V
10.9.35	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "101"	VdhshOd5	SL= -0.5 to 1.2V	0.99	1.1	1.21	V
10.9.36	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "110"	VdhshOd6	SL= -0.5 to 1.2V	1.17	1.3	1.43	V
10.9.37	High Voltage Detection Voltage of Vds, VDS1Hth, VDS2Hth = "111"	VdhshOd7	SL= -0.5 to 1.2V	1.35	1.5	1.65	V
10.9.38	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "000"	VshslOd0	SL= -0.5 to 1.2V	0.01	0.1	0.19	V
10.9.39	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "001"	VshslOd1	SL= -0.5 to 1.2V	0.2	0.3	0.4	V
10.9.40	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "010"	VshslOd2	SL= -0.5 to 1.2V	0.4	0.5	0.6	V
10.9.41	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "011"	VshslOd3	SL= -0.5 to 1.2V	0.6	0.7	0.8	V
10.9.42	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "100"	VshslOd4	SL= -0.5 to 1.2V	0.8	0.9	1.0	V
10.9.43	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "101"	VshslOd5	SL= -0.5 to 1.2V	0.99	1.1	1.21	V
10.9.44	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "110"	VshslOd6	SL= -0.5 to 1.2V	1.17	1.3	1.43	V
10.9.45	High Voltage Detection Voltage of Vds, VDS1Lth, VDS2Lth = "111"	VshslOd7	SL= -0.5 to 1.2V	1.35	1.5	1.65	V
10.9.46	Cutoff Pulse Width of Digital LPF for High Voltage Detection of Vds, t_VDS1fil, t_VDS2fil = "00"	TvdsOpw0	-	0.74	1	1.54	μs
10.9.47	Cutoff Pulse Width of Digital LPF for High Voltage Detection of Vds, t_VDS1fil, t_VDS2fil = "01"	TvdsOpw1	-	1.48	2	3.08	μs
10.9.48	Cutoff Pulse Width of Digital LPF for High Voltage Detection of Vds, t_VDS1fil, t_VDS2fil = "10"	TvdsOpw2	-	2.96	4	6.16	μs
10.9.49	Cutoff Pulse Width of Digital LPF for High Voltage Detection of Vds, t_VDS1fil, t_VDS2fil = "11"	TvdsOpw3	-	5.92	8	12.31	μs

Note: The temperature specifications in sections 10.9.21 to 10.9.23 are design-based and have not been tested during shipment.

The overheat shutdown circuit is designed to temporarily avoid abnormal conditions. This does not guarantee the prevention of IC damage.

11. Test Circuit

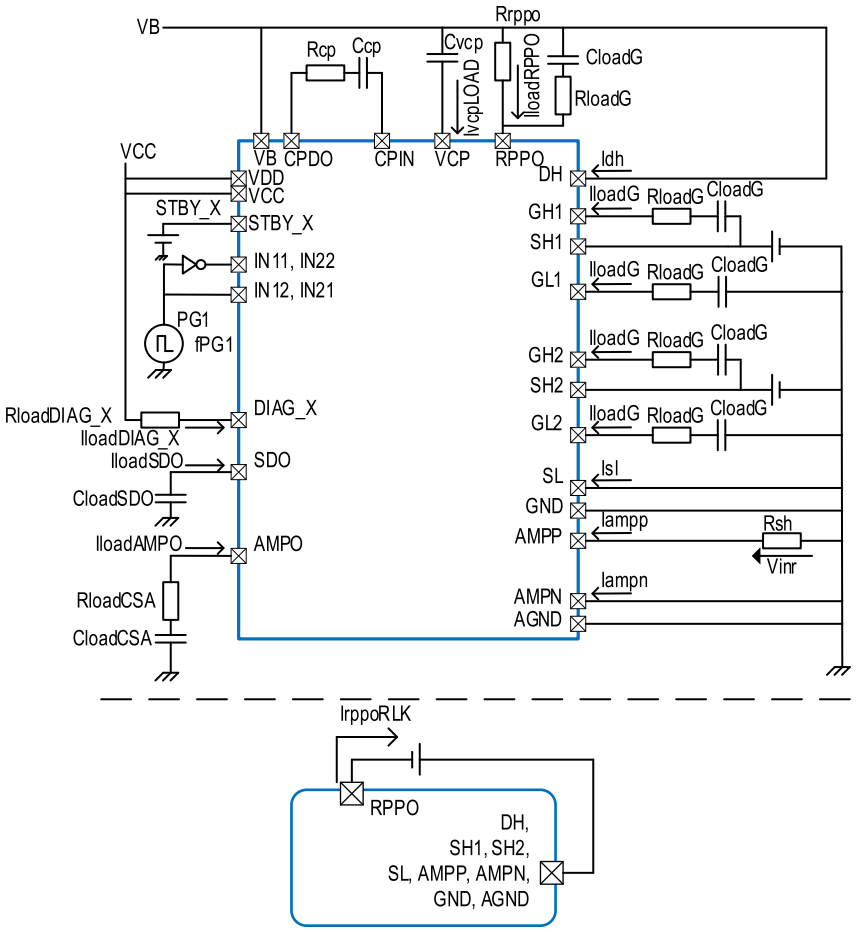


Fig. 11.1 Test Circuit

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC.

Note: The above diagram is a representative measurement circuit. Depending on the measurement conditions listed in the measurement items, the external circuit of the IC may be changed from the above diagram.

12. Characteristic Chart

13. Application circuit example

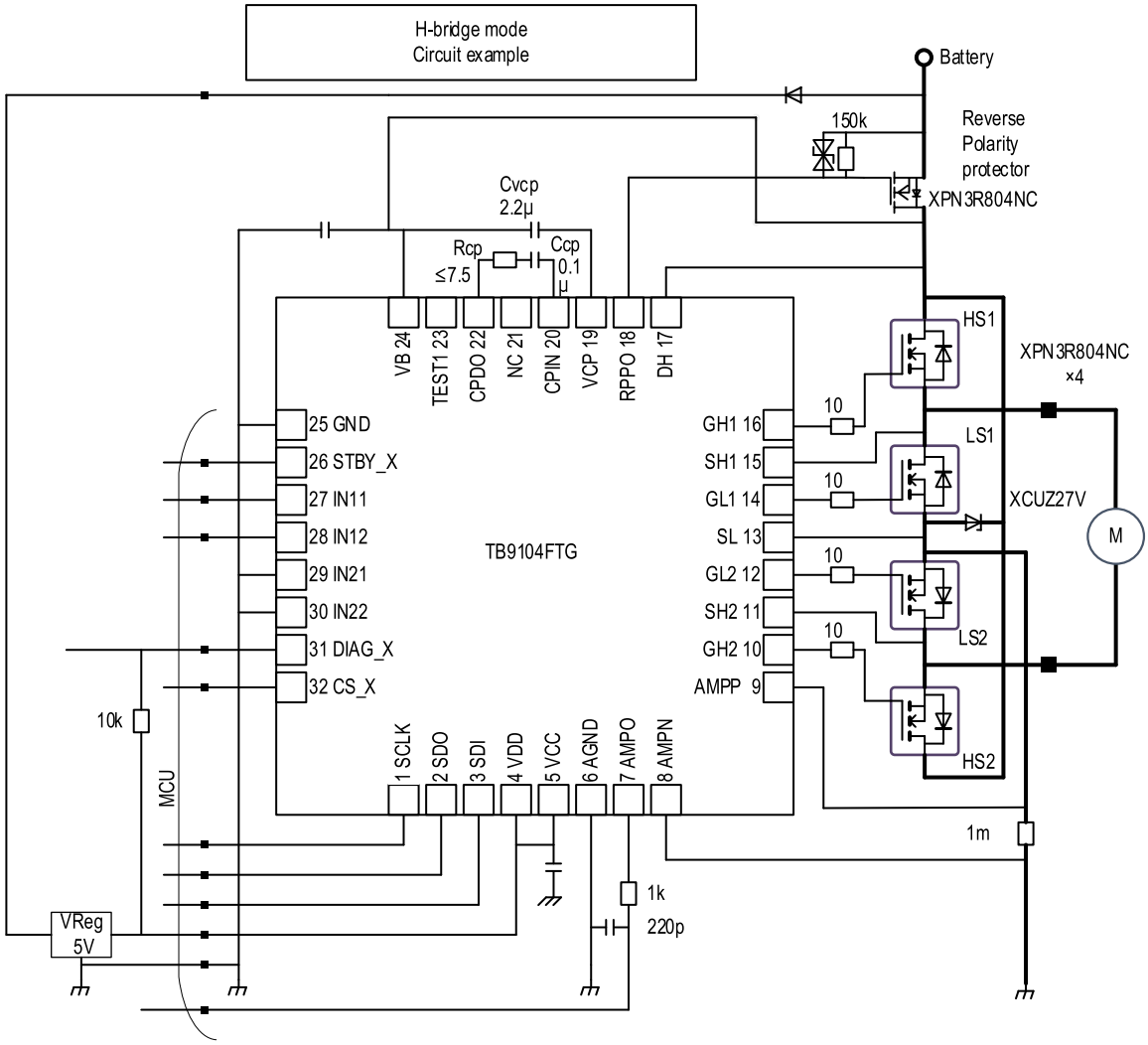


Fig. 13.1 H-bridge mode (Application circuit example)

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC. When using multilayer ceramic capacitors for Cvcp, Ccp, and similar applications, please consider their temperature and voltage dependence, and ensure thorough verification before use. The circuit configuration, component selection, and resistance and capacitance values are examples. Please thoroughly verify and determine these based on the configuration you have selected.

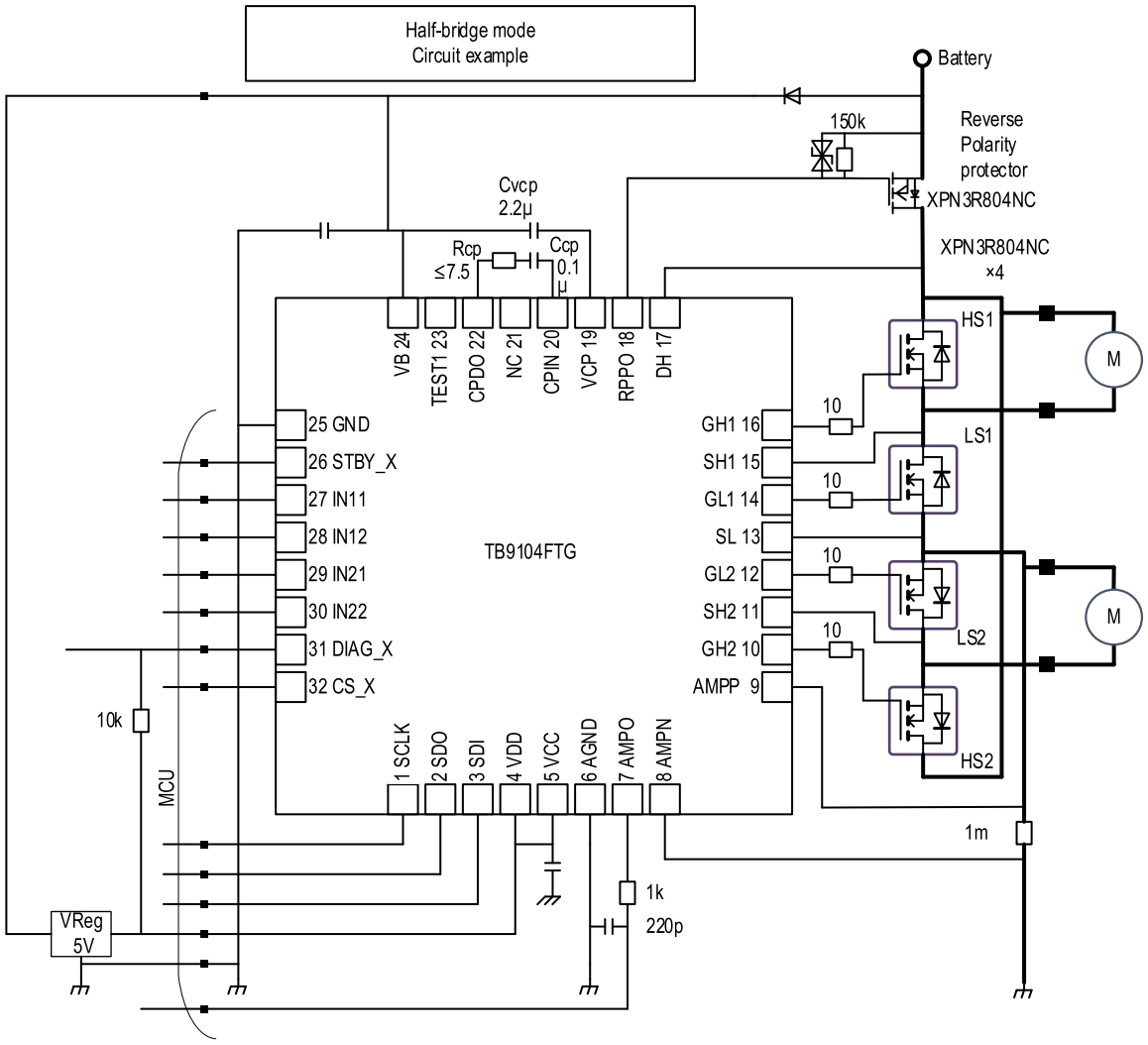


Fig. 13.2 Half-bridge mode (Application circuit example)

Note: The above diagram is partially omitted and simplified in order to explain the functions and operations of the IC. When using multilayer ceramic capacitors for Cvcp, Ccp, and similar applications, please consider their temperature and voltage dependence, and ensure thorough verification before use. The circuit configuration, component selection, and resistance and capacitance values are examples. Please thoroughly verify and determine these based on the configuration you have selected.

14. Package Information

14.1. Package dimensions

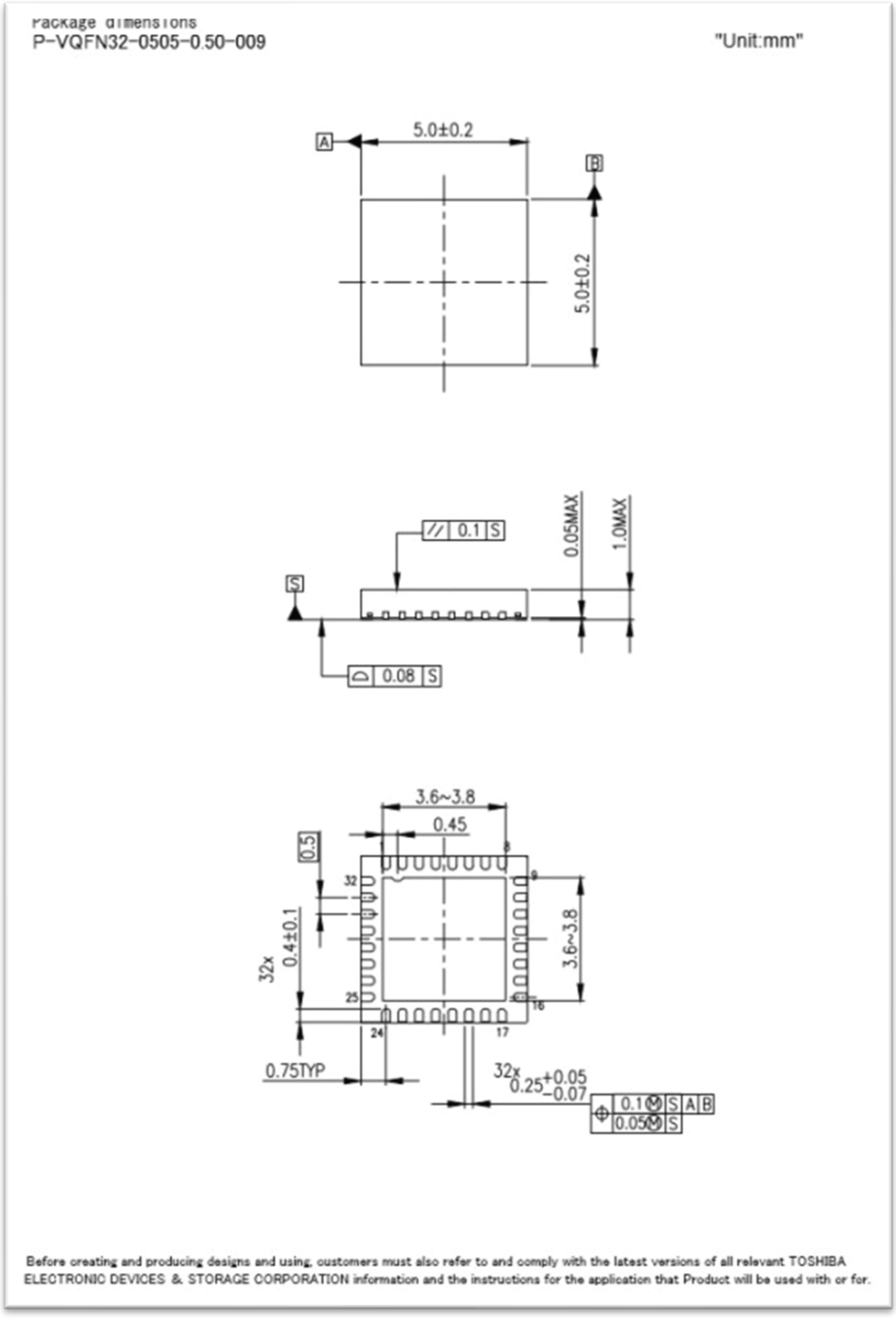


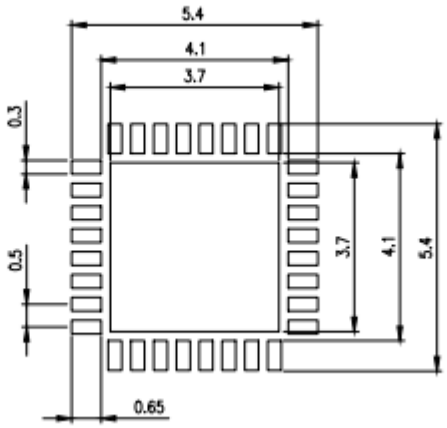
Fig. 14.1.1 Package dimension

Weight: 0.07g (Typ.)

14.2. Land Pattern Dimensions for Reference only

P-VQFN32-0505-0.50-009

"Unit: mm"



Notes

- All linear dimensions are given in millimeters unless otherwise specified.
- This drawing is based on JEITA ET-7501 Level3 and should be treated as a reference only.
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15. IC Usage Considerations

15.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

15.2. Points to Remember on Handling of ICs

(3) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(4) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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