MOSFETs Silicon P-Channel MOS

XSM6J830R

1. Applications

- Power Management Switches

2. Features

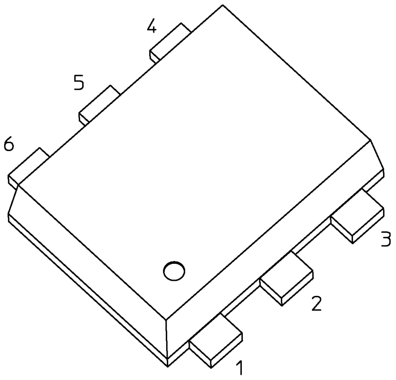
(1) Low drain-source on-resistance

: $R_{DS(ON)}$ = 54 mΩ (typ.) (@V_{GS} = -10 V)

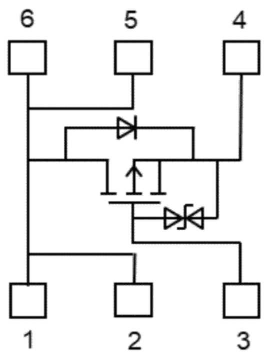
$R_{DS(ON)}$ = 80 mΩ (typ.) (@V_{GS} = -4.5 V)

$R_{DS(ON)}$ = 89 mΩ (typ.) (@V_{GS} = -4 V)

3. Packaging and Pin Assignment



TSOP6F



1: Drain
2: Drain
3: Gate
4: Source
5: Drain
6: Drain

Start of commercial production
2026-03

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	-30	V
Gate-source voltage			V_{GSS}	-20/+10	
Drain current (DC)		(Note 1)	I_D	-4	A
Drain current (pulsed)	t ≤ 10 ms	(Note 1), (Note 2)	I_{DP}	-16	
Power dissipation		(Note 3)	P_D	1.5	W
Power dissipation	t ≤ 10 s	(Note 3)	P_D	3.5	
Single-pulse avalanche energy		(Note 4)	E_{AS}	18.8	mJ
Single-pulse avalanche current			I_{AS}	-4	A
Channel temperature			T_{ch}	150	°C
Storage temperature			T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150°C

Note 2: Pulse width (PW) ≤10 ms, duty ≤ 1%

Note 3: Device mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 645 mm^2)

Note 4: V_{DD} = -24 V, T_{ch} = 25 °C (Inicial state), L = 0.91 mH, R_G = 25 Ω, I_{AS} = -4.0 A

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Thermal Characteristics

Characteristics		Symbol	Max	Unit
Channel-to-ambient thermal resistance	(Note 1)	$R_{th(ch-a)}$	83.3	°C/W

Note 1: Device mounted on an 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm^2)

6. Electrical Characteristics

6.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = -16/+10 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	—	—	-1	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -10 mA, V_{GS} = 0 V	-30	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = -10 mA, V_{GS} = 10 V	-21	—	—	
Gate threshold voltage	(Note 2)	V_{th}	V_{DS} = -10 V, I_D = -0.1 mA	-0.8	—	-2	
Drain-source on-resistance	(Note 3)	$R_{DS(ON)}$	I_D = -1 A, V_{GS} = -4 V	—	89	136	mΩ
			I_D = -2 A, V_{GS} = -4.5 V	—	80	105	
			I_D = -3 A, V_{GS} = -10 V	—	54	71	

Note 1: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-0.1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 3: Pulse measurement.

6.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	—	280	—	pF
Reverse transfer capacitance	C_{rss}		—	40	—	
Output capacitance	C_{oss}		—	55	—	
Switching time (rise time)	t_r	V_{DD} = -15 V, I_D = -1 A, V_{GS} = 0 to -4.5 V, R_{GG} = 10 Ω, R_{GS} = 10 Ω	—	8	—	ns
Switching time (turn-on time)	t_{on}		—	13	—	ns
Switching time (fall time)	t_f		—	9	—	ns
Switching time (turn-off time)	t_{off}		—	22	—	ns

6.3. Switching Time Test Circuit

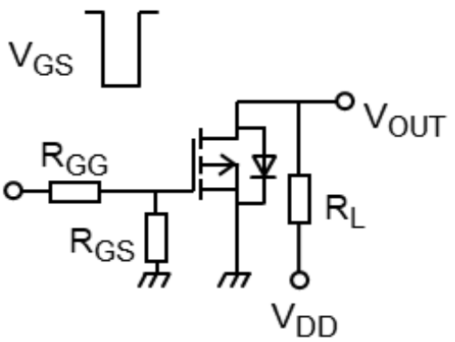


Fig. 6.3.1 Switching Time Test Circuit

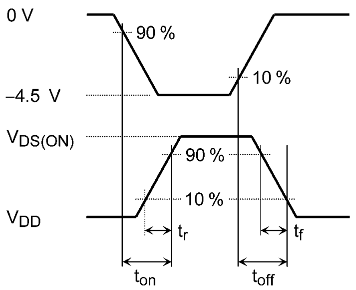


Fig. 6.3.2 Input Waveform/Output Waveform

6.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = -15 V, V_{GS} = -10 V, I_D = -4 A	—	5.9	—	nC
Gate-source charge 1	Q_{gs1}		—	0.8	—	
Gate-drain charge	Q_{gd}		—	1.2	—	

6.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V_{DSF}	I_{DR} = -4 A, V_{GS} = 0 V	—	0.9	1.2	V

Note 1: Pulse measurement.

7. Marking

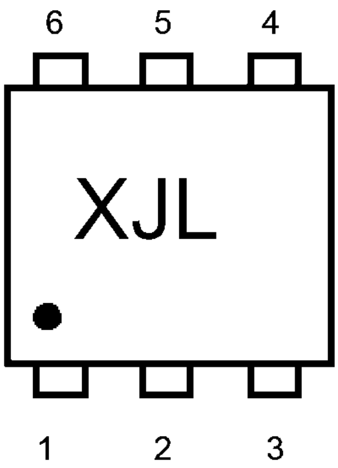


Fig. 7.1 Marking

8. Characteristics Curves (Note)

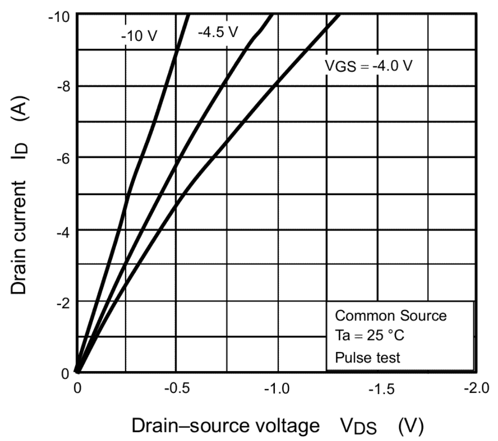


Fig. 8.1 I_D - V_{DS}

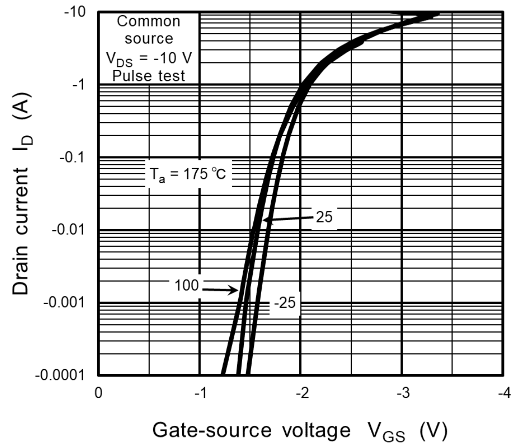


Fig. 8.2 I_D - V_{GS}

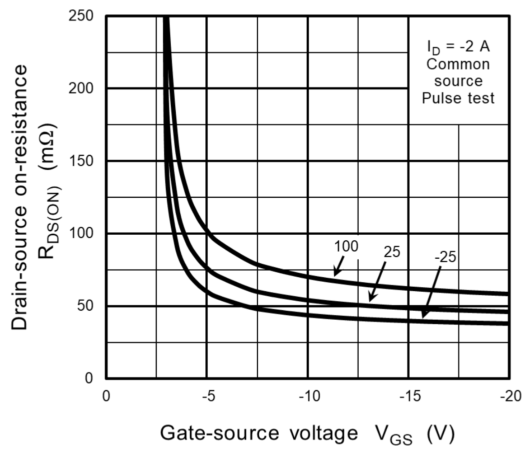


Fig. 8.3 $R_{DS(ON)}$ - V_{GS}

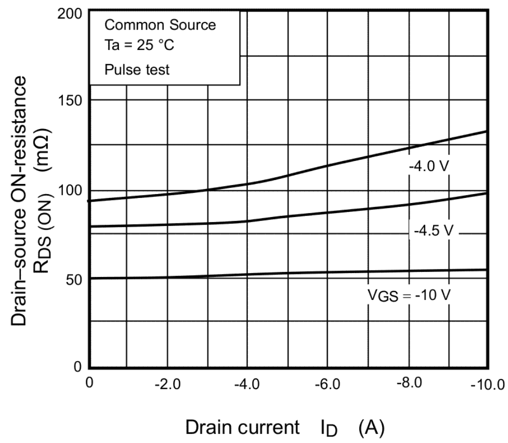


Fig. 8.4 $R_{DS(ON)}$ - I_D

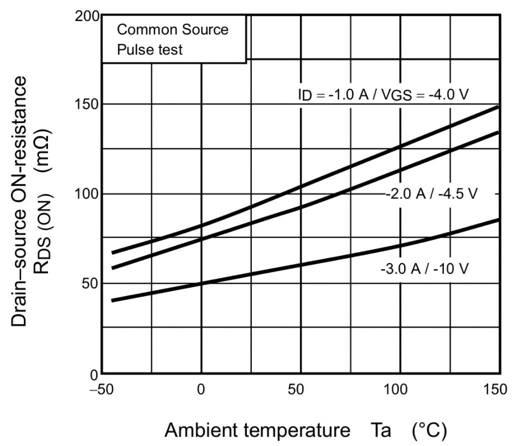


Fig. 8.5 $R_{DS(ON)}$ - T_a

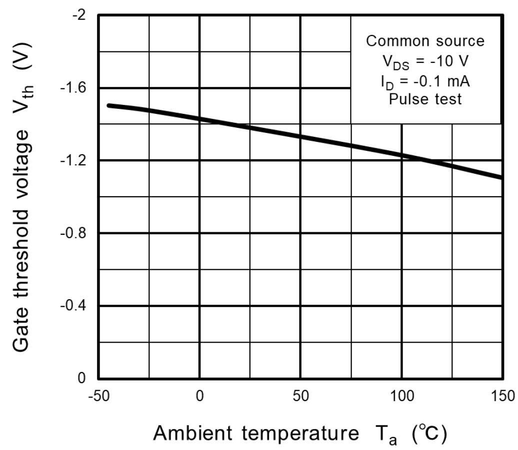


Fig. 8.6 V_{th} - T_a

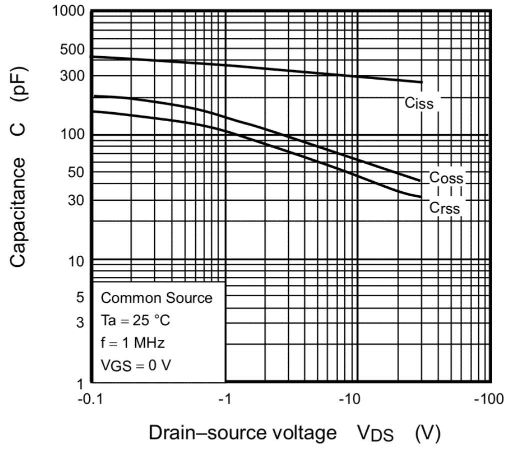


Fig. 8.7 C - V_{DS}

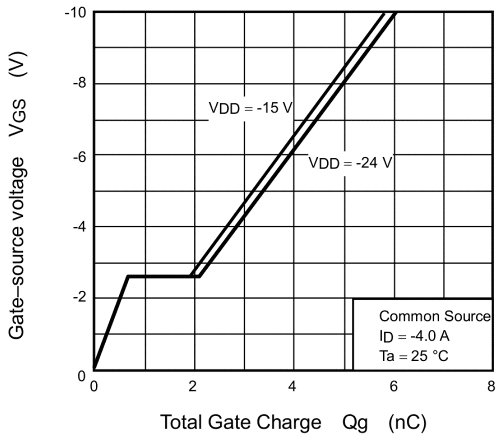


Fig. 8.8 Dynamic Input Characteristics

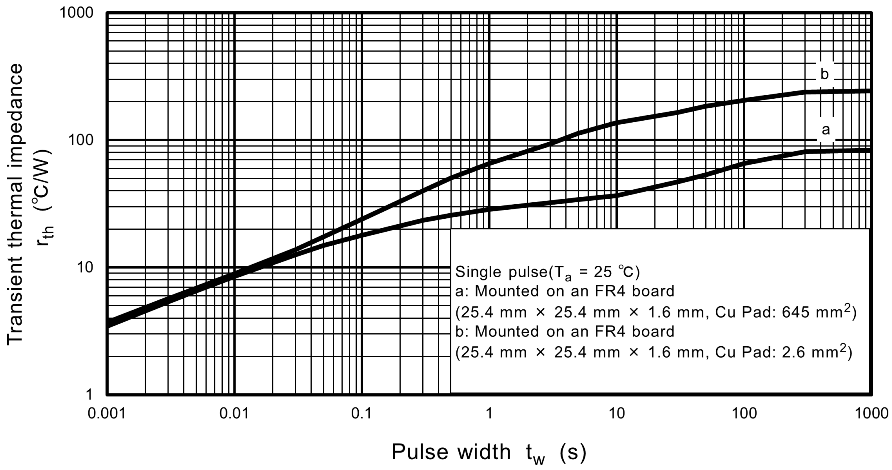


Fig. 8.9 r_{th} - t_w

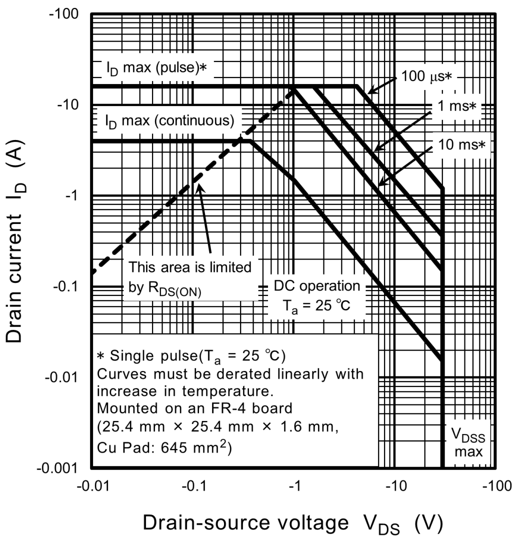


Fig. 8.10 Safe Operating Area

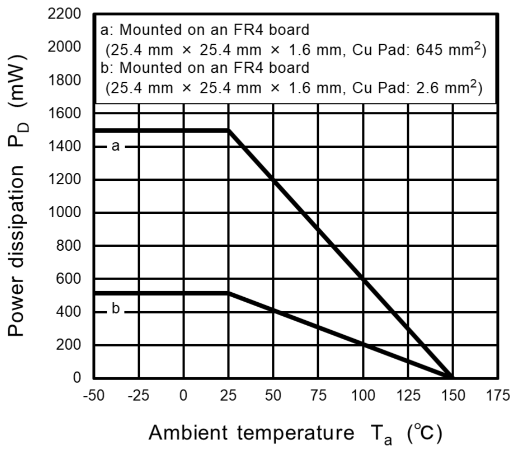
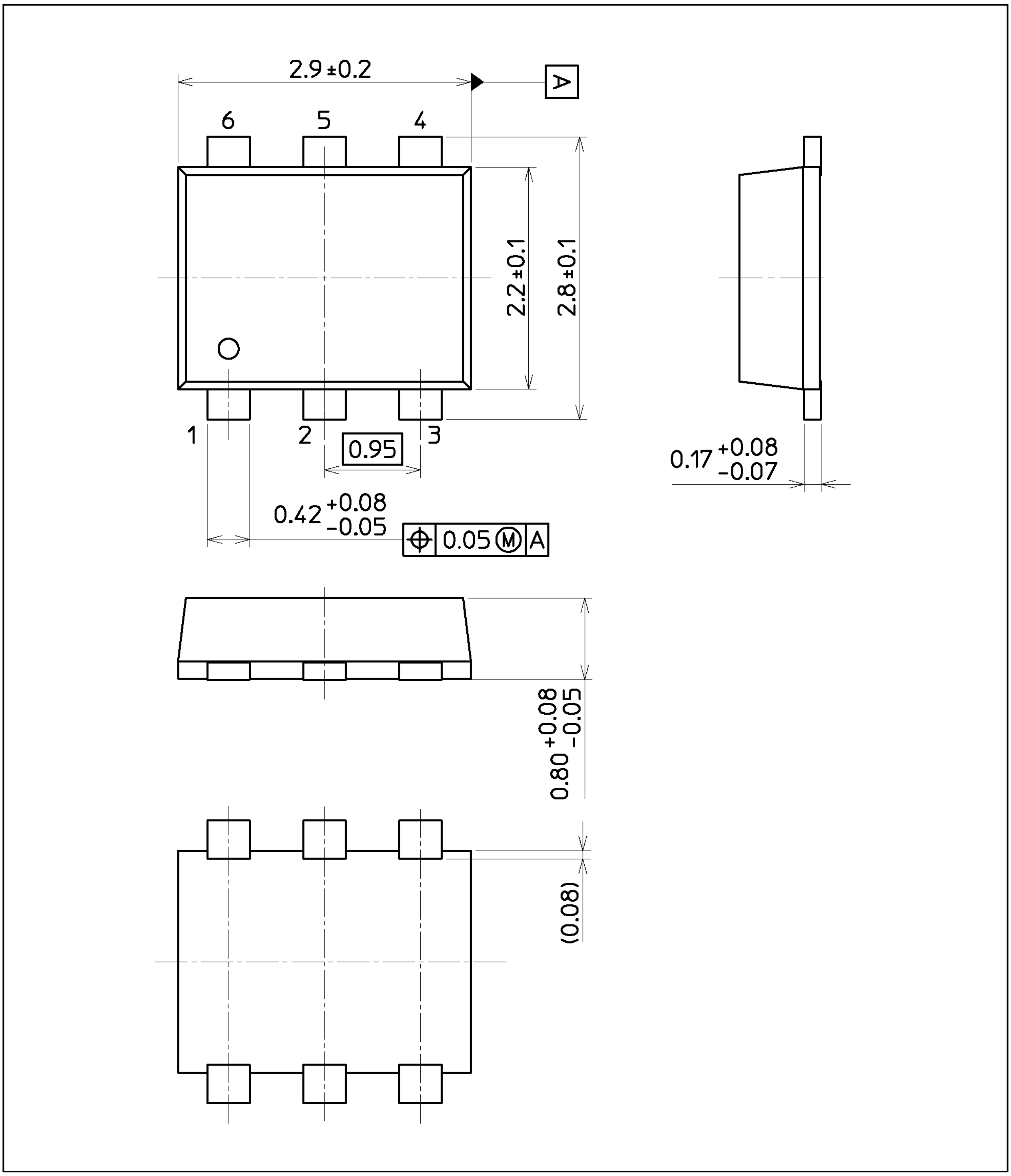


Fig. 8.11 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.016 g (typ.)

Package Name(s)
Nickname: TSOP6F

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