3kW Power Supply for Servers and Telecoms Using Surface-Mounted SiC MOSFET

Design Guide

RD244-DGUIDE-01

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1. Introduction

This design guide describes the design overview of each circuit block of the 3kW power supply for servers and telecoms with surface-mounted SiC MOSFET (hereafter referred to as “this design”).

In recent years, data centers have become increasingly large and dense. As a result, server power supplies are required to deliver higher efficiency, higher power output, and more compact form factors, making high power density essential. This design accepts an AC input voltage range of 180 to 264V and outputs DC 50V through a semi-bridgeless PFC (Power Factor Correction) circuit and a Phase Shift Full Bridge (PSFB) circuit. The maximum output power is 3kW when using an AC 200V input. It includes an output ORing circuit that enables redundant operation, as well as an internal auxiliary power supply circuit required for powering internal control circuits. By separating the power devices from the main board, the footprint per output is reduced, contributing to a more compact power supply. In addition to server applications, this design can be applied to telecom systems and other applications that utilize 48V.

This design uses the SiC MOSFET TW092V65C and the SiC Schottky Barrier Diode TRS12V65H in the semi-bridgeless PFC circuit. The PSFB circuit uses the SiC MOSFET TW027U65C with integrated Schottky Barrier Diode on the primary full-bridge side, and the power MOSFET TPW2900ENH on the secondary synchronous rectification side. For isolated gate signal transmission from the secondary-side controller, the digital isolator DCL540C01 is used. The output ORing circuit uses the power MOSFET TPM1R908QM. By integrating these advanced Toshiba devices, this design achieves high efficiency equivalent to 80PLUS Platinum level (V_{in} = 230V, P_{out} = 3kW) in a compact form factor.

Note:
80 PLUS is an efficiency certification standard for computer power supply units, including those used in servers.

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2. Main Components

This chapter describes the main components used in this design.

2.1. SiC MOSFET TW092V65C

This design uses the 650V SiC MOSFET (TW092V65C) as the switching device of the PFC circuit. The main features of the TW092V65C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 92mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V
  (V_{DS} = 10V, I_D = 0.6mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout

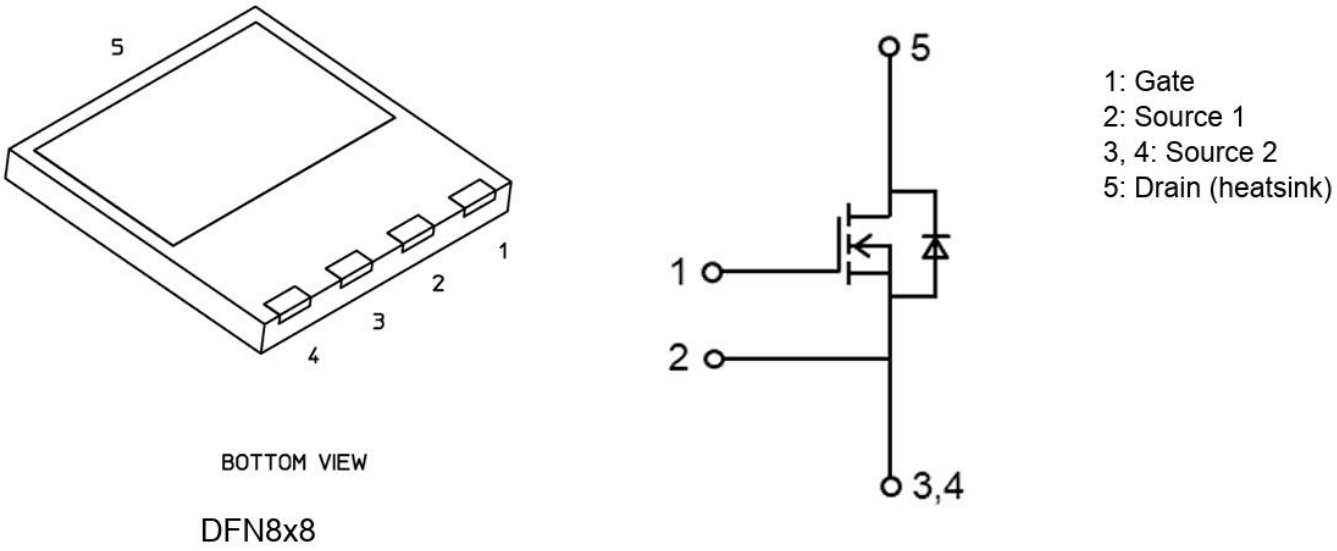


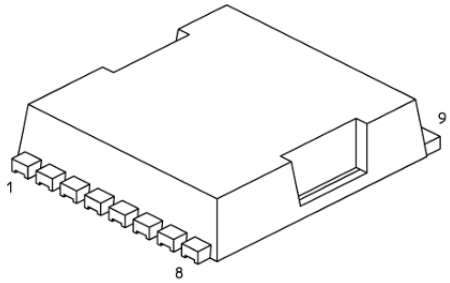
Fig. 2.1 Appearance and Terminal Layout of TW092V65C

2.2. SiC MOSFET TW027U65C

This design uses the 650V SiC MOSFET (TW027U65C) as the primary-side switching device of the PSFB Circuit. The main features of the TW027U65C are as follows:

- Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- Low diode forward voltage: V_{DSF} = -1.35V (Typ.)
- High voltage: V_{DSS} = 650V
- Low drain-source on-resistance: $R_{DS(ON)}$ = 27mΩ (Typ.)
- Less susceptible to malfunction due to high threshold voltage: V_{th} = 3.0 to 5.0V
  (V_{DS} = 10V, I_D = 3mA)
- Recommended gate - source drive voltage: V_{GS_on} = 18V, V_{GS_off} = 0V
- Enhancement mode

Appearance and Terminal Layout



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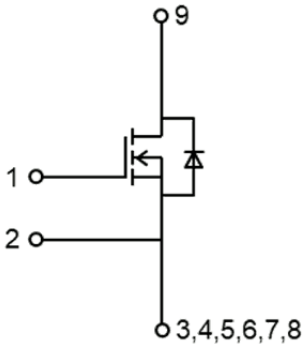

1: Gate
2: Source 1
3, 4, 5, 6, 7, 8: Source 2
9: Drain (heatsink)

Fig. 2.2 Appearance and Terminal Layout of TW027U65C

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2.3. Power MOSFET TPW2900ENH

This design uses the Power MOSFET (TPW2900ENH) as the secondary-side rectifiers of the PSFB Circuit. The main features of the TPW2900ENH are as follows:

- High-speed switching
- Small gate switch charge: Q_{SW} = 8.2nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 24mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 200V)
- Enhancement mode: V_{th} = 2.0 to 4.0V (V_{DS} = 10V, I_D = 1.0mA)

Appearance and Terminal Layout

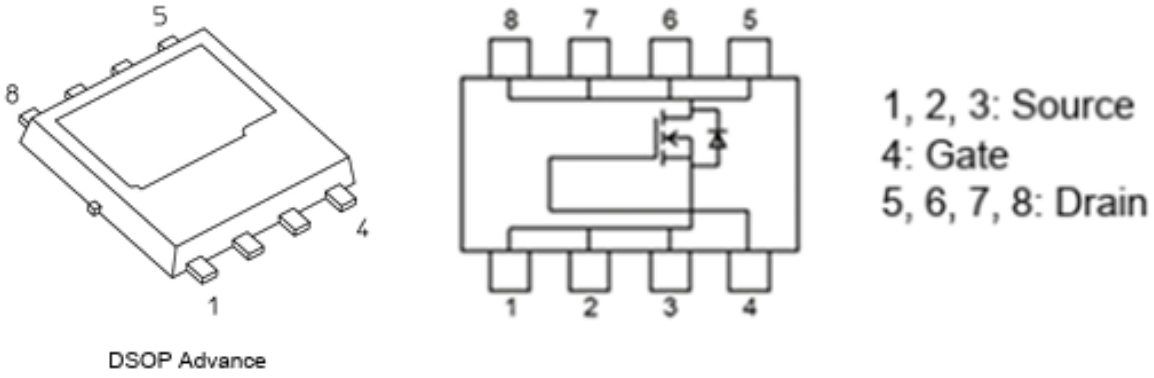

Fig. 2.3 Appearance and Terminal Layout of TPW2900ENH

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2.4. Power MOSFET TPM1R908QM

This design uses the Power MOSFET (TPM1R908QM) as the switching device of the output ORing Circuit. The main features of the TPM1R908QM are as follows:

- High-speed switching
- Small gate switch charge: Q_{SW} = 35nC (Typ.)
- Small output charge: Q_{oss} = 111nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 1.5mΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 80V)
- Enhancement mode: V_{th} = 2.5 to 3.5V (V_{DS} = 10V, I_D = 1.2mA)

Appearance and Terminal Layout

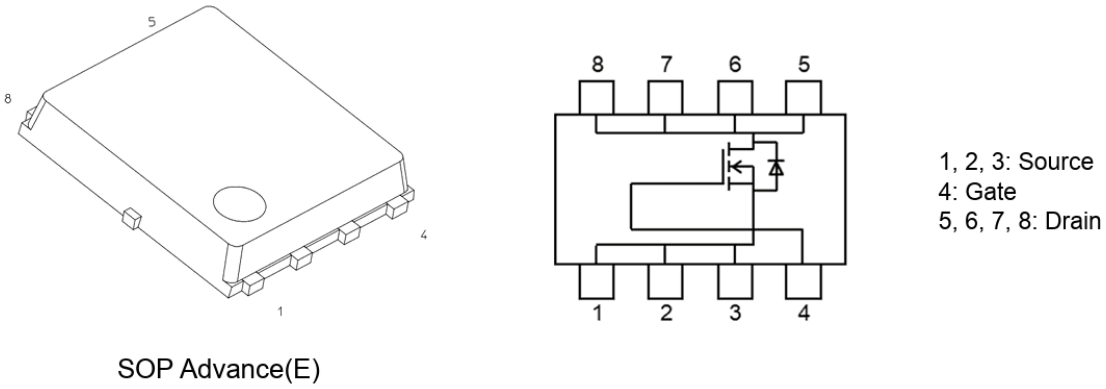

Fig. 2.4 Appearance and Terminal Layout of TPM1R908QM

2.5. SiC Schottky Barrier Diode TRS12V65H

This design uses the SiC Schottky Barrier Diode (TRS12V65H) as the switching device of the PFC Circuit. The main features of the TRS12V65H are as follows:

- Chip design of 3rd generation
- Low forward voltage: V_F = 1.2V (Typ.)
- Low total capacitive charge: Q_c = 33nC (Typ.)
- Low reverse current: I_R = 2.4μA (Typ.)

Appearance and Terminal Layout

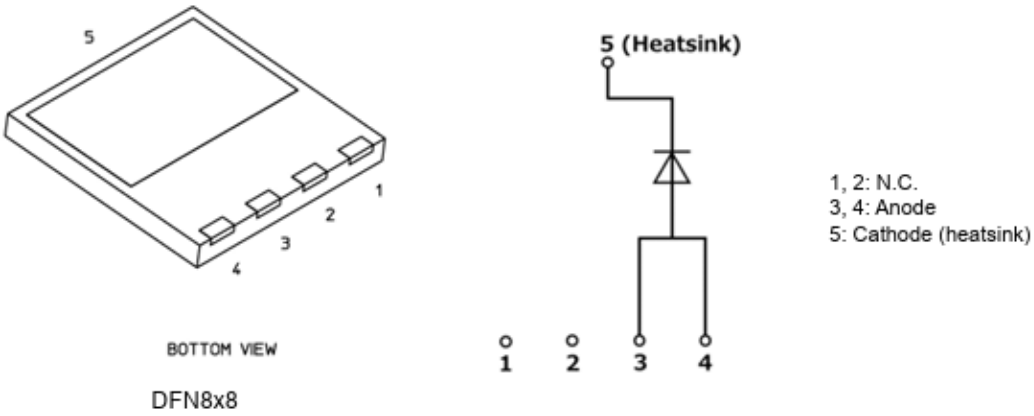

Fig. 2.5 Appearance and Terminal Layout of TRS12V65H

2.6. Digital Isolator DCL540C01

This design uses the 4-channel digital isolator DCL540C01 for signal transmission between the primary-side and secondary-side sides of the PSFB circuit.
The main features of the DCL540C01 are as follows:

- Data rate: Up to 150Mbps
- Supply voltage: 2.25V to 5.5V
- Temperature Range: -40°C to 110°C
- Propagation Delay: 10.9ns (Typ.) (5.0V operation)
- Default Output: High and Low Options
- CMTI: 100kV/μs (Min.)
- Withstand Voltage: 5kVrms
- Safety-Related Certification
  UL : UL1577, File No. E519997
  cUL : CSA Component Acceptance Service Notice No. 5A, File No. E519997
  VDE : DIN EN IEC 60747-17 (VDE V 0884-17) Certificate No.40055132
  CQC : GB 4943.1-2022 Certificate No. CQC22001345018

Appearance and Block Diagram

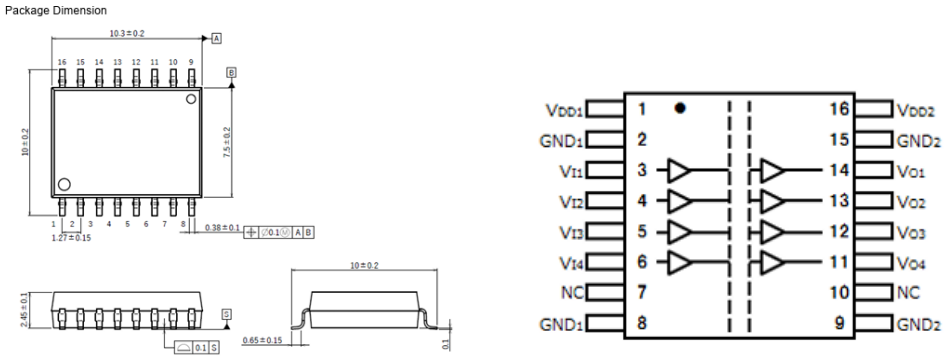

Fig. 2.6 Appearance and Block Diagram of DCL540C01

3. Circuit design

This section describes the points of circuit design of this design.

3.1. AC line circuit design

This section describes the AC line design of this design. The AC line circuit of this design is shown in Fig. 3.1.

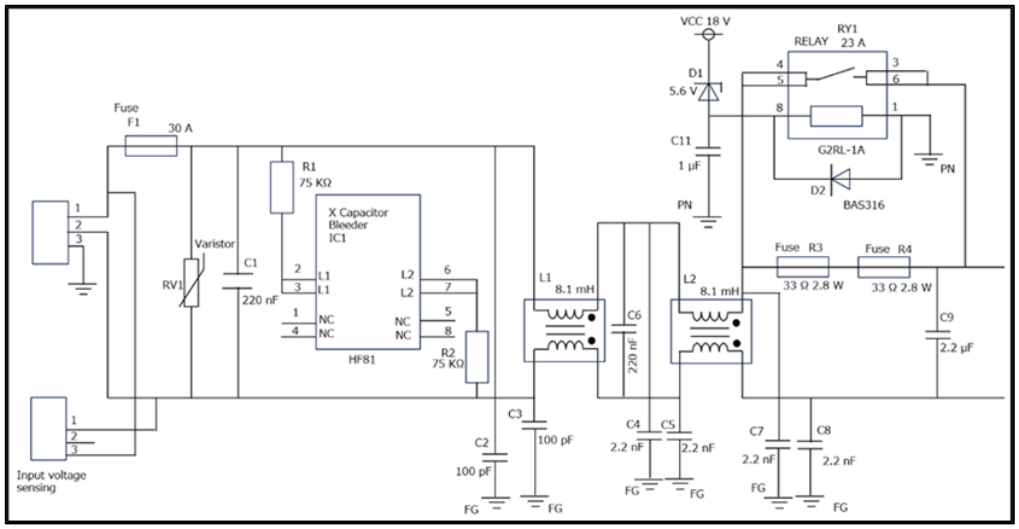

Fig. 3.1 AC Line Circuit

Fuse

A fuse (F1) is installed to shut off the AC line when abnormal current flows through the AC line. Select a fuse from the maximum current value of the AC line. The effective value of the maximum AC line input current is calculated by the following formula.

Maximum AC line input current = maximum power/power supply efficiency/power factor/input phase voltage RMS value (min)

This design is specified to deliver 3kW output when the input is AC 200V. If the power efficiency of the PFC stage remains constant regardless of input voltage, the maximum AC line input current would be the same. However, in general, the efficiency of the PFC stage tends to decrease at lower input voltages. Therefore, when calculating the maximum AC line input current, the minimum input voltage of 180V is used.

Assuming maximum output power of 3kW, power efficiency of 90%, and power factor of 1, input phase voltage (minimum RMS) of 180V, the maximum AC line input current is approximately 18.5A. This design uses a 30A fuse, considering margin. When selecting a fuse, in addition to the above maximum current, it is necessary to consider the inrush current at AC power-on and whether the fuse complies with relevant safety standards.

Varistor

A ceramic varistor (RV1) is implemented to protect the system when surge voltage, such as that caused by lightning induction, is applied to the AC line. The varistor is selected based on the voltage level of the AC line used. This design has a maximum input voltage of 264V RMS and 373V peak. Considering margin for these voltages, a varistor with a voltage rating of 560V (maximum allowable circuit voltage: AC 350V, DC 460V) is used. When selecting a varistor, in addition to voltage ratings, surge current capability and energy tolerance must also be considered. Since the failure mode of varistors is often short-circuit, it is recommended to implement a fuse on the AC input side upstream of the varistor.

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X Capacitor Discharge Circuit

To prevent electric shock when the AC input is disconnected, it is necessary to quickly discharge the charge stored in the X capacitors(*3-1) (C1, C6, C9). This power supply implements the HF81 (IC1) as the discharge IC for the X capacitors. While AC power is supplied, this IC disables the discharge path, contributing to system power savings. When AC power is lost, the circuit composed of this IC and its external resistors (R1, R2) discharges the stored charge in the X capacitors so that the voltage drops to 37% or less of its initial value within 1 second, in accordance with IEC62368. This power supply includes approximately 3μF of X capacitors and therefore implements two 75kΩ resistors as external components to discharge this capacitance. Note that if the X capacitors are changed for noise suppression or other reasons, the resistance values connected to this IC may also need to be adjusted. For cost reduction, it is possible to replace this IC with discharge resistors. However, in that case, continuous power loss due to the discharge resistors will occur while AC is connected, so it is necessary to confirm whether the system's power-saving requirements are still met.

EMI Suppression Components

For common-mode noise suppression, Y capacitors(*3-1) (C2, C3, C4, C5, C7, C8) and common-mode chokes (L1, L2) are implemented. For differential-mode noise suppression, X capacitors (C1, C6, C9) are used. Noise levels are affected by PCB layout and enclosure design. Modify, remove, or add the above components as necessary. Note that increasing the capacitance of Y capacitors may lead to higher leakage current. Therefore, it is necessary to confirm whether the system still complies with the required safety standards.

Note: (*3-1)

X capacitors are connected between the lines of the power supply and act to short high-frequency signals between the lines, thereby reducing noise.
Y capacitors are connected between the power lines and the reference ground, and serve to prevent noise from flowing toward the power lines.

Inrush Current Suppression Components

To suppress inrush current when AC power is applied, fuse-integrated resistors (R3, R4) and a relay (RY1) are implemented. When the power supply is started following the correct procedure, the relay circuit remains off when AC power-on, and current flows through the fuse-integrated resistors (33Ω + 33Ω), allowing inrush current to be suppressed. The relay circuit is designed to turn on after AC power is applied, driven by the internal primary-side 18V power supply. Once the relay is turned on, current flows through the lower-resistance relay path, reducing power loss during operation. It is necessary to confirm that the conditions and timing for turning the relay on and off meet the system's specification requirements.

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3.2. PFC circuit design

3.2.1. Semi-Bridgeless PFC Circuit

Before describing the power supply circuit of this design, an overview of the semi-bridgeless PFC circuit operation is provided. In general power supply circuits, AC input is rectified and then passed through a smoothing capacitor to generate DC output. The AC input current flows only during the period when the input voltage exceeds the voltage across the smoothing capacitor and therefore does not form a sinusoidal waveform. A PFC circuit shapes the input current to resemble a sine wave, eliminating the phase difference between input voltage and current, and improving the power factor toward unity. The bridgeless PFC circuit integrates the bridge diode section and PFC functionality to reduce losses associated with full-wave rectification of AC input.

Fig. 3.2 shows the basic circuit configuration of the bridgeless PFC and the current paths for each half-cycle of the AC input. During the positive half-cycle of the AC input on the L_a side, Q_a performs switching operation, and D_a acts as the output diode for PFC operation. In this period, Q_b operates in synchronous rectification mode throughout the half-cycle to perform rectification of the AC input. Conversely, during the negative half-cycle, Q_b and Dc perform switching operation, while Q_a operates in synchronous rectification mode.

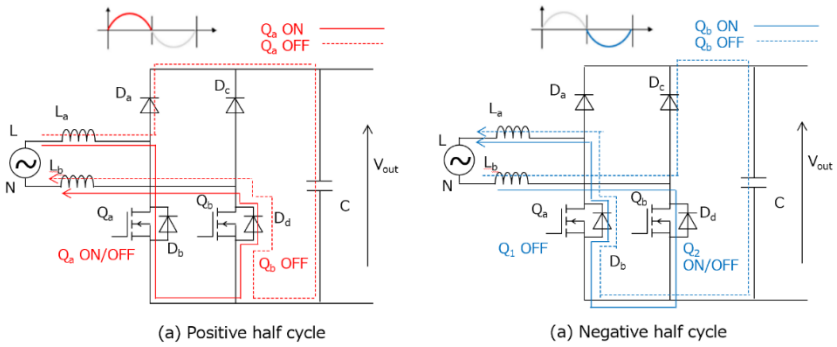

Fig. 3.2 Bridgeless PFC Circuit

Fig. 3.3 shows an example of the semi-bridgeless PFC circuit implemented in this design. This configuration adds diodes to the AC input side of the bridgeless PFC circuit described above. Through two diodes (D_{aa}, D_{bb}), the PFC output ground is connected to the input line, resulting in the input line voltage being referenced to ground rather than floating. Therefore, the input voltage of the PFC circuit becomes a ground-referenced sine wave. As a result, noise issues commonly associated with the bridgeless PFC circuit are suppressed.

D_{cc} and D_{dd} are inrush diodes used to peak-charge capacitor C during initial startup. After the capacitor is charged and the converter begins operation, these diodes no longer contribute to the circuit's behavior.

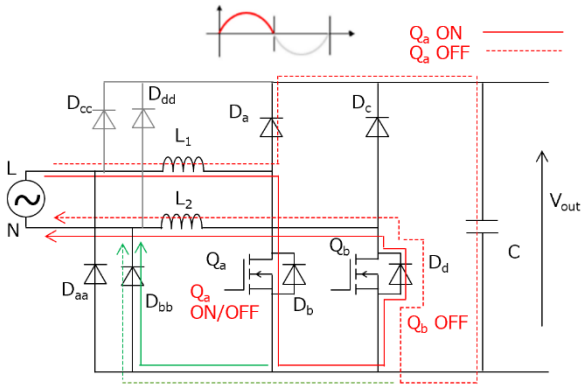

Fig. 3.3 Semi-bridgeless PFC Circuit

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3.2.2. This design's PFC Circuit

This design adopts a semi-bridgeless PFC circuit configuration using the UCC28070A (IC51), a controller manufactured by Texas Instruments (hereafter referred to as the PFC controller). The following section describes the basic design considerations for the semi-bridgeless PFC circuit used in this design. For detailed information regarding the circuitry around the controller, please refer to the UCC28070A datasheet and related documentation.

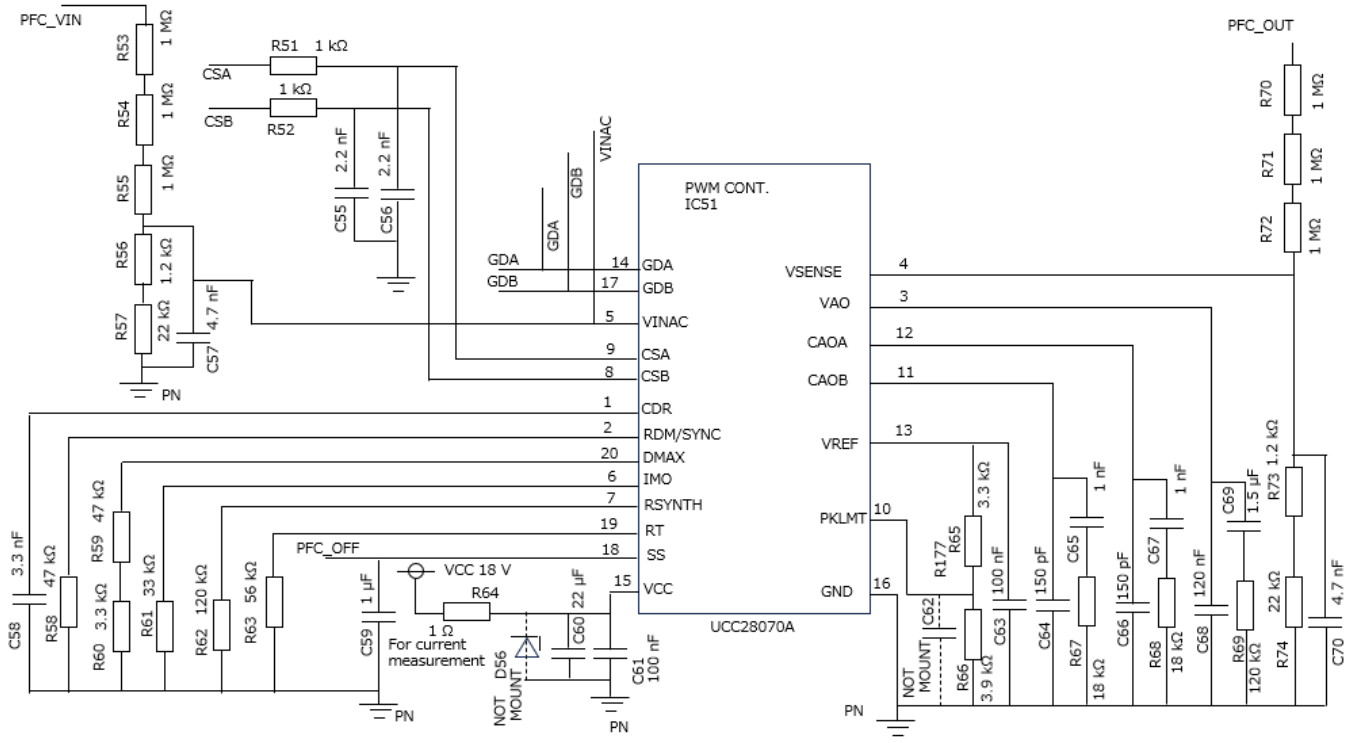

Fig.3.4 PFC Circuit1 (PFC Controller)

Output Voltage Setting

The output voltage of the PFC circuit, V_{PFC_OUT}, can be set using external resistors R70, R71, R72, R73, and R74. The output voltage is controlled by comparing the sensed voltage at the output terminal, VSENSE—divided by the above resistors—with the internal reference voltage (3.0V) of the PFC controller. The output voltage setting value can be calculated using the following formula.

$$V_{out\_PFC} = \frac{3.0 \times (R70+R71+R72+R73+R74)}{(R73+R74)}$$

When changing the output voltage of the PFC circuit, it is also necessary to adjust the resistor values used for AC line voltage sensing: R53, R54, R55, R56, and R57. The initial output voltage setting of the PFC circuit is approximately 391V, based on the following resistor values:
R73 = 1.2kΩ, R74 = 22kΩ, and R70 = R71 = R72 = 1MΩ. Adjust the above resistor values as needed to set the desired output voltage.

Switching Frequency

The switching frequency of the PFC circuit, f_{PWM}, can be set by the external resistor R63 connected to the RT pin of the PFC controller.

$$f_{PWM}(kHz) = \frac{7500}{R63\ (k\Omega)}$$

The initial setting of the switching frequency is 100kHz, with R63 = 75kΩ. Adjust the value of R63 as needed to set the desired switching frequency.

Soft Start

The soft start time of the PFC circuit can be set by the external capacitor C59 connected to the SS pin of the PFC controller.

$$T_{SS}(s) = C59 \times \frac{2.25(V)}{10(\mu A)}$$

The initial setting for the soft-start time is C59 (C_{SS}) = 1µF, which corresponds to approximately 225ms. Change the capacitance value of C59 as needed to set the desired soft-start duration. It is necessary to confirm that the current limiter does not operate during the soft-start period and that the output voltage recovers to the normal range at the restart after the hold-up period.

Current Limiter

The current limiter of the PFC circuit in Fig. 3.5 can be set by the current transformers (T601, T602), the current sense resistors (R602, R610), and the threshold setting resistors (R65, R66) connected to VREF of the PFC controller (Fig. 3.4). The detected values are input to CSA and CSB of the PFC controller, and when the current reaches the threshold, the PFC controller disables the gate drive signals (GDA, GDB) input to INA and INB of the gate driver UCC27524AD. The current limit level I_limit is calculated by the following formula.

$$I\_limit = \left(\frac{P_{PFC\_OUT} \times \sqrt{5}}{efficiency, \eta(\%) \times V_{inAC}} + \frac{\Delta I}{2} \right) \times \text{margin}$$

(The power factor is assumed to be 1.)

The initial setting for the current limit level is 41.04A when V_{inAC} = 180V, P_{PFC_OUT} = 3333W, efficiency η = 90%, ΔI = 10.2A (calculated by the following formula), and margin = 1.2. Change the above values as needed to set the desired current value.

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$$ACin_{peak} = \frac{P_{PFC_{OUT}} \times \sqrt{2}}{V_{inAC} \times \eta} = \frac{3333 \times \sqrt{2}}{180 \times 0.9} = 29.1$$

$$\Delta I = ACin_{peak} \times 35\ \% = 10.2$$

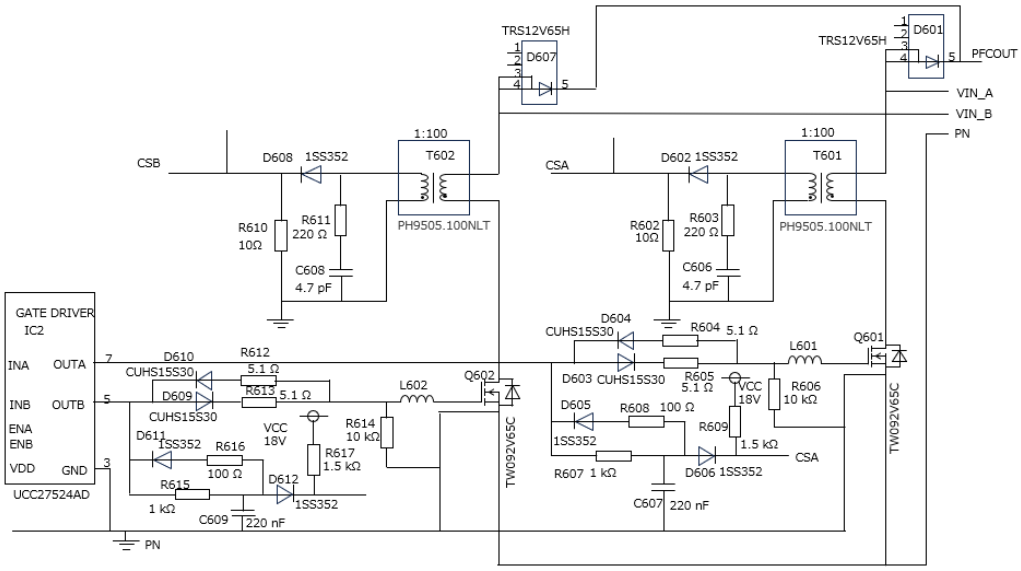

Fig.3.5 PFC Circuit2 (Power MOSFET)

Bridge Diode

Since this design employs a semi-bridgeless PFC circuit configuration, the diodes between pins 2 and 1, and between pins 3 and 1 of the bridge diode D55 (Fig. 3.6) contribute only to the rectification operation during power-up and do not contribute to subsequent operation. This bridge diode (D55) can also be replaced with a half-bridge diode and a surface-mount type diode. When using a surface-mount type diode, it is necessary to select a product with ratings that can support the inrush current.

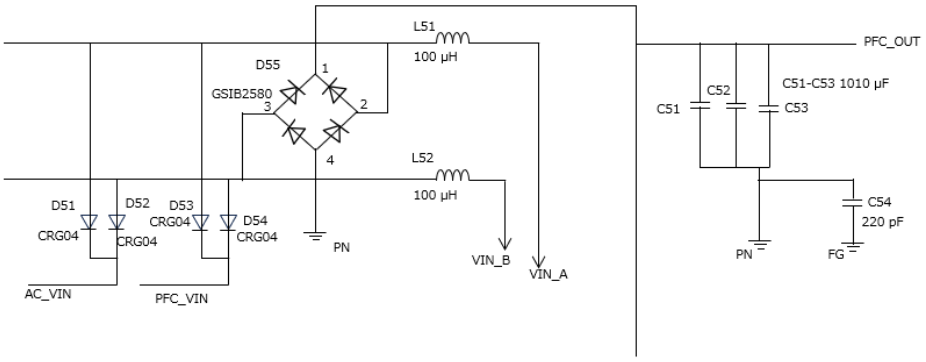

Fig.3.6 PFC Circuit3 (Bridge Diode and Inductor)

Output Capacitor

The capacitance value of the output capacitors (C51, C52, C53) is calculated based on the hold-up time requirement. The hold-up time T_{hold} is determined by the output capacitor capacitance Cout (C51, C52, C53), the output voltage V_{PFC_OUT}, the lower limit of the output voltage V_{min}, and the maximum output power P_{out}. Since the output voltage V_{PFC_OUT} is maintained at the minimum operating voltage V_{min} for the hold-up time T_{hold}, the output power P_{out} is supplied from the output capacitor C_{out} during this period, and the following formula applies.

$$\frac{1}{2} \times C_{out} \times {V_{PFC\_OUT}}^2 - \frac{1}{2} C_{out} \times {V_{min}}^2 = P_{out} \times T_{hold}$$

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$$T_{hold} = C_{out} \times \frac{({V_{PFC_{OUT}}}^2 - {V_{min}}^2)}{2 \times P_{out}}$$

The initial setting is C_{out} = 3030µF, V_{PFC_OUT} = 391V, V_{min} = 280V (*3-2), and P_{out} = 3kW, resulting in a hold-up time of 37.6ms. Adjust the output capacitor value as needed to satisfy the hold-up time required by the system. If an output ripple specification is required, calculate the capacitance necessary to meet the ripple specification and compare it with the capacitance required to satisfy the hold-up time. Use the larger value. In selecting capacitors, tolerance and aging effects must also be taken into consideration.

Note: (*3-2)
This power supply includes a dedicated input monitoring circuit for the DC-DC section. The protection activation voltage is 280V.

Inductor

The selection of the PFC inductors (L51, L52) shown in Fig. 3.6 is based on setting the ripple current ΔI to 35% of the peak AC line input current (AC_{in_peak}). Given the input voltage V_{inAC}, PFC output voltage V_{PFC_OUT}, switching frequency F, and PFC conversion efficiency η, the inductance value can be calculated using the following formula.

$$ACin_{peak} = \frac{P_{PFC_{OUT}} \times \sqrt{2}}{V_{inAC} \times \eta} = \frac{3333 \times \sqrt{2}}{180 \times 0.9} = 29.1$$

$$\Delta I = ACin_{\text{peak}} \times 35\ \% = 10.2$$

In this design, P_{PFC_OUT} = 3333W, V_{inAC} = 180V, and efficiency η = 90%. The inductance value is determined by the maximum voltage applied during the on-time of the PFC switching device (MOSFETs), the on-time (switching time T × on-duty), and the current variation ΔI, and can be expressed using the following formula.

$$L = V \times \frac{dt}{di} = \sqrt{2} \times V_{inAC} \times \frac{T \times D}{\Delta I}$$

Here, T can be expressed using the switching frequency F of the MOSFETs as shown in the following formula.

$$T = \frac{1}{F}$$

The duty of the PFC circuit can be expressed using the following formula.

$$D = \frac{V_{PFC_{OUT}} - \sqrt{2} \times V_{inAC}}{V_{PFC_{OUT}}}$$

By substituting the formulas for T and D into the formula for the inductor L, the following formula is obtained.

$$L = \sqrt{2} \times V_{inAC} \times \frac{(V_{PFC\_OUT} - V_{inAC})}{V_{PFC\_OUT} \times \Delta I \times F}$$

In this design, with V_{inAC} = 180V, V_{PFC_OUT} = 391V, F = 100kHz, and ΔI = 10.2A, the calculated inductance is 87.1µH. Therefore, a 100µH inductor is used.

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3.3. Phase-Shift Full-Bridge (PSFB) Circuit Design

3.3.1. PSFB Circuit

Fig. 3.7 shows the block diagram of the PSFB circuit. The primary side of the transformer (Transformer) is configured as a full-bridge circuit. Q_{AH} and Q_{BL} are switched with a duty ratio of 50% and a phase difference of 180 degrees, respectively. Q_{CH} and Q_{DL} operate in the same manner. The basic operation involves switching Q_{AH} and Q_{BL} on and off, followed by switching Q_{CH} and Q_{DL} with a certain phase delay. The amount of phase shift determines the overlap between diagonally positioned switches—Q_{AH} and Q_{DL}, Q_{BL} and Q_{CH}—and thus the amount of energy transferred to the secondary side. The output voltage is expressed using the following formula. In general, the legs of Q_{AH} and Q_{BL} are referred to as the "leading legs," while those of Q_{CH} and Q_{DL} are called the "lagging legs."

The PSFB circuit can handle high power levels because switching losses are significantly reduced by the Zero Volt Switching (ZVS) operation of the switching devices.

$$V_{out} = \frac{n_2}{n_1} V_{in} \alpha$$

V_{out}: Output voltage[V], V_{in}: Input voltage[V]
n1: Number of primary-side transformer windings
n2: Number of secondary-side transformer windings
α: Phase shift ratio T1 / (T1 + T2)
T1: Simultaneous on-time of Q_{AH} and Q_{DL}, T2: Simultaneous on-time of Q_{BL} and Q_{DL}

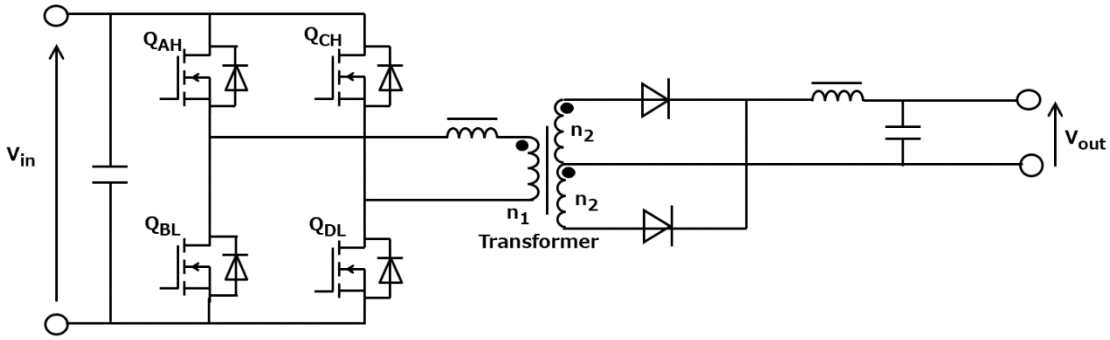

Fig.3.7 PSFB Circuit

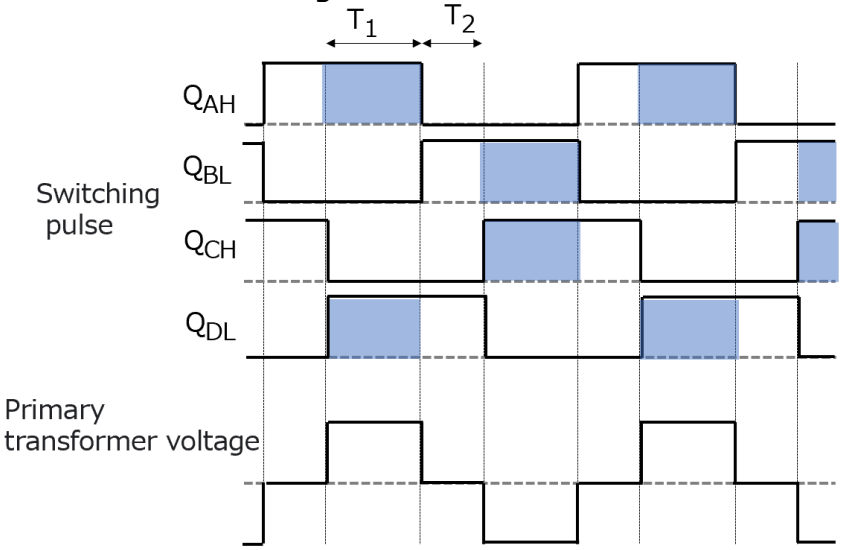

Fig.3.8 PSFB Waveform

3.3.2. This design's PSFB Circuit

In this design, a 50V output is generated following the semi-bridgeless PFC circuit. High efficiency is achieved by using the Texas Instruments controller UCC28950 (IC251, hereafter referred to as the PSFB controller), which enables ZVS operation over a wide load range. The following section describes the basic design parameters of the PSFB circuit in this design. For detailed design information around the controller, refer to the UCC28950 datasheet and related documentation. For the detailed specifications of this design, please refer to the reference guide.

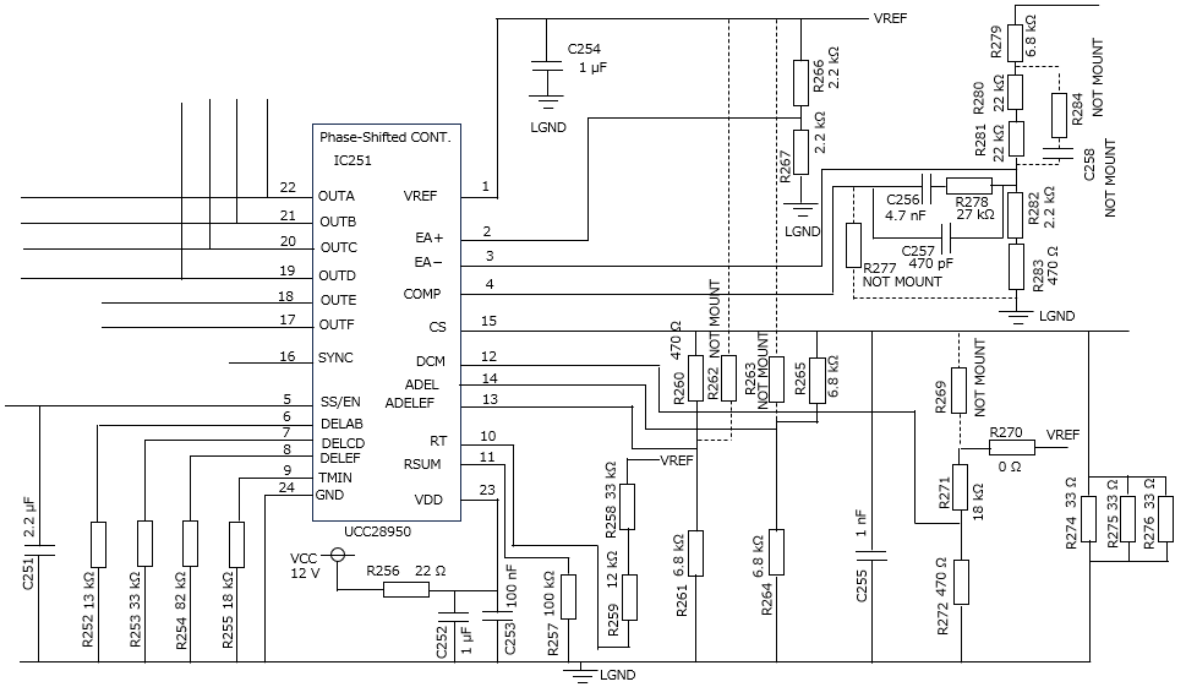

Fig.3.9 PSFB Circuit1 (Controller)

Output Voltage Setting

The output voltage V_{OUT} of the PSFB circuit can be set using the external resistors R266, R267, R279, R280, R281, R282, and R283 shown in Fig. 3.9. The setting value is calculated using the following formula, based on these resistors and the internal reference voltage (VREF = 5.0V) of the PSFB controller UCC28950.

$$V_{out}(V) = \frac{VREF(V) \times R267 \times (R279 + R280 + R280 + R282 + R283)}{(R266 + R267) \times (R282 + R283)}$$

The initial setting for the output voltage of the PSFB circuit is configured with R266 = 2.2kΩ, R267 = 2.2kΩ, R279 = 6.8kΩ, R280 = 22kΩ, R281 = 22kΩ, R282 = 2.2kΩ, and R283 = 470Ω, resulting in $V_{OUT} \fallingdotseq$ 50V. Adjust the above resistor values as needed to set the desired output voltage.

Switching Frequency

The switching frequency f_{PWM} of the PSFB circuit can be set using the external resistors R258 and R259 connected between the RT and VREF terminals of the IC. The switching frequency is calculated using the following formula.

$$f_{PWM}(kHz) = \frac{2.5 \times 10^3}{\left(\frac{R258(k\Omega) + R259(k\Omega)}{VREF(V) - 2.5} + 1\right)}$$

In this formula, the unit of RT is kΩ, VREF is in volts, and f_{PWM} is in kHz. This formula is an empirical approximation, and the units are not dimensionally consistent. The initial setting for the switching frequency is R258 + R259 = 45kΩ, which results in approximately 130kHz. Adjust the resistor values as needed to set the desired frequency.

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Soft Start

The soft-start time of the PSFB circuit can be set using the external capacitor C251 connected between the SS/EN terminal and ground, along with the internal charging current of 25μA (Typ.). The setting value can be calculated using the following formula. In this formula, 0.55V is the voltage at the SS/EN terminal, and VNI is the voltage at the EA+ terminal.

$$T_{SS}(s) = \frac{C251 \times (VNI + 0.55)}{25(\mu A)}$$

$$= \frac{C251 \times \left(\frac{VREF(V) \times R267}{R266 + R267} + 0.55\right)}{25(\mu A)}$$

With R266 and R267 set to 2.2kΩ and VREF at 5V, the initial soft-start time is configured with C251 = 2.2μF, resulting in approximately 268ms. Adjust the capacitance value of C251 as needed to set the desired soft-start duration. It is necessary to confirm that the current limiter does not operate during the soft-start period.

Gate Drive Circuit

The design of the gate drive circuit shown in Fig. 3.10 affects both power supply efficiency and EMI noise. In general, there is a trade-off between efficiency and EMI noise, so a balanced design approach is required. Although ZVS is implemented in the PSFB circuit, if a hard-switching region exists and is identified as the source of EMI noise, it is recommended to increase the gate series resistors (R705, R706, R708, R709) of the corresponding MOSFETs (Q701, Q702) and verify the results.

Similar to the gate drive circuit of the PFC stage, the PSFB gate drive circuit allows independent adjustment of turn-on and turn-off speeds. Therefore, if the issue can be addressed by adjusting only one of them, it may help reduce the impact on overall power supply efficiency.

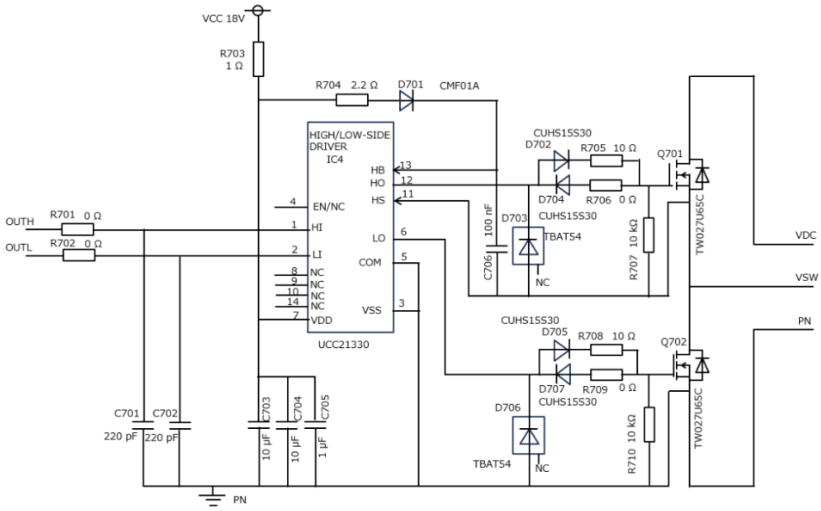

Fig.3.10 PSFB Circuit2 (Primary-side MOSFET)

Current Limiter

The current limiter of the PSFB circuit can be set using the current transformer (T101) shown in Fig. 3.11, the current sense resistors (R274 // R275 // R276) connected between the CS terminal of the PSFB controller and GND in Fig. 3.9, and the current limit threshold (2V). When the voltage generated by the current flowing through the CS terminal and the sense resistors reaches the threshold, the PSFB controller regulates the primary-side MOSFETs to prevent abnormal current from flowing to the secondary side. The current limit level is calculated using the following formula.

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$$I\_limit = \frac{2.0}{(R274//R275//R276) \times transfomer\ turns\ ratio}$$

The initial setting for the current limiter is R274 // R275 // R276 = 11Ω, and with a transformer turns ratio of 100:1, the current limit level is set to 18.2A. Adjust the above values as needed to set the desired current level.

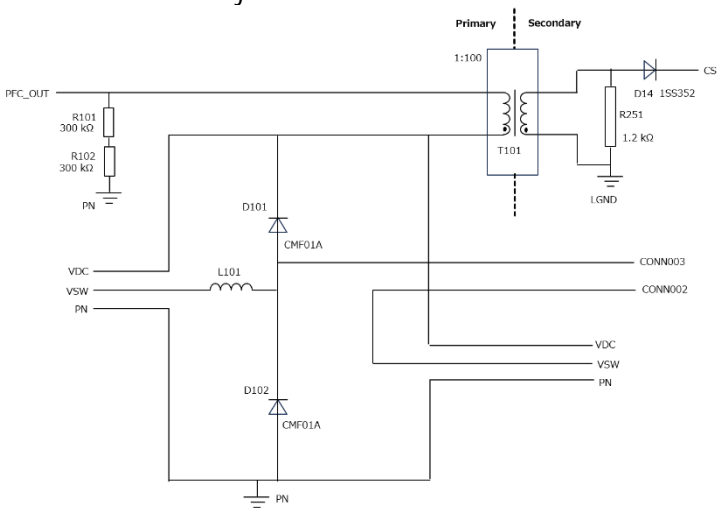

Fig.3.11 PSFB Circuit3 (Current Limit Circuit)

Transformers

The secondary-side circuit of the PSFB is shown in Fig. 3.12. The synchronous rectifier circuit on the secondary side consists of two parallel circuits using transformers T_{PSFB1} and T_{PSFB2}.

When the on-duty of the synchronous rectifier side in steady-state operation is set to 85%, and the output voltage is 50V, a square waveform of approximately 60V is required on the secondary side. Since the PFC output voltage in this design is 391V, the turns ratio of the primary and secondary windings of the transformers (T_{PSFB1}, T_{PSFB2}) is selected as 16:3:3 (center-tapped configuration). This results in a square waveform of approximately 58.65V on the secondary side. In addition, insulation voltage between primary and secondary, winding temperature rise, magnetic flux saturation, and core loss must be carefully considered.

This design also utilizes a resonant coil (L101) in addition to the transformer's leakage inductance to achieve ZVS. If resonance is insufficient, ZVS may not be realized, potentially leading to reduced power efficiency and increased EMI noise. Therefore, when replacing the transformer, it is necessary to verify that ZVS is achieved across a wide load range and adjust the resonant coil accordingly.

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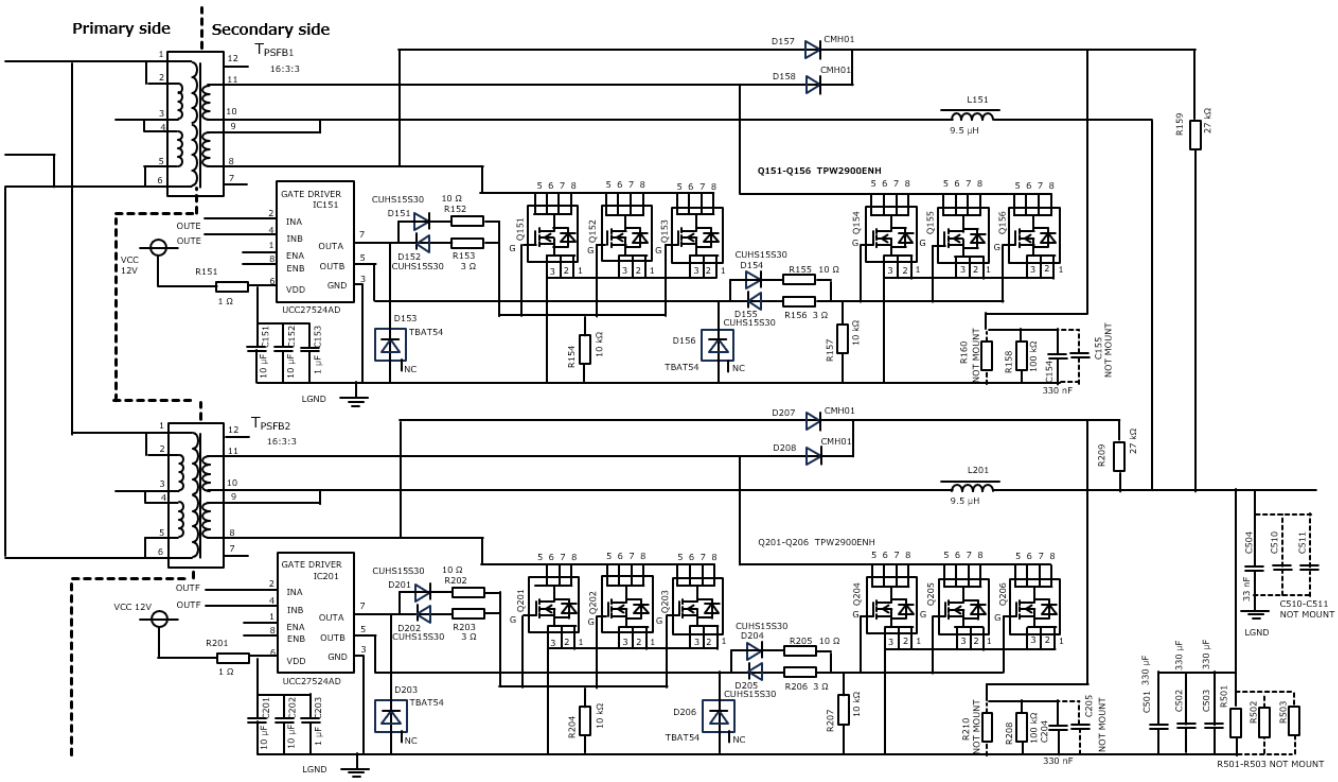

Fig.3.12 PSFB Circuit4 (Secondary-side MOSFETs)

Output Capacitor

The output capacitors are determined based on the output voltage ripple range required by the system. The output voltage ripple V_{ripple} is a composite waveform generated by the ripple current ΔI caused by switching, and the voltages generated by the ESR, capacitance (Cap), and ESL of the output capacitors.

Assuming the switching voltage applied to the center tap is V_{sw}, the output voltage is V_{out}, and the switching frequency is F (Fig. 3.12), the voltages generated by ESR, Cap, and ESL can be calculated using the following formulas.

$$V_{ripple_{ESR}} = \Delta I \times ESR$$

$$V_{ripple_{Cap}} = \frac{\Delta I}{8 \times C_{out} \times F \times 2}$$

$$V_{ripple_{ESL}} = \frac{V_{SW} \times ESL}{L}$$

$$\Delta I = \frac{(V_{SW} - V_{out}) \times V_{out} \times 2(phases)}{V_{SW} \times F \times 2 \times L}$$

therefore, with V_{sw} = 58.65V, V_{out} = 50V, F = 130kHz, and L = 9.5µH, the ripple current ΔI is calculated to be 5.97A.

Most of the output ripple voltage generated by each element is attributed to V_{ripple_ESR}.

The ESR of the capacitors used (C501–C503, EKZN630ELL331MJ25S) is 37mΩ, and since three capacitors are used in parallel, the effective ESR becomes 12.3mΩ. The V_{ripple_ESR} can be calculated using the following formulas.

$$V_{ripple_{ESR}} = \Delta I \times ESR = 5.97 \times 12.3m = 73.4mV$$

To satisfy the ripple voltage requirements of the system, it is necessary to adjust the capacitance of the output capacitors. Additionally, it must be confirmed that the undershoot and overshoot occurring at the output during sudden load changes are within the specified voltage range, and that the allowable ripple current of the output capacitors is ensured.

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3.4. Communication Between Primary-side and Secondary-side in PSFB

As shown in Fig. 3.13, a 4-channel digital isolator DCL540C01 is used for signal transmission between the primary and secondary sides of the PSFB circuit. The MOSFETs drive signals for the primary-side full-bridge circuit, output from the PSFB controller located on the secondary side, are transmitted through the DCL540C01.

Whereas a photocoupler integrates a light emitting diode (LED) and a light-receiving element in the same package, electrically isolating them with a light-transmitting resin and transmitting signals by turning the LED on and off, a digital isolator integrates a modulation chip and a demodulation chip with an insulating layer in the same package and transmits signals via magnetic or electric fields (magnetic coupling).

The DCL540C01 adopts our proprietary magnetically coupled isolation transmission method, achieving a high CMTI (*3-2) of 100kV/μs (Min.), which contributes to stable equipment operation by making it less susceptible to malfunction due to noise. In addition, it achieves a low pulse width distortion of 3.0ns (Max.) and a high-speed transmission rate of 150Mbps (Max.), making it suitable for high-speed communication applications.

Note: (*3-3)

Common-mode (CM) noise is a type of noise that is superimposed on both the signal and ground lines, causing current to flow in the same direction. Digital isolators are used to transmit signals while electrically isolating circuits that are driven by independent power supplies; however, even in such cases, common-mode noise can occur if the potential of one side fluctuates. When this common-mode noise causes the displacement current flowing through the coupling capacitance between the primary (input side) and secondary (output side) inside a standard digital isolator to reach a certain level, it can result in malfunction of the digital isolator and, ultimately, the system.

Therefore, the tolerance to such common-mode noise is important for stable system operation. CMTI represents the ability to withstand high slew-rate transient voltages that occur between grounds. The higher the CMTI, the greater the noise immunity, making the device more suitable for applications requiring isolation.

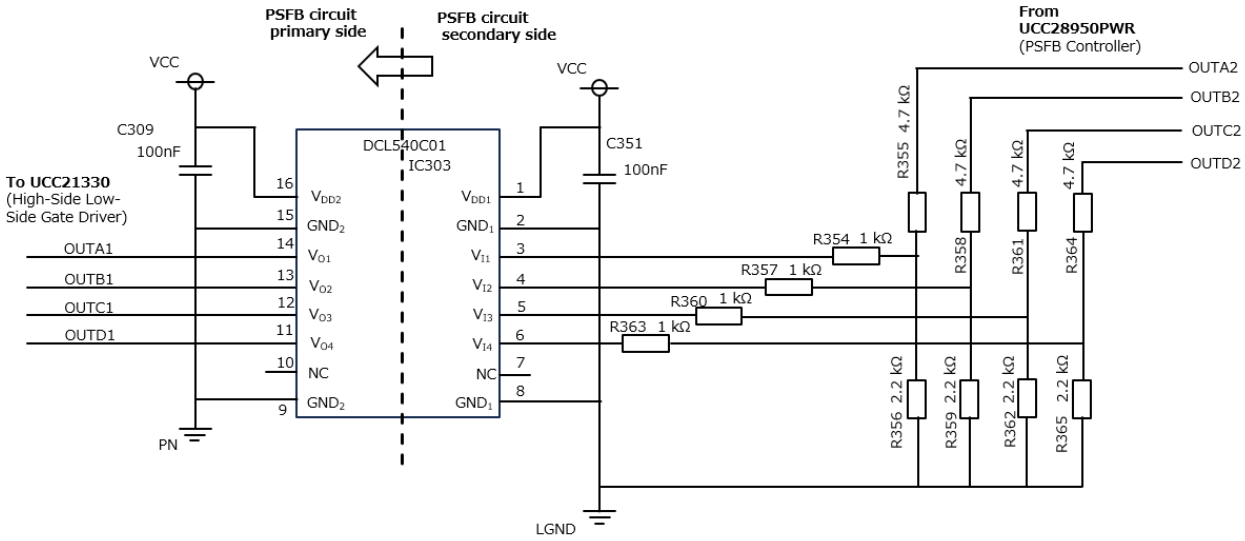

Fig.3.13 Digital Isolator (DCL540C01)

3.5. ORing Circuit Design

This design implements an ORing circuit on the 50V output to support N+1 redundant operation requirements. The ORing circuit consists of a Texas Instruments controller, LM74700-Q1 (IC501), and on/off MOSFETs (Q501–Q504, Q506, Q507). When the output of this design is connected in parallel with other power supplies and the output voltage of this design is higher than that of the other power supplies, the ORing controller turns on the on/off MOSFETs to supply current to the output. Conversely, if the output voltage of this design is lower than that of the other power supplies, the ORing controller turns off the on/off MOSFETs to prevent reverse current from flowing from the other power supplies into this design.

For detailed design of the ORing circuit in this design, please refer to the Texas Instruments LM74700-Q1 datasheet and related documents. The type and quantity of on/off MOSFETs must be selected so that the

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voltage drop and power loss due to on-resistance remain within the system's allowable range when the maximum load (60A) is applied. In this design, six TPM1R908QM devices are implemented.

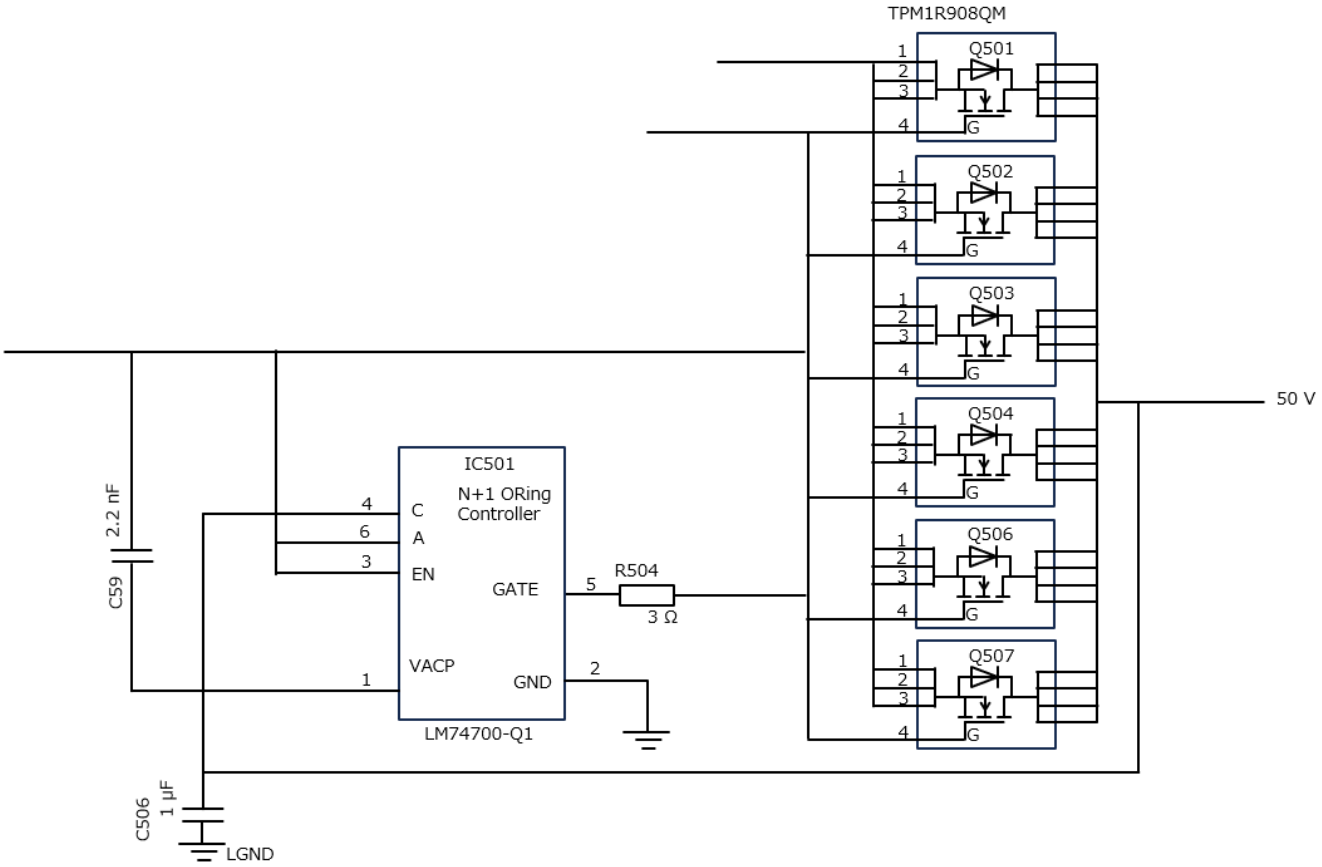

Fig.3.14 ORing Circuit

3.6. Auxiliary Power Supply

As shown in Fig. 3.15, the auxiliary power supply circuit is implemented in this design. This design is equipped with an auxiliary power supply to provide the necessary power for each controller and MOSFET driver IC, allowing operation with only AC input.

The auxiliary power supply adopts a discontinuous current mode (DCM) flyback configuration using the Texas Instruments controller UCC28711, and, in combination with regulator ICs, generates 18V and 5V for the primary side, and 12V and 5V for the secondary-side.

This section describes the transformer design for the auxiliary power supply circuit. For detailed circuit design, please refer to the UCC28711 datasheet and related documents.

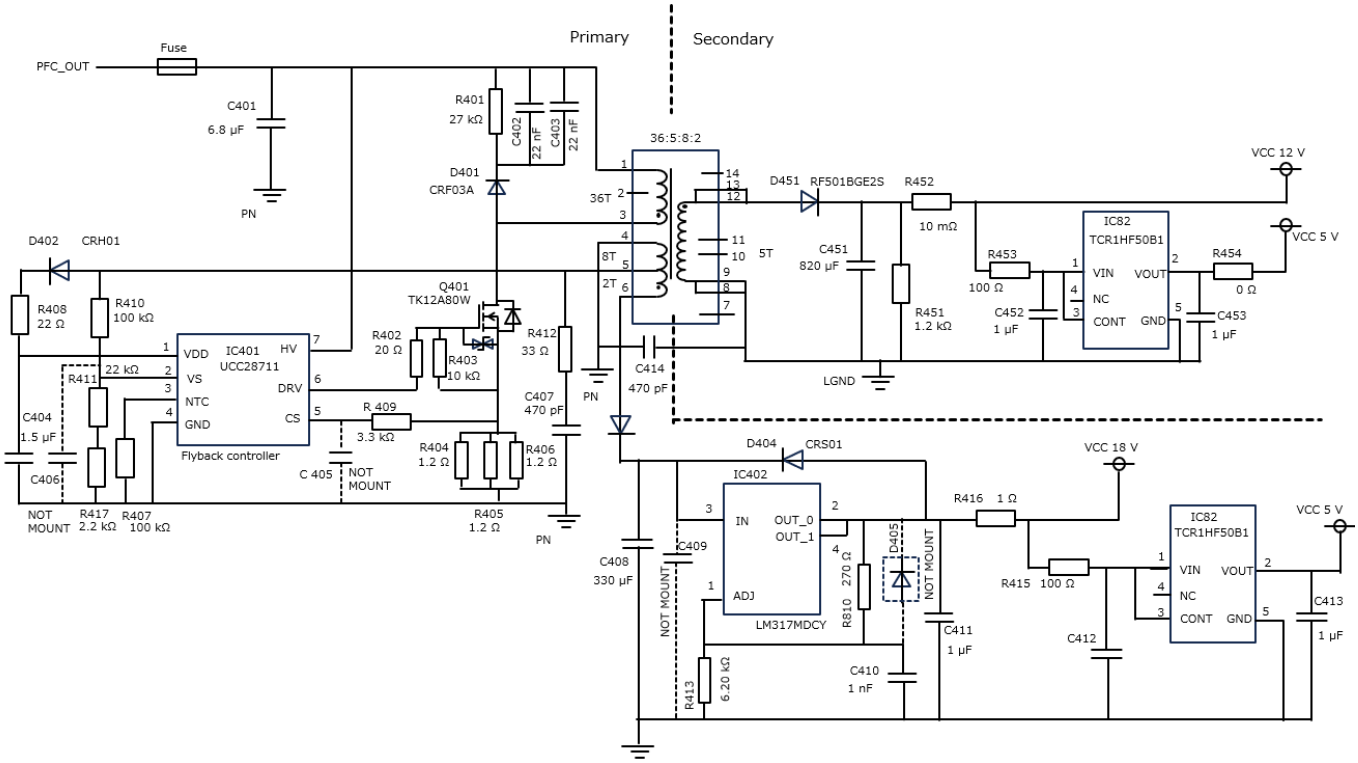

Fig.3.15 Auxiliary Power Supply Circuit

Auxiliary Power Supply Circuit Design

The maximum primary-to-secondary turns ratio, N_{PS} (Max.), can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonance time. First, based on the target switching frequency and DCM resonance time, the maximum available total duty cycle, D_{MAX}, for the on-time and secondary conduction time is determined.

D_{MAX} is calculated using the maximum oscillation frequency, f_{MAX}, of the auxiliary power controller and the DCM resonance time, t_R (assumed to be 1/500 kHz here), according to the following equation.

Once D_{MAX} is known, the maximum turns ratio between the primary and secondary windings can be determined by the following equation. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant current (CC) operation and is internally set to 0.425 by the auxiliary power controller. The total voltage of the secondary winding is the sum of the converter output voltage V_{OCV}, the secondary rectifier voltage V_F, and the cable compensation voltage (V_{OCBC}).

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX}\right) - D_{MAGCC} = 1 - (1\mu s \times 100kHz) - 0.425 = 0.475$$

$$N_{PS(max)} = \frac{D_{MAX} \times V_{Bulk(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_{F(D451-453)} + V_{OCBC}\right)}$$

$$= \frac{0.475 \times 110V}{0.425 \times (12V + 0.68V)} = 9.7$$

V_{OCBC} is the cable compensation voltage, but it is omitted in the calculation.

Here, if the number of turns of the primary winding, N_P, is set to 36 turns, the number of turns of the secondary winding, N_S can be calculated using the following formula.

$$N_S > \frac{N_P}{N_{PS}} = \frac{36}{9.7} = 3.7$$

Therefore, in this design, the number of turns of the secondary winding, N_s is set to 5 turns.

The transformer turns ratio between the secondary winding and the auxiliary winding (N_{AS}) is determined by the shutdown voltage $V_{DD(off)}$ of the auxiliary power controller and the minimum operating voltage V_{OCC} of the PSFB controller.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA(D402)}}{V_{OCC} + V_{F(D451\text{-}453)}} = \frac{(8.5 + 0.68)}{6.15 + 0.71} = 1.34$$

The number of turns of the auxiliary winding, N_{AUX} can be calculated using the following formula.

$$N_{AUX} = N_{AS} \times N_S = 1.34 \times 5 = 6.7$$

Therefore, in this design, the number of turns of the auxiliary winding, N_{AUX}, is set to 8 turns.

The primary-side control voltage is generated as 18V via LDO (IC402) from the output of the auxiliary winding with the increased number of turns.

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