TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75W55FU, TC75W55FK

Dual Operational Amplifier

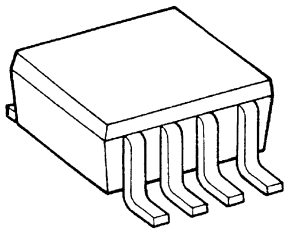
1. General

TC75W55 is a CMOS operational amplifier with low supply voltage, low supply current.

2. Features

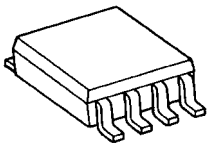
- Low supply voltage : V_{DD} = ±0.9 to 3.5 V or 1.8 to 7 V
- Low supply current : I_{DD} (V_{DD} = 3 V) = 20 μA (Typ.)
- The internally phase compensated operational amplifier.
- Small package

TC75W55FU



SSOP8-P-0.65 (SM8)

TC75W55FK



SSOP8-P-0.50A (US8)

Weight
SSOP8-P-0.65 : 0.021 g (Typ.)
SSOP8-P-0.50A : 0.01 g (Typ.)

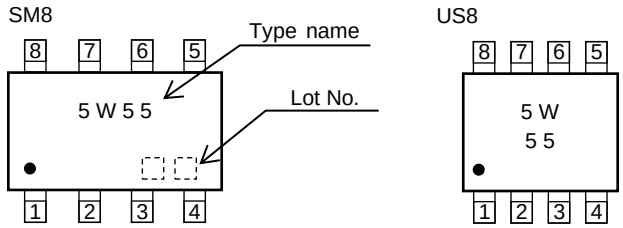
3. Absolute Maximum Ratings (Note) (Ta = 25 °C)

Characteristic	Symbol	製品名	Rating	Unit
Supply voltage	V_{DD}, V_{SS}		7	V
Differential input voltage	DV_{IN}		±7	V
Input voltage	V_{IN}		V_{SS} to V_{DD}	V
Power dissipation	P_D	TC75W55FU	250	mW
		TC75W55FK	200	
Operating temperature	T_{opr}		−40 to 85	°C
Storage temperature	T_{stg}		−55 to 125	°C

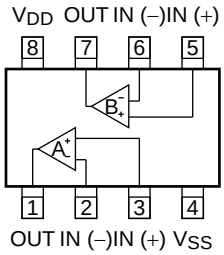
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
1995-06

4. Marking (Top View)



5. Pin Connection (Top View)



6. Electrical Characteristics

6.1 DC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25 °C)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 10 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	2.1	V
Voltage gain (Open Loop)	G_V	—	—	60	70	—	dB
Maximum output Voltage	V_{OH}	3	R_L ≥ 1 MΩ	2.9	—	—	V
	V_{OL}	4	R_L ≥ 1 MΩ	—	—	0.1	
Common mode input signal rejection ratio	CMRR	2	V_{IN} = 0.0 to 2.1 V	60	70	—	dB
Supply voltage rejection ratio	SVRR	1	V_{DD} = 1.8 to 7.0 V	60	70	—	dB
Supply current	I_{DD}	5	—	—	20	40	μA
Source current	I_{source}	6	—	10	20	—	μA
Sink current	I_{sink}	7	—	100	450	—	μA

6.2 DC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25 °C)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	1	R_S = 100 kΩ	—	2	10	mV
Input offset current	I_{IO}	—	—	—	1	—	pA
Input bias current	I_I	—	—	—	1	—	pA
Common mode input voltage	CMV_{IN}	2	—	0.0	—	0.9	V
Voltage gain (Open loop)	G_V	—	—	60	70	—	dB
Maximum output voltage	V_{OH}	3	R_L ≥ 1 MΩ	1.7	—	—	V
	V_{OL}	4	R_L ≥ 1 MΩ	—	—	0.1	
Supply current	I_{DD}	5	—	—	16	32	μA
Source current	I_{source}	6	—	8	16	—	μA
Sink current	I_{sink}	7	—	100	400	—	μA

6.3 AC Characteristics (V_{DD} = 3.0 V, V_{SS} = GND, Ta = 25 °C)

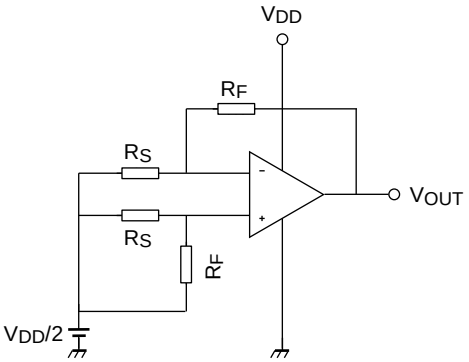
Characteristics	Symbol	TEST Circuit	TEST Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.08	—	V/μs
Unity gain cross frequency	f_T	—	—	—	160	—	kHz

6.4 AC Characteristics (V_{DD} = 1.8 V, V_{SS} = GND, Ta = 25 °C)

Characteristics	Symbol	TEST Circuit	TEST Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	0.06	—	V/μs
Unity gain cross frequency	f_T	—	—	—	140	—	kHz

6.5 TEST Circuit

1. SVRR, V_{IO}



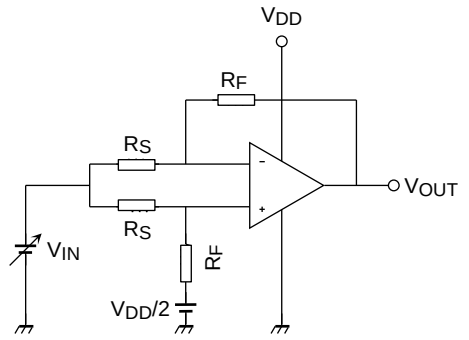
- SVRR
  For each of the two V_{DD} values, measure the V_{OUT} value, as indicated below, and calculate the value of SVRR using the equation shown.
  When V_{DD} = 1.8 V : V_{DD} = $V_{DD}1$, V_{OUT} = $V_{OUT}1$,
  When V_{DD} = 7.0 V : V_{DD} = $V_{DD}2$, V_{OUT} = $V_{OUT}2$

$$SVRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{DD}1 - V_{DD}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- VIO
  Measure the value of V_{OUT} and calculate the value of V_{IO} using the following equation.

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. CMRR, CMV_{IN}

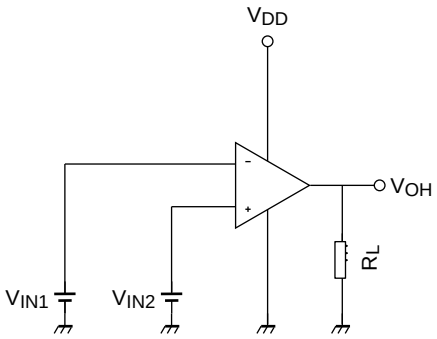


- CMRR
  Measure the V_{OUT} value, as indicated below, and calculate the value of the CMRR using the equation shown.
  When V_{IN} = 0.0 V : V_{IN} = $V_{IN}1$, V_{OUT} = $V_{OUT}1$
  When V_{IN} = 2.1 V : V_{IN} = $V_{IN}2$, V_{OUT} = $V_{OUT}2$

$$CMRR = 20\log\left(\left|\frac{V_{OUT}1 - V_{OUT}2}{V_{IN}1 - V_{IN}2}\right| \times \frac{R_S}{R_F + R_S}\right)$$

- CMV_{IN}
  Input range within which the CMRR specification guarantees VOUT value (as varied by the VIN value).

3. V_{OH}

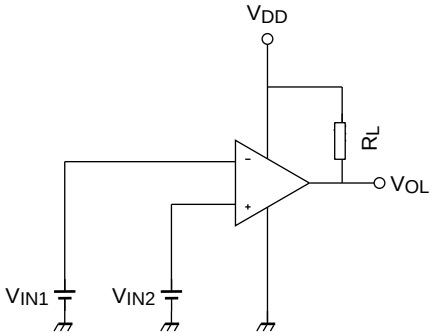


- V_{OH}

  TEST Condition $V_{IN1} = \frac{V_{DD}}{2} - 0.05\ V$

  $V_{IN2} = \frac{V_{DD}}{2} + 0.05\ V$

4. V_{OL}

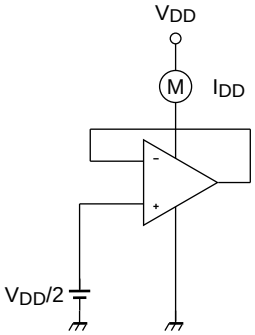


- V_{OL}

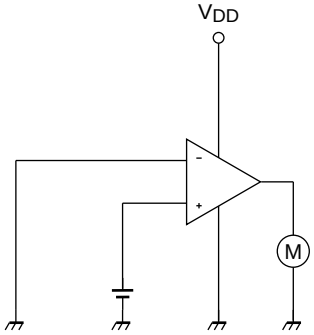
  TEST Condition $V_{IN1} = \frac{V_{DD}}{2} + 0.05\ V$

  $V_{IN2} = \frac{V_{DD}}{2} - 0.05\ V$

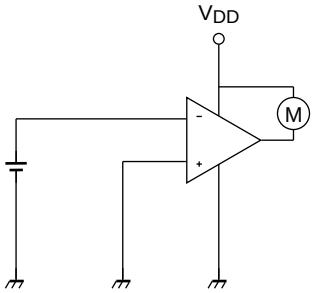
5. I_{DD}



6. Isource

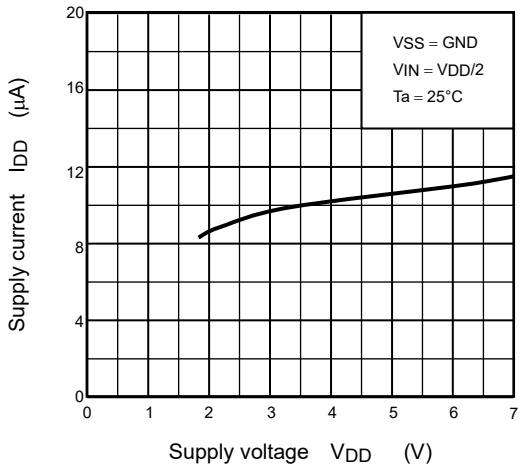


7. Isink

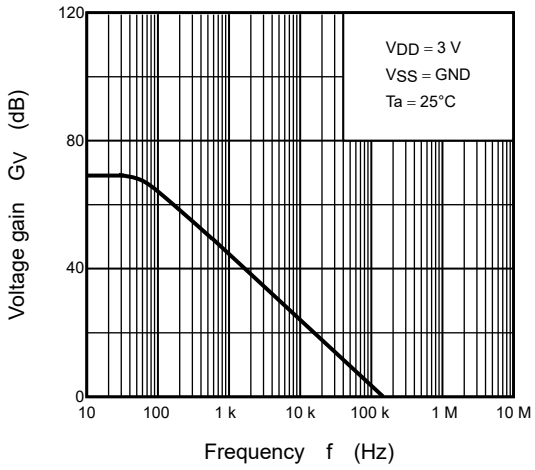


7. Characteristics Curves (Note)

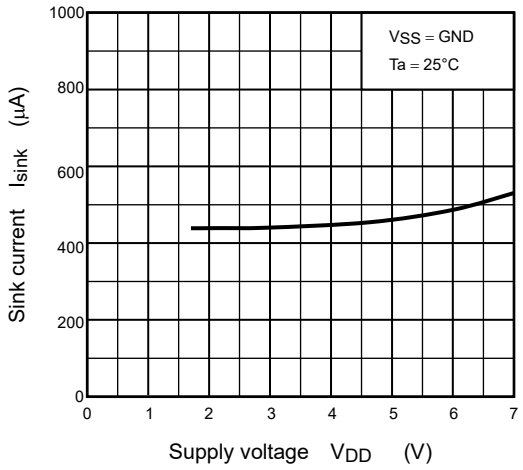
$I_{DD} - V_{DD}$



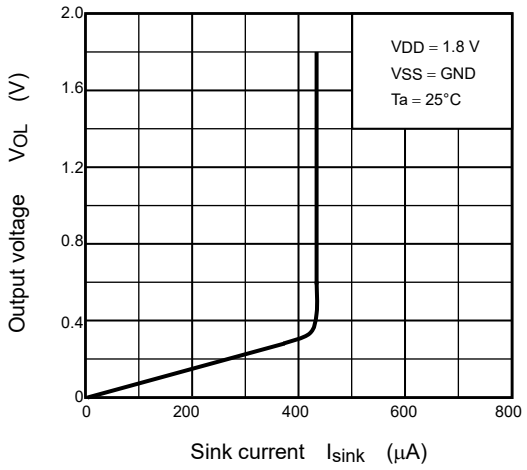
$G_V - f$



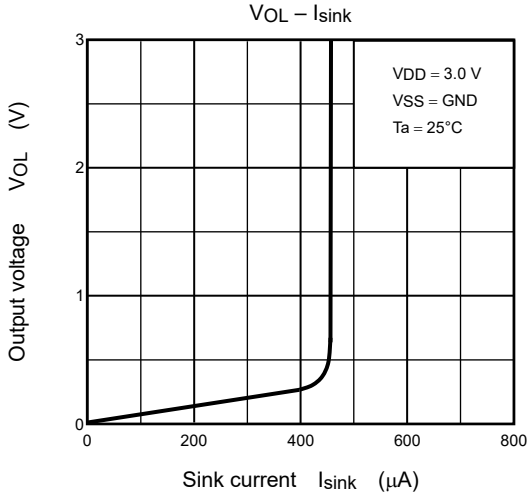
$I_{sink} - V_{DD}$



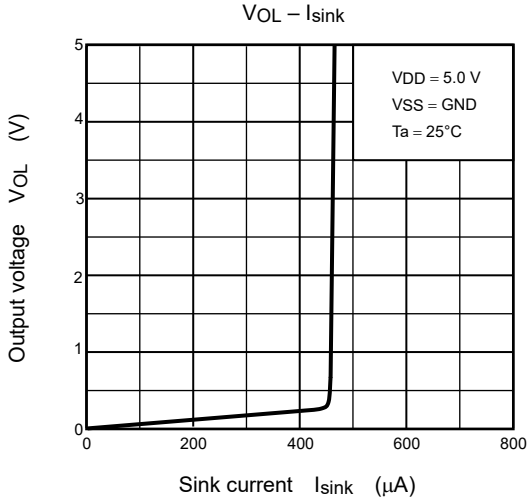
$V_{OL} - I_{sink}$



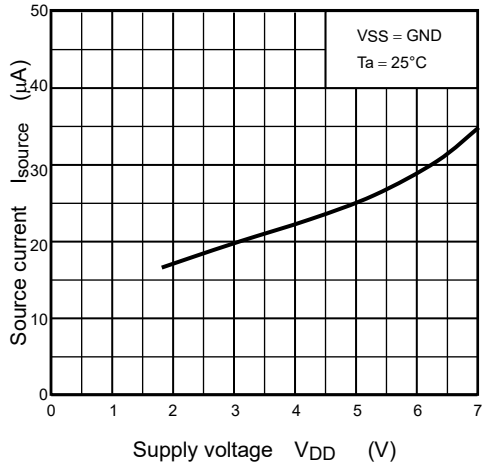
$V_{OL} - I_{sink}$



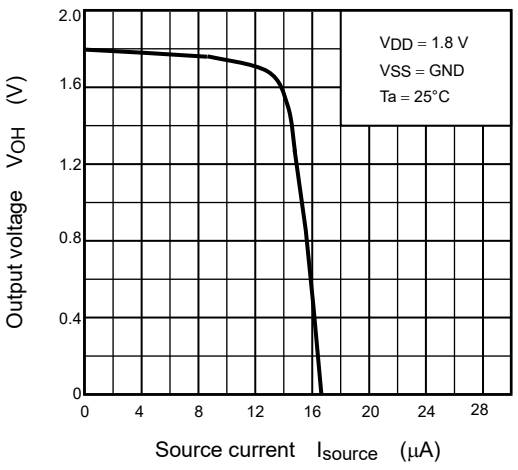
$V_{OL} - I_{sink}$



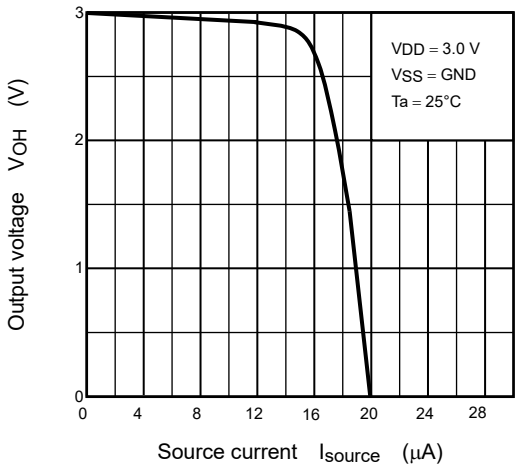
I_{source} – V_{DD}



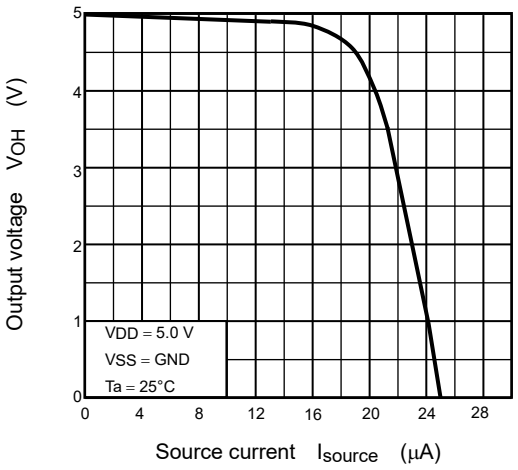
V_{OH} – I_{source}



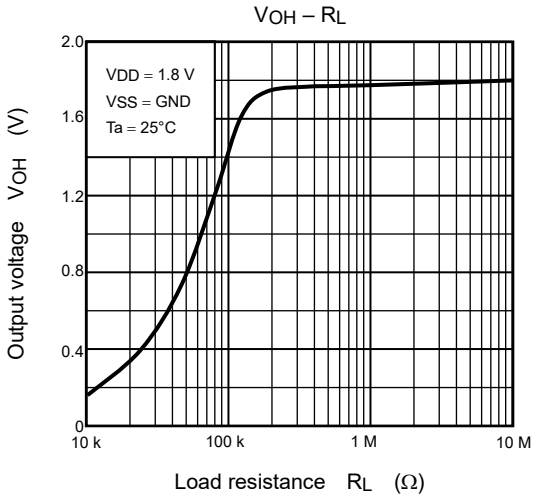
V_{OH} – I_{source}



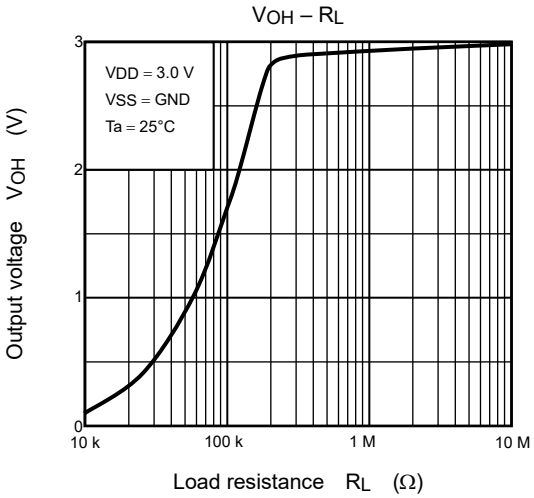
V_{OH} – I_{source}

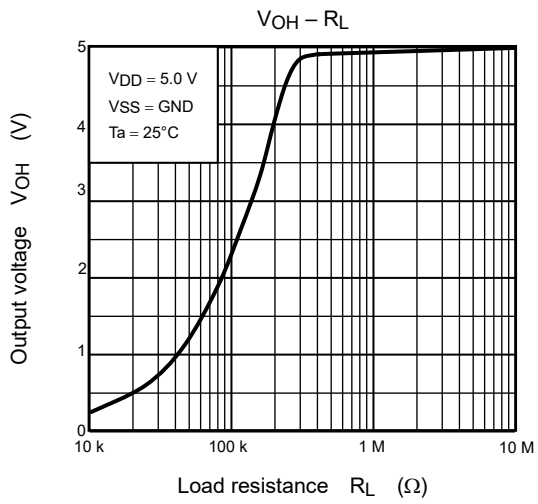


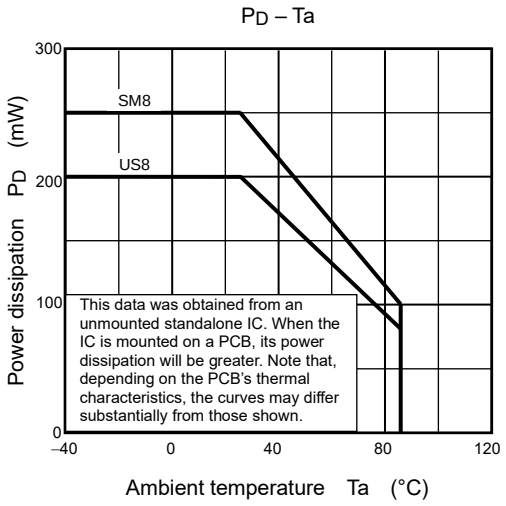
V_{OH} – R_L



V_{OH} – R_L





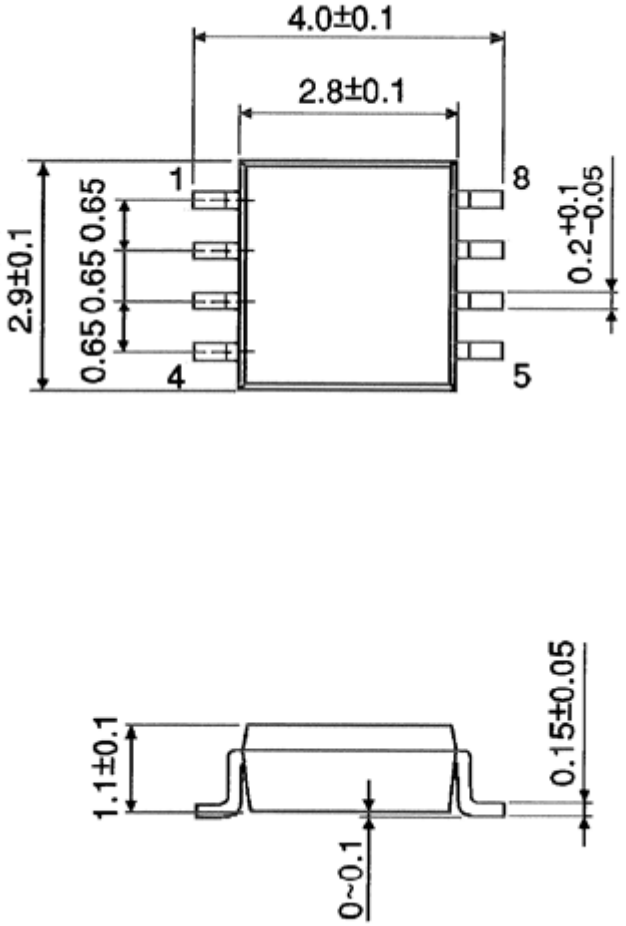


Note The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

8 Package Dimensions

8.1 TC75W55FU

SSOP8-P-0.65 Unit : mm

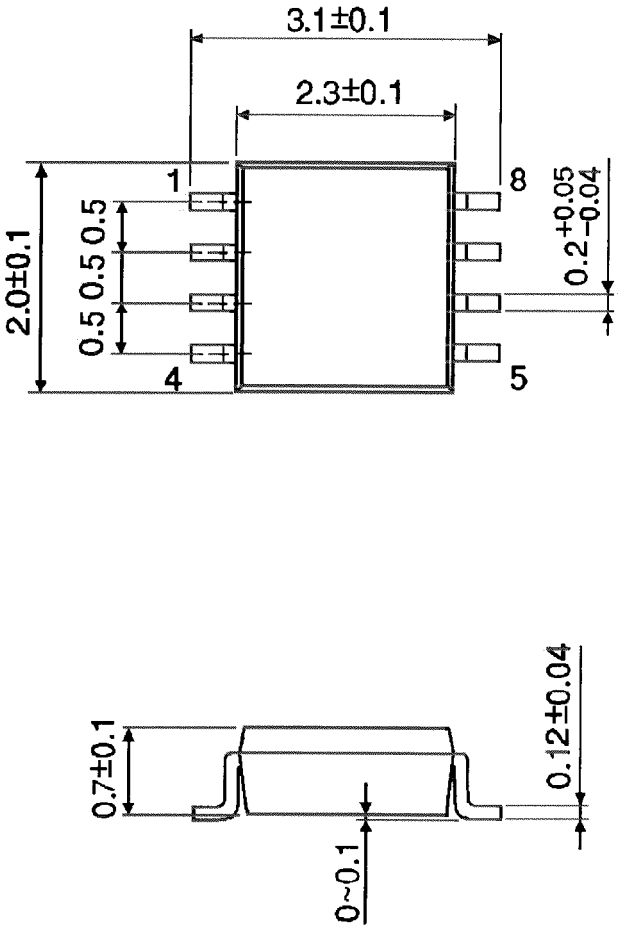


Weight: 0.021 g (typ.)

8.2 TC75W55FK

SSOP8-P-0.50A

Unit : mm



質量: 0.01 g (標準)

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