1.6kW LLC Resonant AC-DC Converter for Servers

Design Guide

RD212-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This Design Guide describes the design methodology of the 1.6kW LLC Resonant AC-DC Converter for Servers (hereinafter referred to as "this design").

With the increase in the amount of information handled daily, the number of data centers is increasing, and the size of data centers is also increasing. Therefore, reducing the power consumption of data centers has become a global issue. Various measures are being considered to reduce power consumption in data centers, and one of them is the use of 48V bus voltages in servers used in data centers, and 48V servers have become increasingly popular in recent years. This design is an AC-DC converter that takes 100V/200V AC input and outputs 54.5V DC to a 48V server.

In order to improve power supply efficiency, following topologies have been used, an active bridge circuit that uses MOSFETs instead of a diode bridge, an interleaved PFC circuit, and a 3-phase LLC resonant DC-DC converter. This allowed to achieve an efficiency that exceeds the Titanium standard of 80 PLUS* at 230V input condition.

Toshiba's latest power MOSFETs like TK024N60Z1 mounted on the active bridge section, TK080N60Z1 mounted on the interleaved PFC section, TK125A60Z1 mounted on the primary side of the 3-phase LLC resonant DC-DC converter, and TPH2R408QM mounted on the secondary side of the 3-phase LLC resonant DC-DC converter and ORing section, and 650V SiC Schottky barrier diodes TRS8E65H mounted on the interleaved PFC contributes to reduced losses and high-efficiency operation.

Toshiba's TMPM372FWUG microcontroller is used to generate the 3-phase control signal for the LLC resonant DC-DC converter.

*80 PLUS: It is the efficiency standard for power supply units for computers such as servers, and Titanium is the name of the highest standard.

2. Main Components Used

This chapter describes the main components used in this design.

2.1. Power MOSFET TK024N60Z1

600V withstand voltage N-channel MOSFETs TK024N60Z1 are used as switching elements of active bridge circuit instead of the diode bridge circuits. The main features of TK024N60Z1 are as follows.

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.02Ω (Typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 3.84mA)

Appearance and Terminal Layout

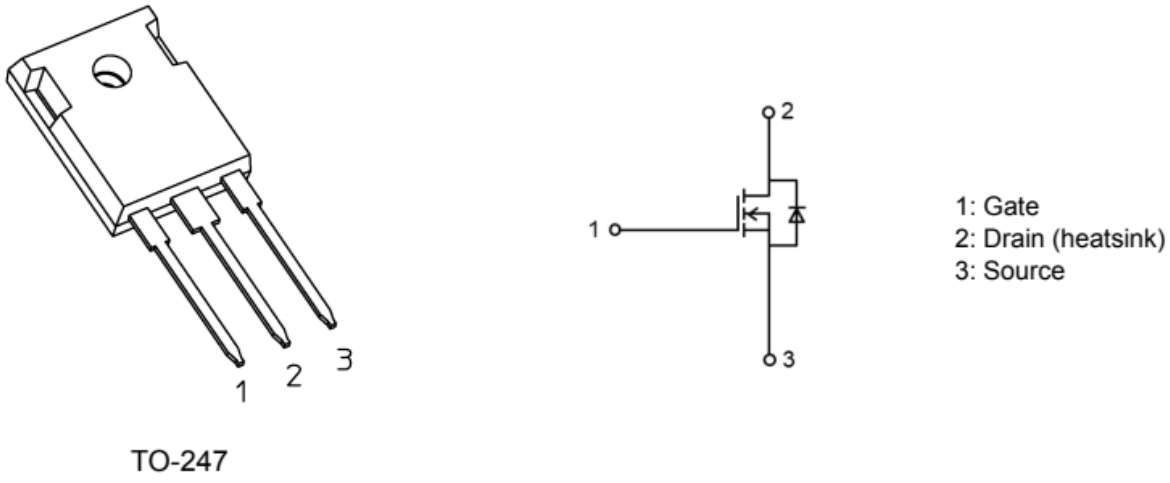


Fig. 2.1 Appearance and Terminal Layout of TK024N60Z1

2.2. Power MOSFET TK080N60Z1

600V withstand voltage N-channel MOSFETs TK080N60Z1 are used as the switching elements of the PFC circuit. The main features of TK080N60Z1 are as follows.

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.067Ω (Typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 1.17mA)

Appearance and Terminal Layout

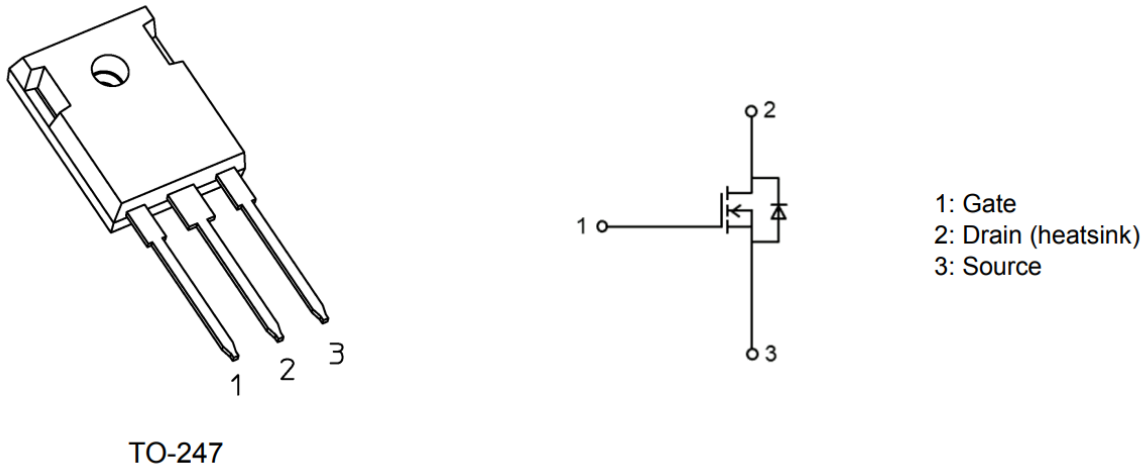


Fig. 2.2 Appearance and Terminal Layout of TK080N60Z1

2.3. Power MOSFET TK125A60Z1

600V withstand voltage N-channel MOSFETs TK125A60Z1 are used as the primary-side switching elements of the LLC resonant DC-DC converter circuit. The main features of TK125A60Z1 are as follows.

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.105Ω (Typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 0.73mA)

Appearance and Terminal Layout

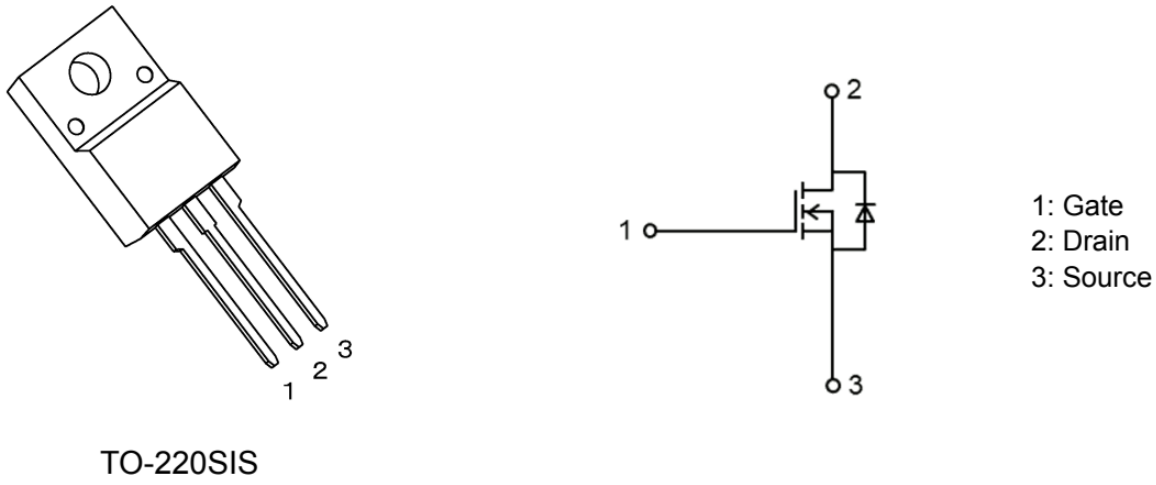


Fig. 2.3 Appearance and Terminal Layout of TK125A60Z1

2.4. Power MOSFET TPH2R408QM

80V withstanding voltage N-channel MOSFETs TPH2R408QM are used as the secondary-side switching elements of the LLC Resonant DC-DC converter circuit and the switching element of the output ORing circuit. The main features of TPH2R408QM are as follows.

- High-speed switching.
- Small gate charge: Q_{SW} = 28nC (Typ.)
- Small output charge: Q_{oss} = 90nC (Typ.)
- Low drain-source on-resistance: $R_{DS(ON)}$ = 1.9nΩ (Typ.) (V_{GS} = 10V)
- Low leakage current: I_{DSS} = 10μA (Max.) (V_{DS} = 80V)
- Enhancement mode: V_{th} = 2.5 to 3.5V (V_{DS} = 10V, I_D = 1.0mA)

Appearance and Terminal Layout

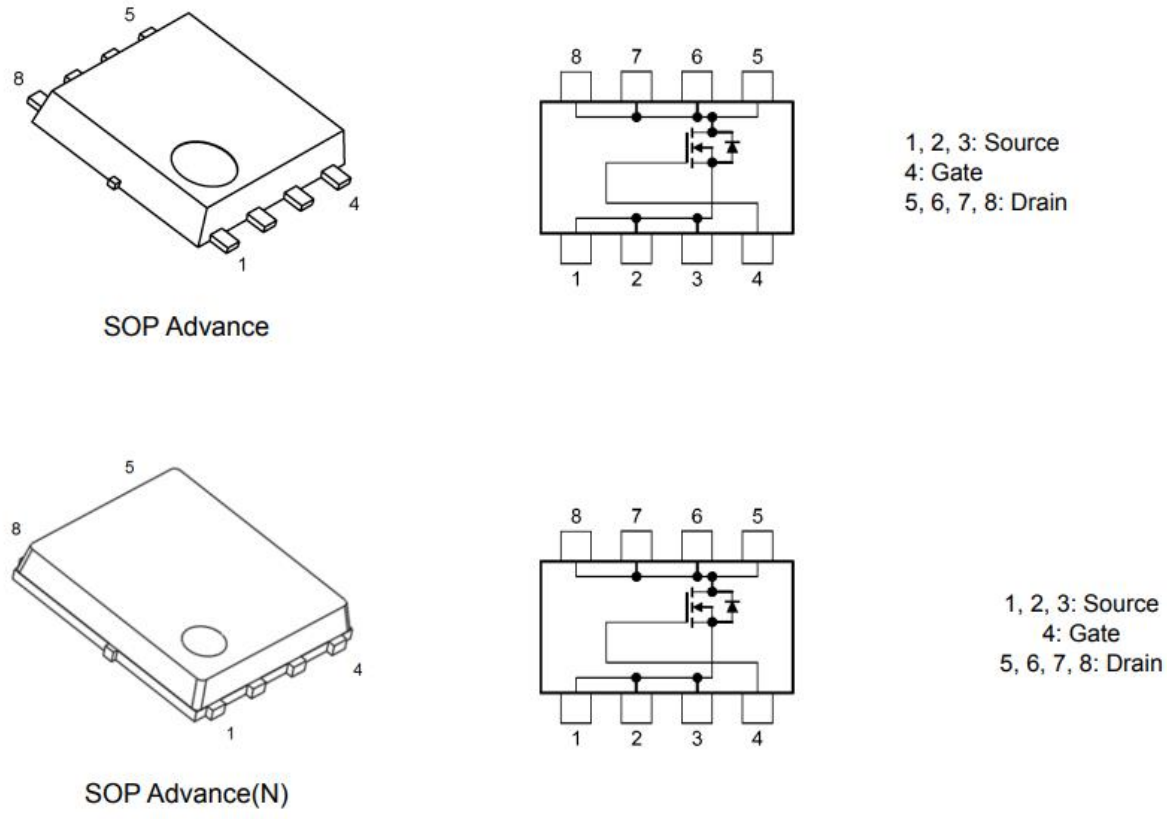


Fig. 2.4 Appearance and Terminal Layout of TPH2R408QM

2.5. SiC Schottky Barrier Diode TRS8E65H

650V system diodes TRS8E65H are used as the rectifiers in the PFC circuit. The main features of TRS8E65H are as follows.

- Chip design of 3rd generation
- Low forward voltage: V_F = 1.2V (Typ.)
- Low total capacitive charge : Q_c = 22nC (Typ.)
- Low reverse current: I_R = 1.5μA (Typ.)

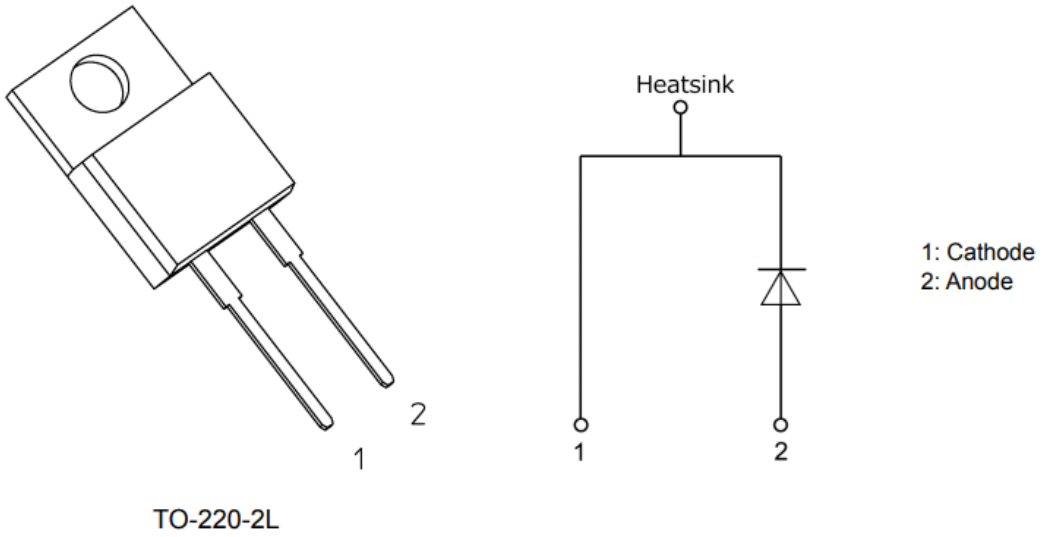


Fig. 2.5 Appearance and Terminal Layout of TRS8E65H

2.6. Microcontroller TMPM372FWUG

Microcontroller TMPM372FWUG is used in the 3-phase control-signal generator of the 3-phase LLC resonant DC-DC converter. The main features of TMPM372FWUG are as follows.

- Arm Coretex-M3 core-equipped, maximum operating frequency: 80MHz (operating temperature -40 to 85°C)
- 16-bit timer/event counter: 8 channels
- 5V voltage-operation
- Tiny package: LQFP44

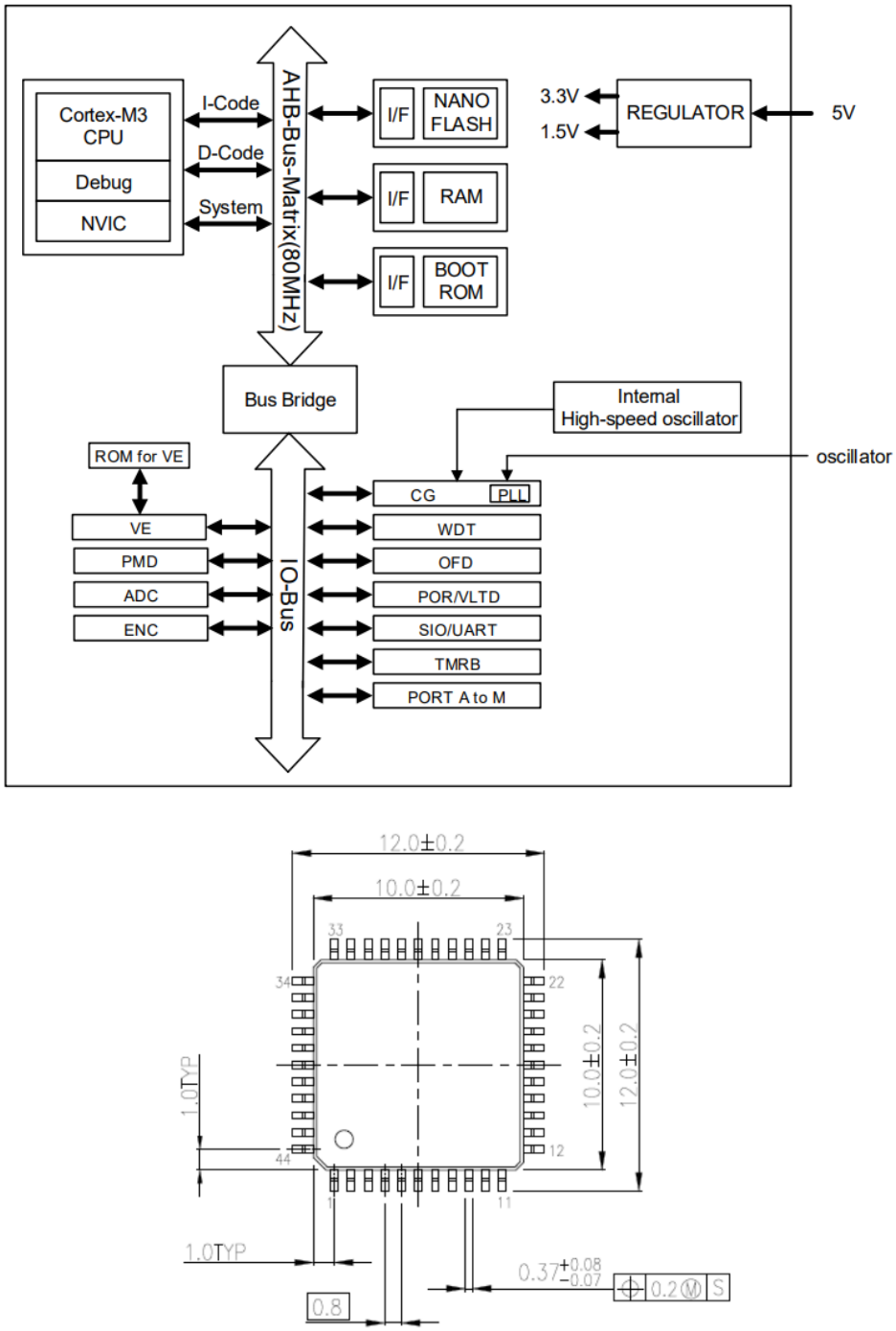


Fig. 2.6 Appearance and Block Diagram of TMPM372FWUG

3. Outline of Interleaved PFC Circuit and 3-Phase LLC Resonant DC-DC Converter

This chapter describes the basic concepts of the interleaved PFC and 3-phase LLC resonant DC-DC converters used in this design.

3.1. Interleaved PFC Circuit

Interleaved PFC circuits, in which multiple step-up converter circuits are arranged in parallel, are becoming increasingly popular in medium to large power supplies that exceed 500W. In principle, three or more phases are possible, but a two-phase system as shown in Fig. 3.1 is common. Here, a circuit consists with L_1, Q_1 and D_5 on the Fig. 3.1 is named PFC Circuit 1, and a circuit consists with L_2, Q_2 and D_6 on the Fig. 3.1 is named PFC Circuit 2. Since each phase is switched by shifting the phase by 180 degrees, the frequency of the synthesized inductor current is apparently double the frequency of the switching element.

Fig. 3.1 shows the current paths when the input AC voltage is positive (Fig. 3.1 (a) and (b)), and the current paths when it is negative (Fig. 3.1 (c) and (d)). The input current is always the sum of the currents of the two L_1, L_2, and the input ripple current is reduced because the phase is shifted by 180 degrees. The interleaving method enables loss to be dispersed into two elements, facilitating thermal design.

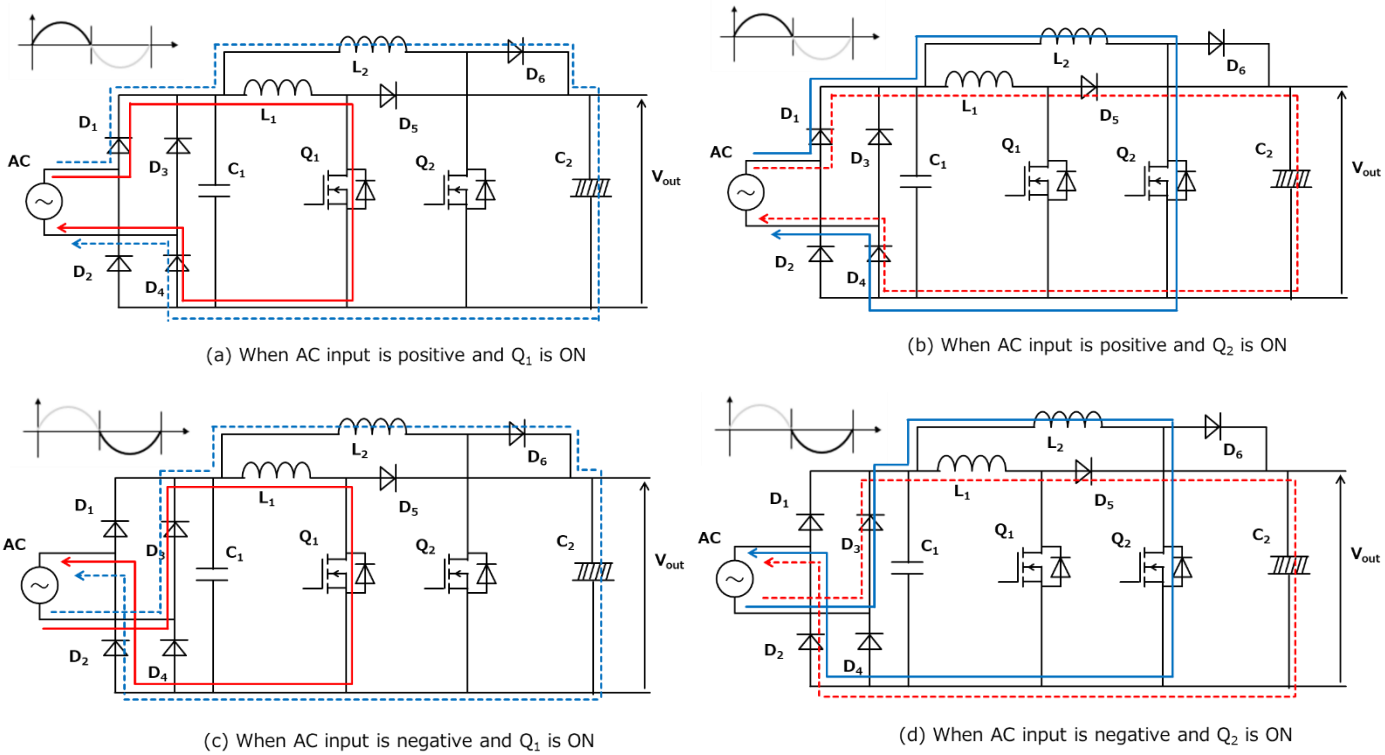
The following describes the operation of the interleaved PFC circuit. For simplicity, consider the case where the on-duty of each phase is less than 50% (when the switching element of one phase is on, and the switching element of the other phase is off).

During Positive AC Input

The PFC Circuit 1 stores energy on L_1 when Q_1 is on (and Q2 is off). At this time, the PFC circuit 2 draws current from the energy stored in L_2 (Fig. 3.1 (a)). And PFC circuit 2 stores energy in L_2 when Q_2 is on (Q_1 is off). At this time, the PFC circuit 1 draws current from the energy stored in L_1 (Fig. 3.1 (b)).

During Negative AC Input

The operation after rectification of AC input is the same as the operation during positive AC input. Fig. 3.1 (c) shows the operation when Q_1 is on (Q_2 is off), and Fig. 3.1 (d) shows the operation of when Q_2 is on (and Q_1 is off).



(a) When AC input is positive and Q_1 is ON

(b) When AC input is positive and Q_2 is ON

(c) When AC input is negative and Q_1 is ON

(d) When AC input is negative and Q_2 is ON

Fig. 3.1 Interleaved PFC Circuit Operation

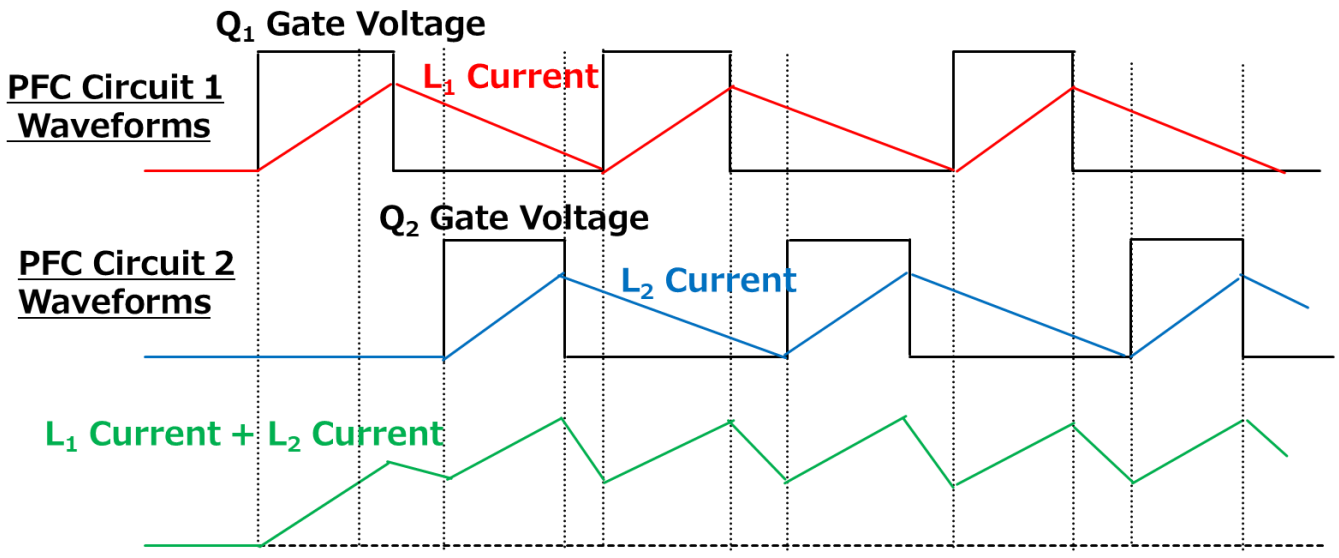


Fig. 3.2 Interleaved PFC Current Waveforms

3.2. 3-Phase LLC Resonant DC-DC Converter Circuit

Fig. 3.3 shows the configuration of the 3-phase LLC resonant DC-DC converter used in this design. Three half-bridge LLC converters are arranged in parallel on the primary-side, and the secondary-side terminals of the transformer are connected in Y configuration. By adopting this configuration, a 1U sized system using a general-purpose transformer achieves 1.6kW power.

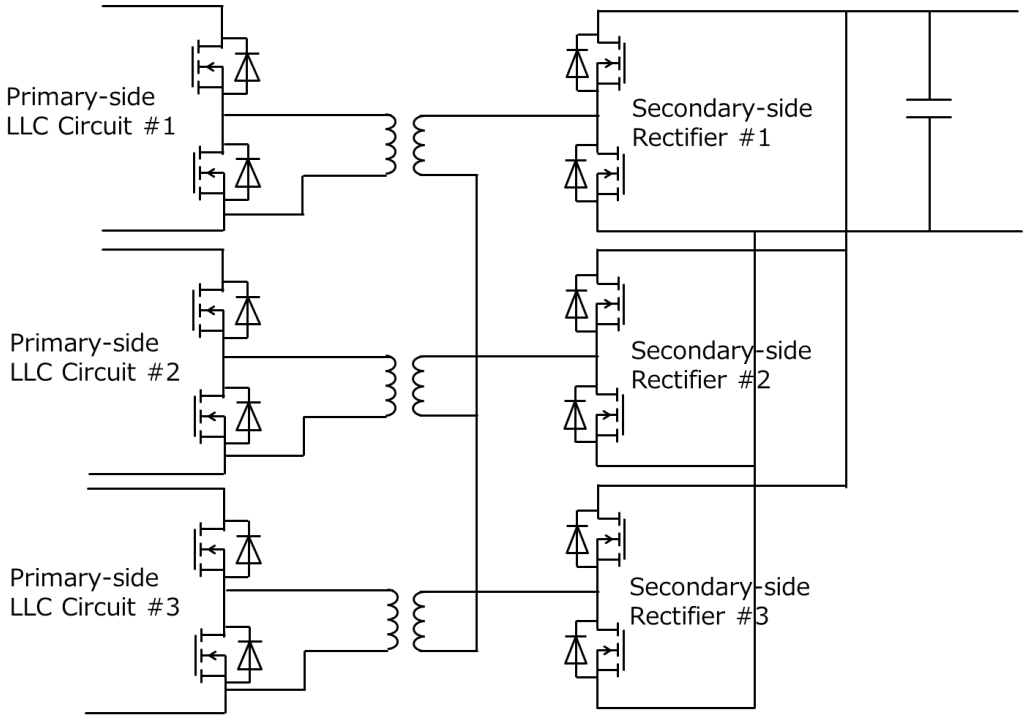
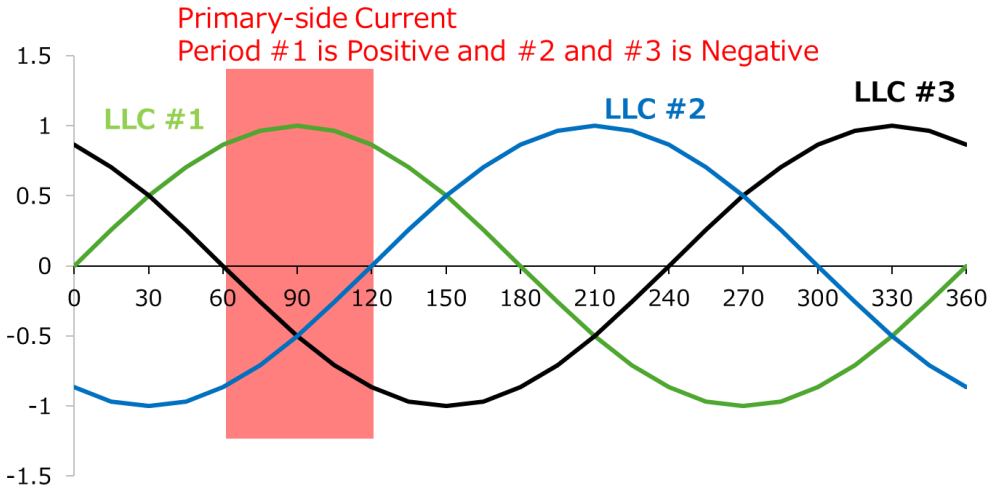


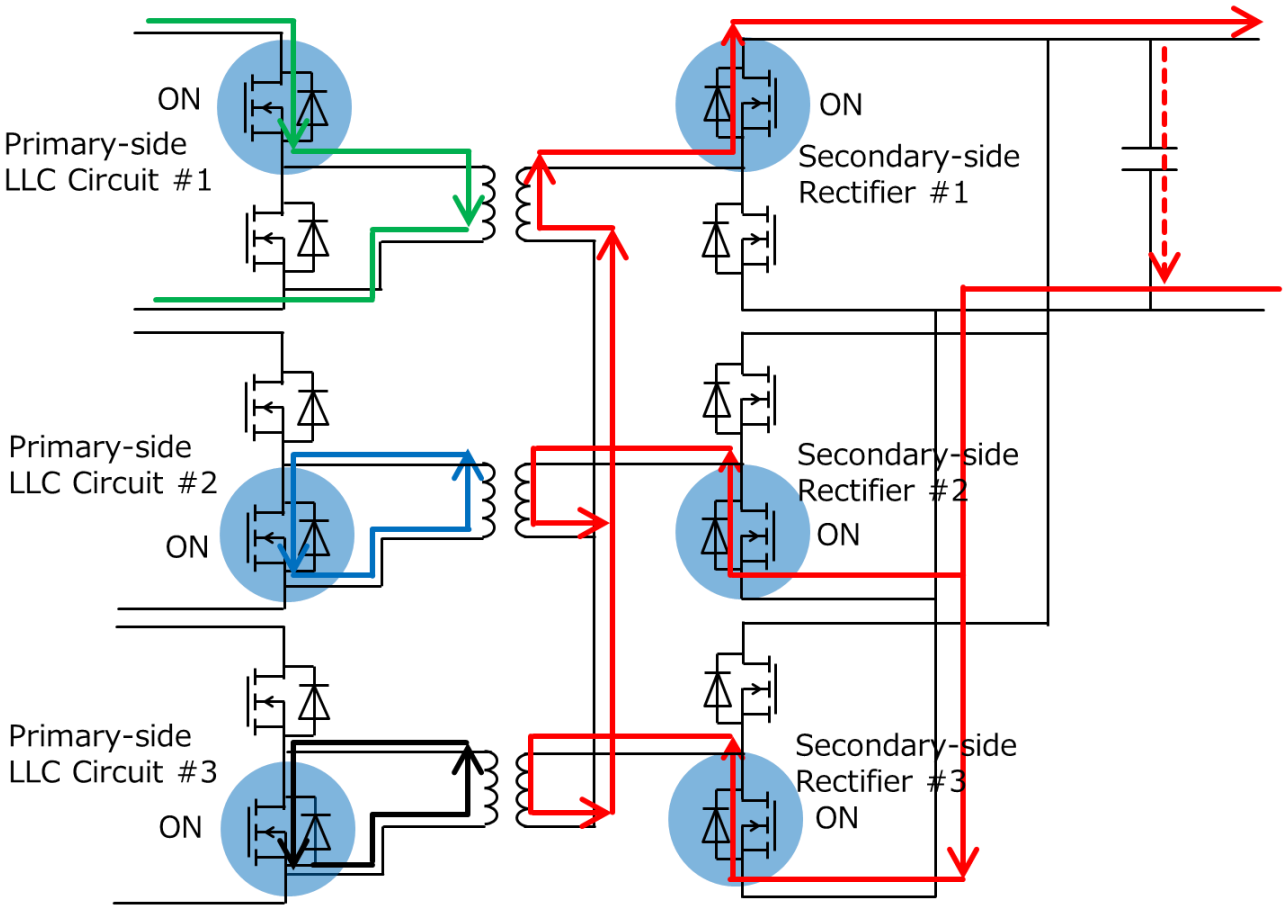
Fig. 3.3 3-phase LLC Resonant DC-DC Converter

This section outlines the operation of the 3-phase LLC resonant DC-DC converter. Each phase operates at a phase difference of 120 degrees, and the current on the primary-side of the transformer has a waveform equivalent to 3-phase AC. Fig. 3.4 (a) shows an image of the transformer's primary-side current. The actual current waveform is not a sine wave, but it will be described with an image of 3-phase AC. The positive and negative currents shown here indicate the direction of the current flowing in the transformer's primary-side (the direction in which the primary-side high-side MOSFET turns on and the current flows from the top to the bottom of the primary-side transformer winding is assumed to be positive). Fig. 3.4 (b) shows the current paths of secondary-side rectifiers #1, #2, and #3 when LLC circuit #1 is positive and circuits #2 and #3 are negative, as shown in Fig. 3.4 (a). The primary-side and secondary-side high-side/low-side MOSFETs are switched on and off in conjunction, while the secondary-side rectifier circuits #1, #2, and #3 operate in conjunction with one another.

The output voltage is twice the voltage between the transformer secondary windings. The voltage applied to the secondary-side MOSFETs is 1/2 of the output voltage, and devices with lower withstand voltage than typical LLC resonant DC-DC converters can be used.



(a) Image of Transformer's Primary-Side Current



(b) Current Path in Secondary-Side Rectifiers

Fig. 3.4 Operation of 3-phase LLC Resonant DC-DC Converter

4. 1.6kW LLC Resonant AC-DC Converter for Servers for Servers

This chapter provides an overview of the configuration of this design and the circuit design of each part. Fig. 4.1 shows the functional configuration diagram of this design, and Fig. 4.2 shows the circuit block diagram.

DC 390V is generated from the AC power supplies of 100V and 200V systems through an active-bridge circuit that uses MOSFET and an interleaved PFC circuit in a two-phase configuration. And this DC 390V is converted into DC 54.5V using a 3-phase LLC resonant DC-DC converter which is then outputs it via an ORing circuit. The 3-phase LLC resonant DC-DC converter is controlled using a conventional single-phase LLC controller, and its output is used by a MCU to generate MOSFET drive signals that differ in phase by 120 degrees.

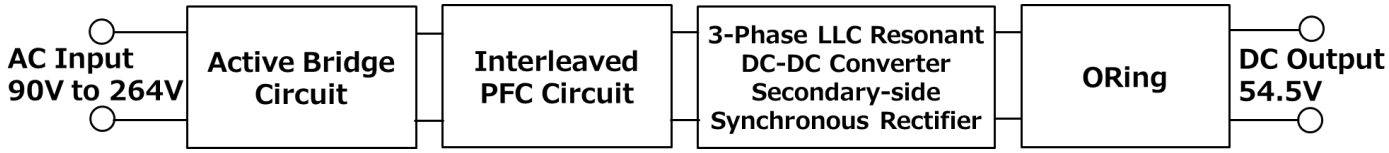


Fig. 4.1 Functional Configuration Diagram

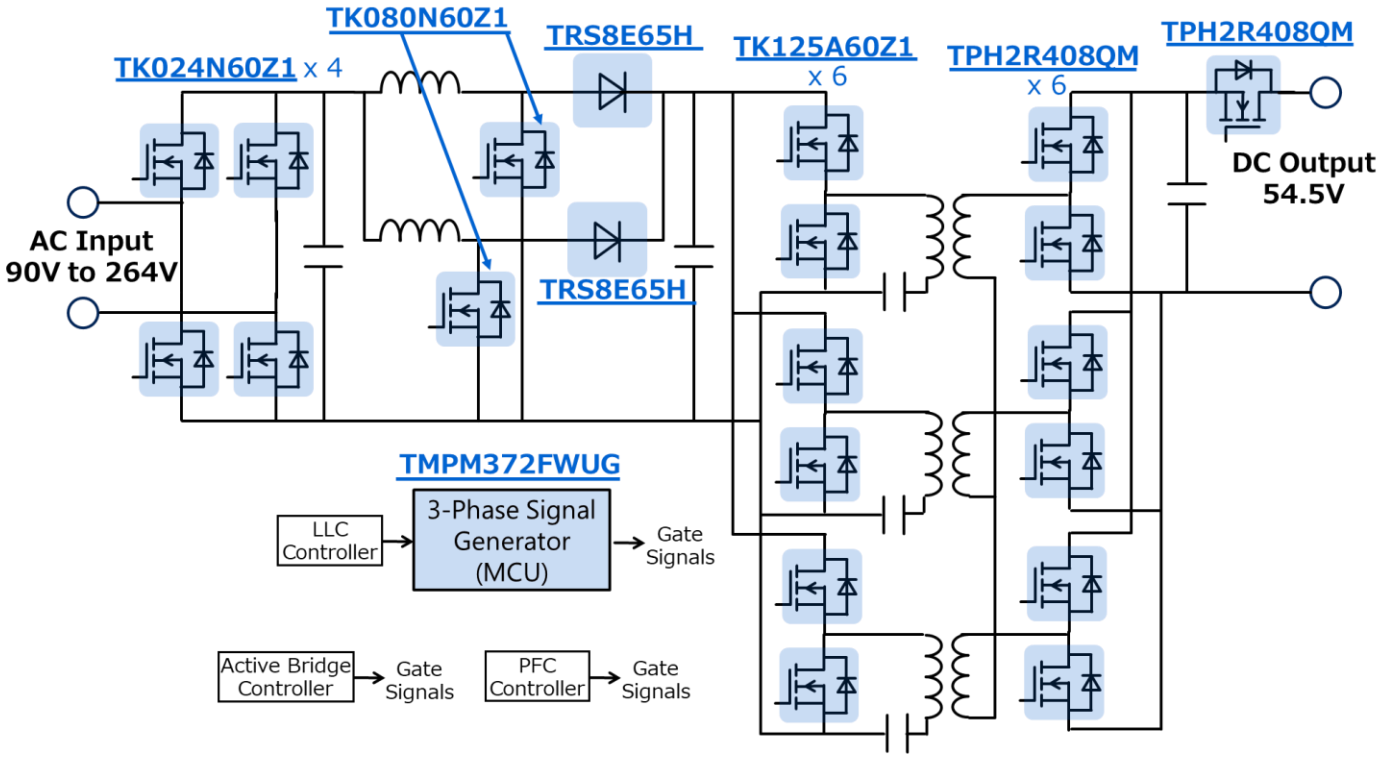


Fig. 4.2 Circuit Block Diagram

4.1. Specifications

Table 4.1 lists the main specifications of this design.

Table 4.1 Specifications of This Design

Item	Conditions	Min.	Typ.	Max.	Unit
Input characteristics					
AC input voltage (rms)		90		264	V
AC input current (rms)	Vin = AC 90V, Iout = 20A			12	A
Input frequency		47		63	Hz
Internal characteristics (Interleaved PFC circuit)					
Output voltage			390		V
Maximum output power	Vin = AC 230V			1.77	kW
	Vin = AC 115V			0.89	kW
Switching frequency			62.5		kHz
Output characteristics (3-phase LLC resonant DC-DC converter circuit)					
Output voltage		51.7	54.5	57.3	V
Output current	Vin = AC 230V			29.4	A
	Vin = AC 115V			14.7	A
Maximum output power	Vin = AC 230V			1.6	kW
	Vin = AC 115V			0.8	kW
Output ripple voltage	Ta = 25℃			2180	mV
Other					
Protective functions	Output overvoltage protection, output overcurrent protection, output short-circuit protection, and overheat protection				
Board layer configuration	Main board: FR-4 4-layer structure, copper foil thickness 70μm (all layers) Active bridge circuit board: FR-4 2-layer configuration, copper foil thickness 70μm PFC control board, LLC control board: FR-4 2-layer configuration, copper foil thickness 35μm				

4.2. AC Line Circuit

This section describes the design of AC line-circuits. Fig. 4.3 shows AC line-circuit.

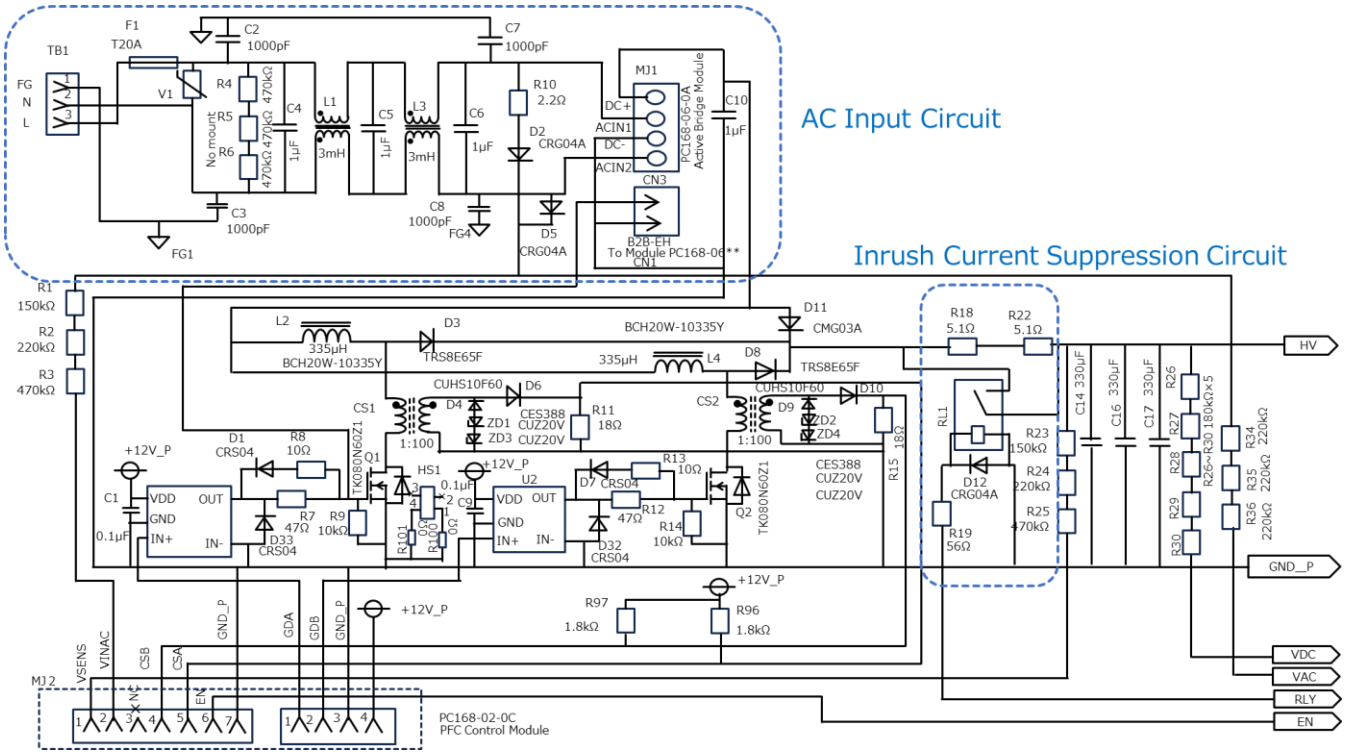


Fig. 4.3 AC Line Circuit

Fuse

To cut-off AC line when excessive current flows through AC line, the fuse F1 is installed. Select a fuse using the max. value of the rms current value of AC line $ACin_{peakrms}$. The maximum power Pout, total power supply efficiency η, the power factor PF, and the minimum value of the rms value of AC line voltage $VinAC_{min}$ are used to calculate the maximum value of the rms current value of AC line $ACin_{peakrms}$ using the following equation.

$$ACin_{peakrms} = \frac{Pout}{\eta \times PF \times VinAC_{min}}$$

If $VinAC_{min}$ = 90V, Pout = 800W, η = 90%, and PF = 99%, then $ACin_{peakrms}$ = 10A.
In this design, 20A fuse is selected considering the margins.

When selecting a fuse, in addition to the above max. current, the inrush current which flows when AC power supply is turned on, and whether the product has acquired the safety standard to be complied with, etc. must also be considered.

Varistor

A metal-oxide varistor (V1) is used for protection from the surge-voltage that might appears on the AC line because of inductive lightning. A varistor is selected based on the AC line voltage. Since the maximum AC line voltage of this design is 264V in rms value and 373V in peak value, a varistor with the maximum allowable circuit voltage of 420V (AC rms value) and the varistor voltage of 680V is selected considering the margins.

When selecting a varistor, it is necessary to consider not only the maximum allowable circuit voltage and varistor voltage, but also the surge current tolerance, energy tolerance, etc. In addition, since the varistor failure mode has many short modes, a fuse is inserted before the varistor (on the AC input side).

EMI suppression components

The Y capacitors (C2, C3, C7, C8) and the common mode chokes (L1, L3) are installed to suppress common mode noise, and the X capacitors (C4, C5, C6) are installed to suppress differential noise. Since the noise-levels are affected by PCB layout/enclosure construction, thus these components must be changed, removed, or added according to the requirement. Note that this design does not have an adequate Y capacitor because there is no enclosure. When designing a system with a chassis, install a sufficient Y capacitor as a countermeasure against common mode noise. Increasing the capacitance of the Y capacitor will increase the leakage current, so it is necessary to check whether the system satisfies the required safety standards.

Inrush current suppression component

The fuse resistors (R18, R22) and the relay (RL1) are installed to suppress inrush current when AC power is turned on. When AC power is turned on, RL1 opens and AC current flows to R18, R22, suppressing the inrush current. After AC power supply is turned on, RL1 closes when the specified conditions are met. When RL1 conducts, R18, R22 that was suppressing AC current are short-circuited, reducing power dissipation during operation. It is necessary to select a fuse resistor that can withstand the inrush current. Also, confirm that the conditions and timing for opening and closing the relay satisfy the required specifications.

4.3. Active Bridge Circuit

For full-wave rectification before PFC circuit, an active-bridge circuit using four power MOSFETs TK024N60Z1 was adopted to improve the power supply efficiency. Fig. 4.4 shows the active bridge circuit.

MOSFETs are controlled by the TEA2209T (made by NXP, hereinafter referred to as the active bridge controller). For more information about the Active Bridge Controller, refer to TEA2209T datasheet and related documentation. The active bridge controller senses the polarity of AC power supply between terminals L and R and turns on/off the diagonal-pair MOSFETs according to the polarity.

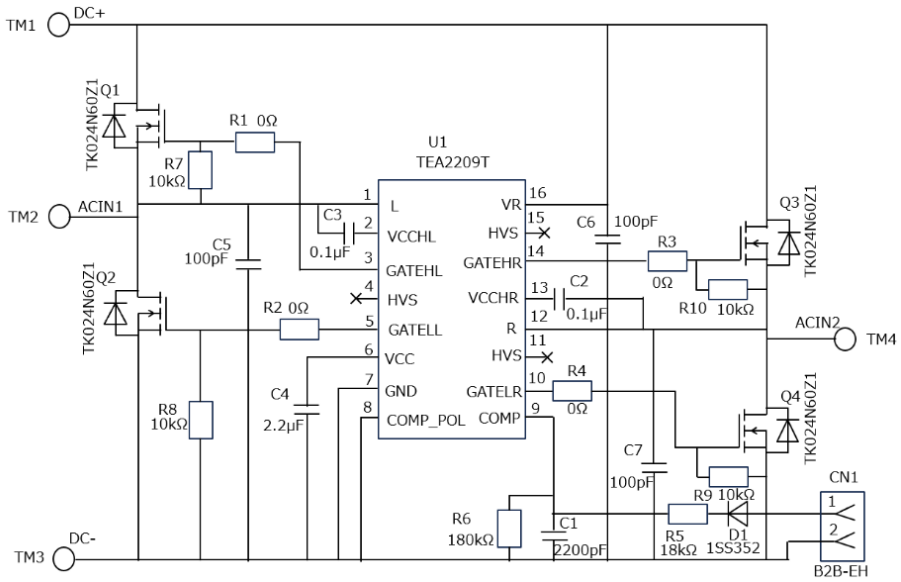


Fig. 4.4 Active Bridge Circuit

X capacitor discharge

The discharging resistors Rdis (R4, R5, R6) of the X capacitors Cx (C4, C5, C6) shown in Fig. 4.3 are not mounted. Discharging of the X capacitors Cx is performed by the active bridge controller mentioned above. When the mains voltage is disconnected from the power supply, the capacitor C_{VCC} (C4 in Fig. 4.3) that has been charged to V_{reg}, is discharged with an internal biased current I_{bias} (23μA). When VCC pin drops below V_{dis} (disable voltage 9.7V), the X capacitor starts discharging at 2mA current. The following table shows t_d waiting time before the X capacitor starts discharging.

$$t_d = \frac{C_{VCC}(V_{reg} - V_{dis})}{23\ \mu A} = 0.11E6 \times C_{VCC}$$

Since C_{VCC} in this design uses the default value of 2.2μF, td is approximately 0.24 seconds.

4.4. Interleaved PFC Circuit

In this design, interleaved PFC circuit is configured using UCC28070 (made by Texas Instruments, hereinafter referred to as PFC controller). The basic design items are described below. Refer to UCC28070 datasheet and related documentation for detailed description of design around PFC controller.

Fig. 4.5 shows the interleaved PFC circuit on the mainboard and Fig. 4.6 shows PFC controller peripherals on the PFC control board.

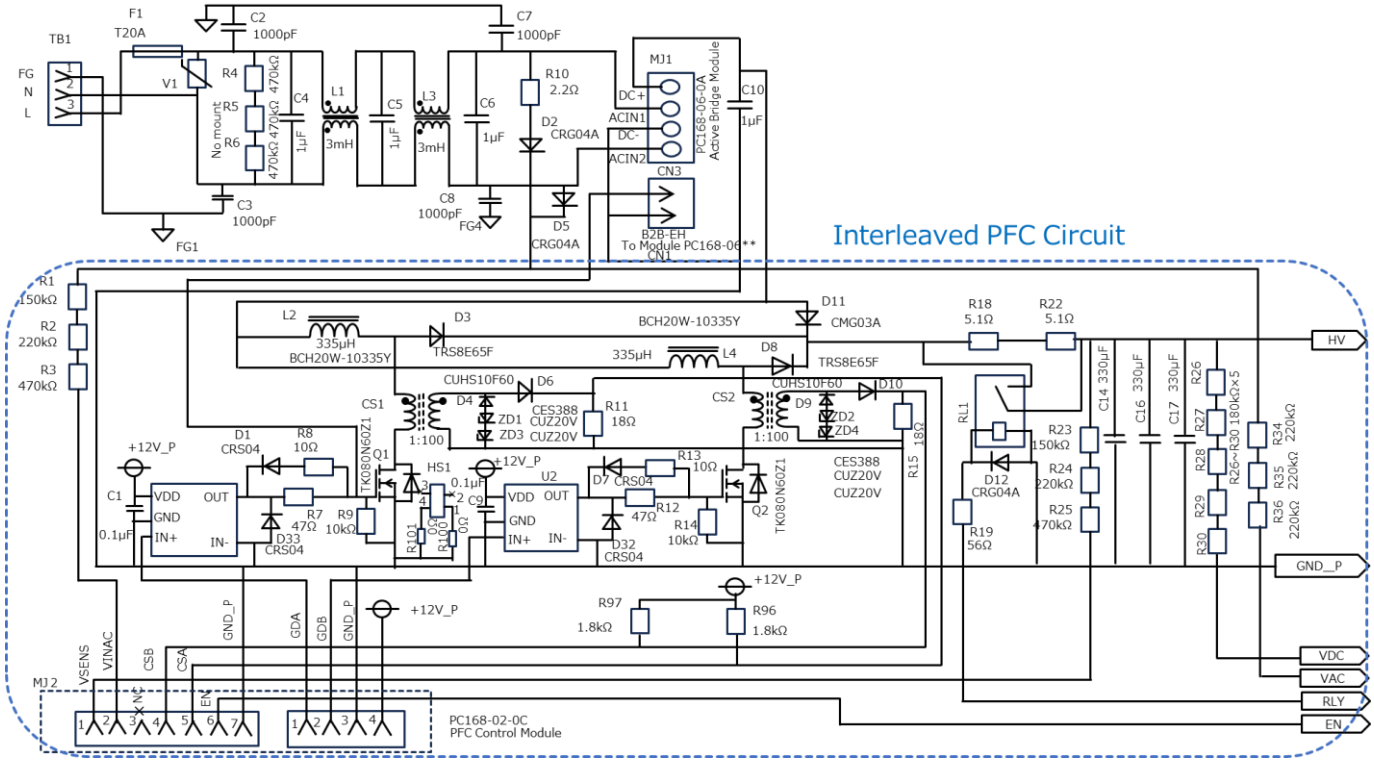


Fig. 4.5 Interleaved PFC Circuit

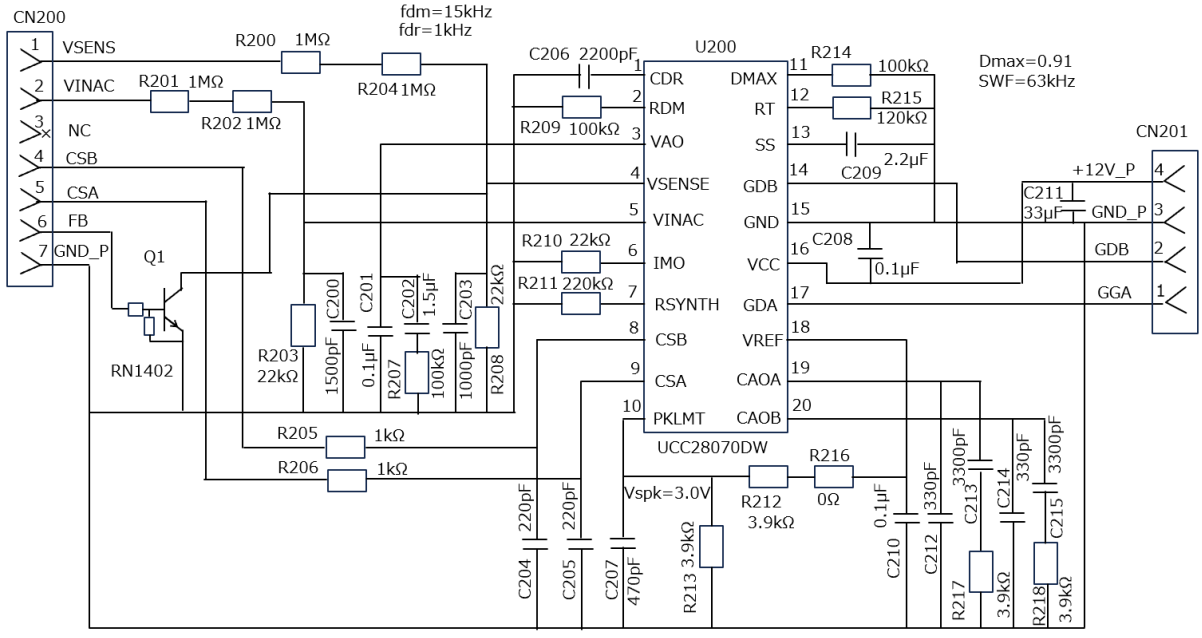


Fig. 4.6 PFC Controller Peripheral Circuit

Output voltage setting

The output voltage setting circuit is shown in Fig. 4.7. Set the output-voltage (Vout_PFC) with the resistors (R23, R24, R25, R200, R204, R208) located on the main board and PFC control board. PFC control ensures that the output-sense-voltage (V_{VSENSE}) divided by these resistors matches VSENSE voltage (3V) of the PFC controller. The output voltage (Vout_PFC) at Ta = 25 °C is calculated using the following equation by using the bias current Ibias_PFC (250nA).

$$Vout\_PFC = \frac{VSENSE\ voltage \times (R23+R24+R25+R200+R204+R208)}{R208} + Ibias\_PFC \times (R23+R24+R25+R200+R204)$$

In this design, 840kΩ is used for total resistance of R23 to R25, 1MΩ for R200, 1MΩ for R204, and 22kΩ for R208, and therefore Vout_PFC is set as 390V. The above resistance can be changed as necessary to set the desired output voltage.

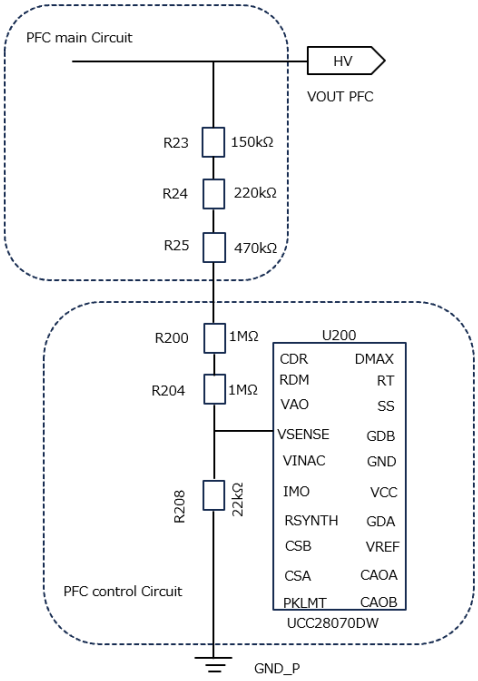


Fig. 4.7 Output Voltage Setting Circuit

Switching frequency, maximum duty setting

The switching frequency and the max duty of PWM are set by RT pin and the resistor connected to DMAX pin shown in Fig. 4.8. RT Resistor R_{RT} (R215) sets PWM Frequency (f_{PWM}) and is calculated by the following equation:

$$R_{RT}(k\Omega) = \frac{7500}{f_{PWM}(kHz)}$$

$$f_{PWM}(kHz) = \frac{7500}{R_{RT}(k\Omega)}$$

This design uses 120kΩ for R215 and sets f_{PWM} = 62.5kHz.

The max. duty D_{MAX} of PWM is calculated from R_{RT} and D_{MAX} resistor R_{DMX} (R214) by the following equation.

$$R_{DMX} = R_{RT} \times (2 \times D_{MAX} - 1)$$

This design uses 100kΩ for R214 and therefore sets D_{MAX} = 0.916.

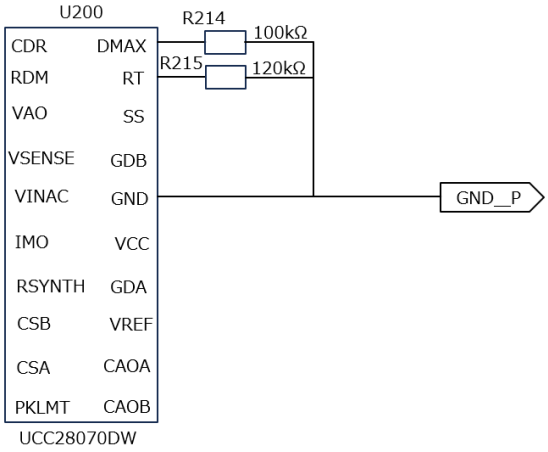


Fig. 4.8 Switching Frequency and Maximum Duty Setting Circuit

Gate drive circuit

Fig. 4.9 shows the gate drive circuit. The gate-driver design affect power-efficiency and EMI (noises). Generally, there is a trade-off between power supply efficiency and EMI, and both need to be well balanced. To adjust EMI, adjust the resistance of the gate-series resistor (R7, R8). The turn-on speed of MOSFET is determined by R7. During turn on, R8 will not have any effect because of D1. And the turn-off speed is determined by the parallel resistances of R7 and R8. If only turn-on speed needs to be changed, both R7 and R8 must be adjusted. If only turn-off speed needs to be changed, and if it is possible to adjust it only using R8, then the turn-on speed will not be affected. Increasing the gate-resistance may reduce the switching speed of MOSFET, which may also reduce the power-supply efficiency. Check that the power supply efficiency specification and heat radiation specification satisfy the required specification.

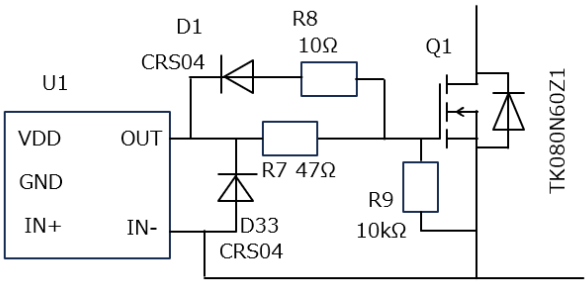


Fig. 4.9 Gate Drive Circuit

Inductor

In the interleaved PFC circuit shown in Fig. 4.5, the inductance value L of the inductor L2 is set using the following items in the input 100V system. The same applies to the inductor L4.

1. Maximum output power (Pout): 800W
2. Min. input AC rms ($VinAC_{min}$): 90V
3. Total power conversion efficiency of this design: 90%
4. Power factor (PF) of this design: 99%
5. PFC output-voltage (Vout_PFC): 390V
6. Switching frequency (f_{PWM}): 63kHz

The peak input current $ACin_{peak}$ of the input AC is calculated by the following equation.

$$ACin_{peak} = \frac{Pout \times \sqrt{2}}{\eta \times PF \times VinAC_{min}}$$

$$= \frac{800 \times \sqrt{2}}{0.9 \times 0.99 \times 90} = 14.11$$

Assuming that ΔIL is the allowable current ripple of the inductor in each phase, L is calculated as follows:

$$L = \frac{\sqrt{2} \times VinAC_{min} - \frac{2 \times VinAC_{min}{}^2}{Vout\_PFC}}{f_{PWM} \times \Delta IL}$$

Here, if the ΔIL is 60% of the peak current i.e. 7.06A, then L is calculated to be 193μH from the above equation. A 335μH inductor is selected for this design.

In addition, the peak current IL_{peak} flowing through the inductor is calculated using AC line peak input current $ACin_{peak}$ as follows.

$$IL_{peak} = \frac{ACin_{peak}}{2} + \frac{\Delta I}{2}$$

Since $ACin_{peak}$ = 14.11A and ΔI = 4.01A, IL_{peak} becomes 9.06A. Therefore, a 10A rated inductor is selected in this design.

Output capacitors

Fig. 4.10 shows the position of the output capacitor. The output capacitance Cout_PFC (C14, C16, C17) is calculated based on holdup time requirements.

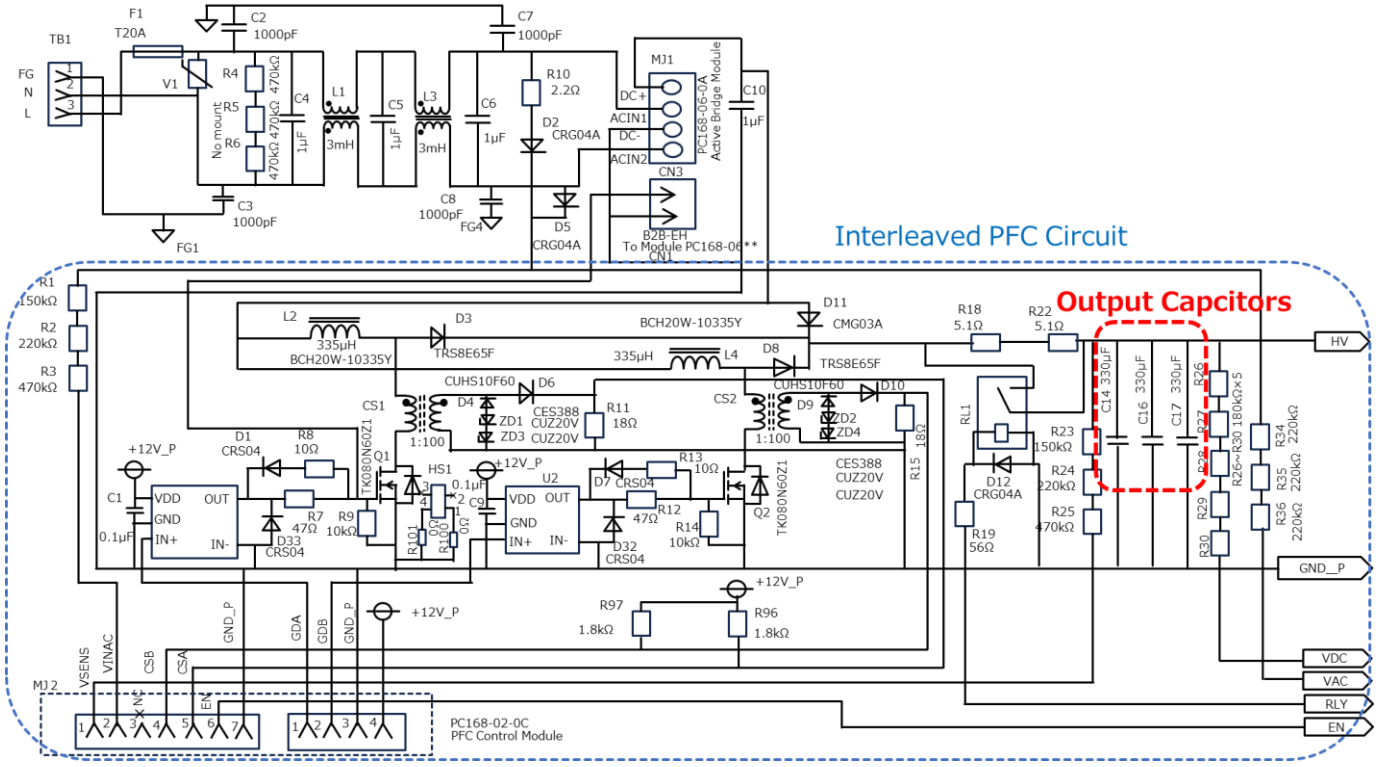


Fig. 4.10 Output Capacitors

The hold-up time Thold is calculated using Cout_PFC, output voltage Vout_PFC, output lower limit voltage Vout_PFC_min, maximum output power Pout_max, and LLC power supply efficiency η2 using the following equation.

$$Thold = Cout\_PFC \times \frac{(Vout\_PFC^2 - Vout\_PFC\_hold^2) \times \eta 2}{2 \times Pout\_max}$$

When Vout_PFC = 390V, Vout_PFC_min = 300V, η2 = 94%, Pout_max = 1600W, and Thold is 10ms which is the half cycle of AC 50Hz, the Cout_PFC becomes 549μF. In this design, three 330μF capacitors are arranged in parallel to make 990μF.

In addition, if there is the required specification for the output ripple, set it by the following method.

1. Find the capacitance value of the output capacitor (Cout_PFC) that satisfies the output ripple specification.
2. Find the capacitance value of the output capacitor (Cout_PFC) that satisfies the hold-up time.
3. The capacitance values of both are compared and a large value is used.

When selecting an output capacitor (Cout_PFC), consider the tolerance and aging.

4.5. 3-Phase LLC resonant DC-DC Converter Circuit Design

Fig. 4.11 shows the schematic of the 3-phase LLC resonant DC-DC converter section of this design. In this 3-phase configuration, each phase operates with a phase difference of 120 degrees.

This design uses a NCP1397 (made by onsemi, hereinafter referred to as LLC controller) to control the power supply. Control signals generated by LLC controller are fed to MCU TMPM372FWUG through a level shifter. MCU generates the control signals (MOSFET drive signals) with the phase differential of 120 degrees and outputs to the gate driver of each phase. Fig. 4.12 shows the circuit diagram of 3-phase LLC resonant DC-DC converter circuit.

The following describes the basic designs of the 3-phase LLC resonant DC-DC converter. For detailed designs around LLC controller, refer to NCP1397 datasheet and related documentation.

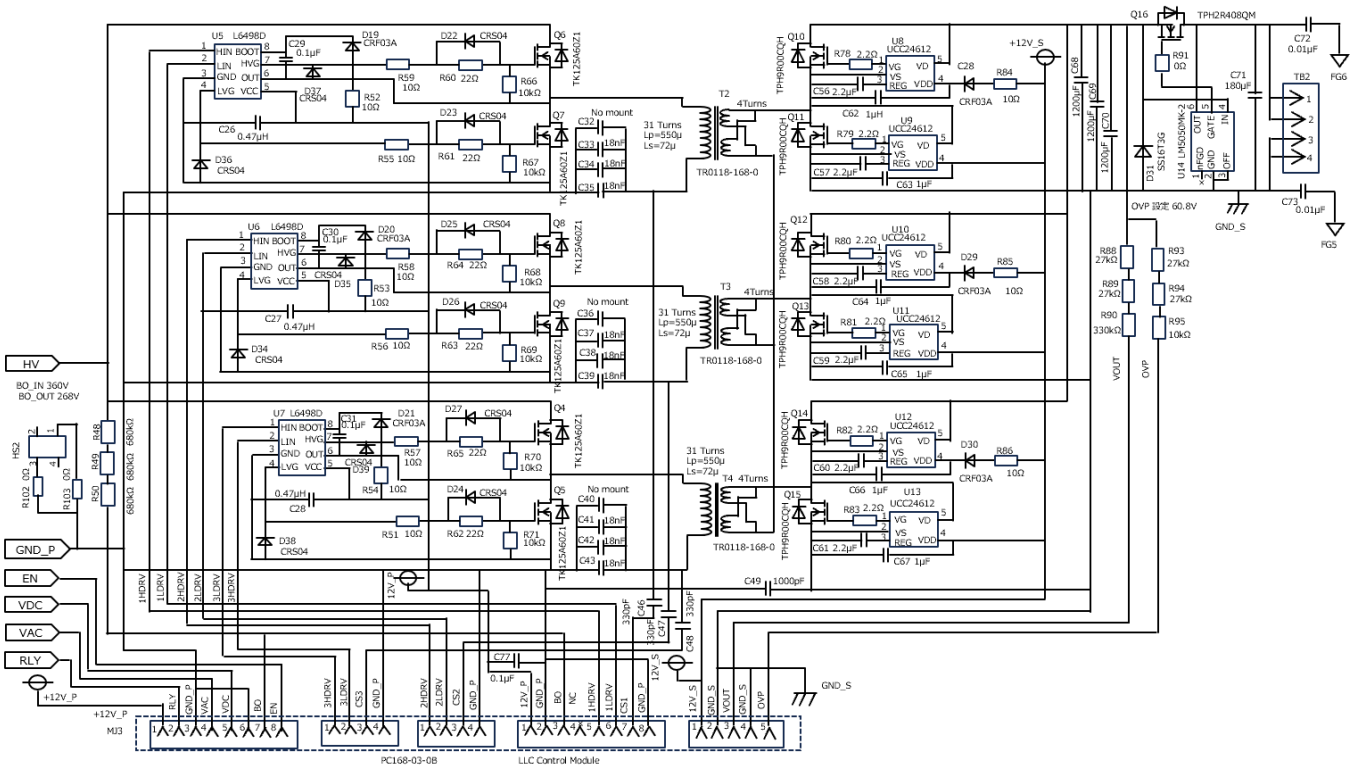


Fig. 4.11 3-Phase LLC resonant DC-DC Converter Circuit

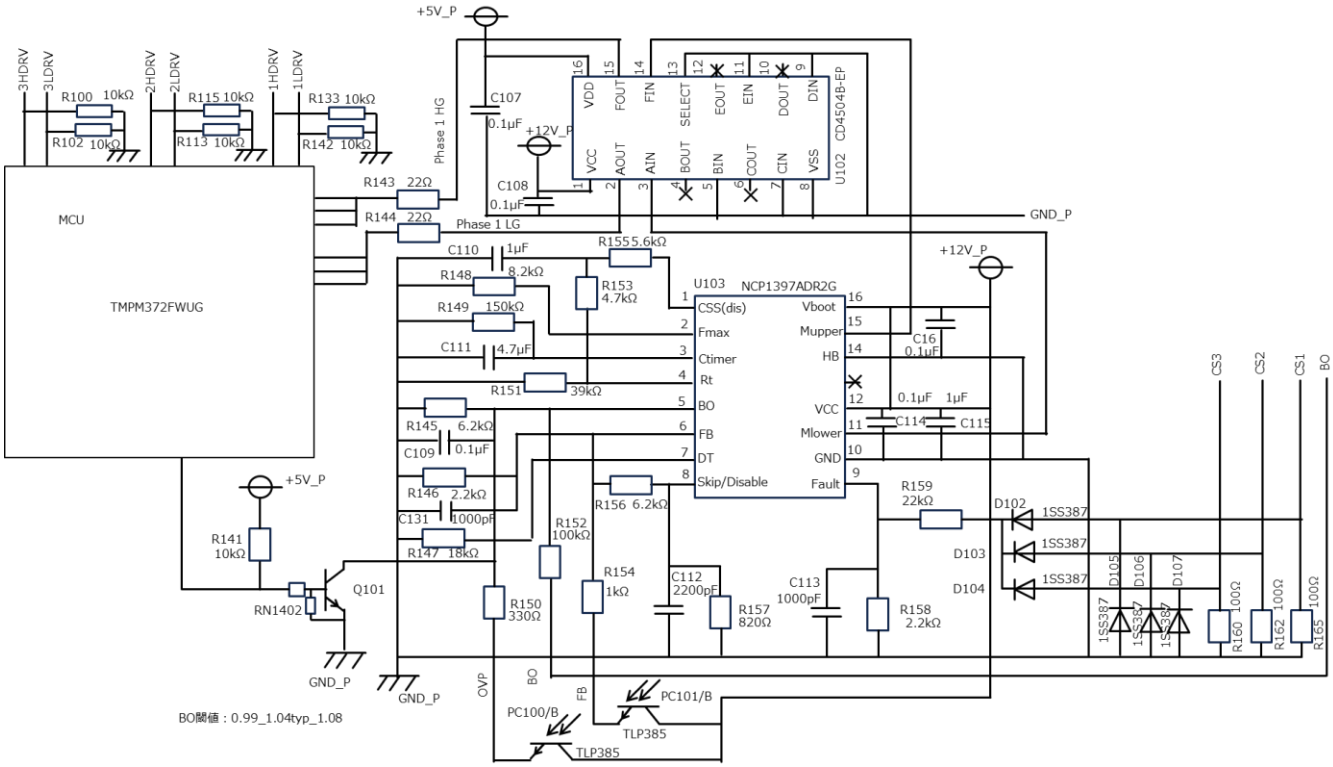


Fig. 4.12 3-Phase LLC resonant DC-DC Converter Control Circuit

Input voltage drop protection circuit

Input voltage drop protection function protects the DC-DC converter when the input voltage of DC-DC converter section is low. LLC controller will deactivate the output-pulse when the input-voltage is lower than the pre-set level. LLC controller controls the operation using the voltage generated by the input voltage divided made up of resistors R_{upper} and R_{lower}. This voltage is input to the BO pin.

Fig. 4.13 shows the resistor divider used for this function. In this design, the protection voltage is set to 360V and the hysteresis when the input voltage drops is set to 60V, and therefore R_{upper} = 2.21MΩ, R_{lower} = 6.2kΩ are selected.

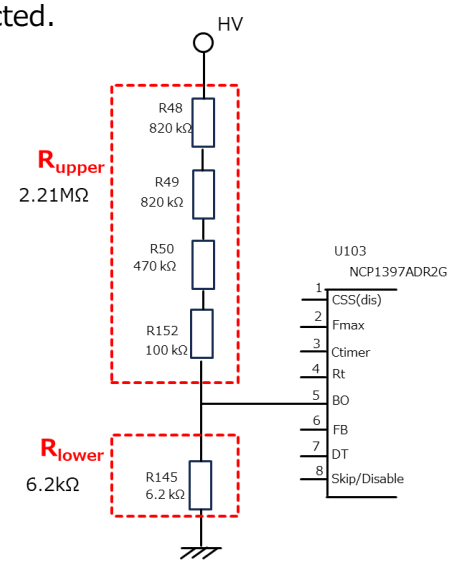


Fig. 4.13 Input Voltage Drop Protection Setting Circuit

Output voltage setting

Fig. 4.14 shows the output voltage setting circuit. The output-voltage Vout_LLC of this design is set using the external resistors (R88, R89, R90, R167 and R166) and the shunt regulator (U104). The shunt regulator controls the photocoupler (PC101) current so that the voltage obtained by dividing Vout_LLC by the resistor above matches the reference voltage Vref_LLC (2.5V). LLC controller operates to keep Vout_LLC constant according to the amount of current fed back from PC101 to FB terminals.

If the bias current to the shunt regulator's REF pin voltage is Ibias_LLC (30nA), Vout_LLC is calculated using the following equation.

$$Vout\_LLC = \frac{Vref\_LLC \times (R88 + R89 + R90 + R167 + R166)}{R166} + Ibias\_LLC \times (R88 + R89 + R90 + R166)$$

In this design, Vout_LLC is set as 54.6V considering voltage drop of output circuit then R88 = 27kΩ, R89 = 27kΩ, R90 = 330Ω, R167 = 330Ω, R166 = 3. 9kΩ are selected.

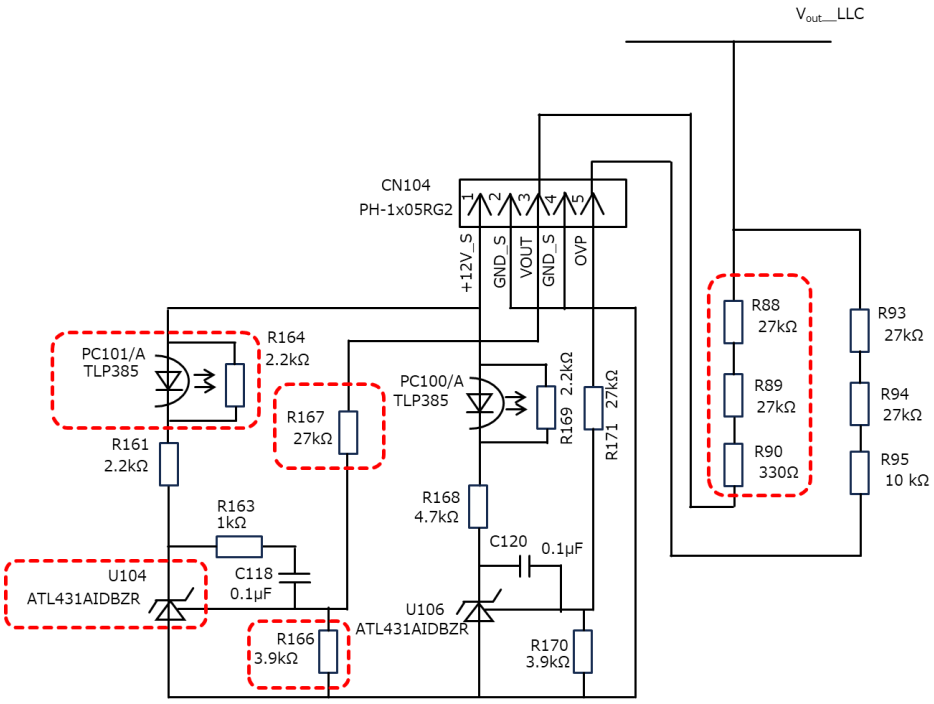


Fig. 4.14 Output Voltage Setting Circuit

Overvoltage protection

Fig. 4.15 shows the overvoltage protection setting circuit. The overvoltage protection voltage Vovp_LLC is set with the external resistors (R93, R94, R95, R171 and R170) and the shunt regulator (U106).

The following equation is used to calculate Vovp_LLC, where Ibias_LLC (30nA) is the bias current to the shunt regulator REF pin voltage.

$$Vovp\_LLC = \frac{Vref\_LLC \times (R93 + R94 + R95 + R171 + R170)}{R170} + Ibias\_LLC \times (R93 + R94 + R95 + R171)$$

In this design, R93 = 27kΩ, R94 = 27kΩ, R95 = 10kΩ, R171 = 27kΩ, R170 = 3.9kΩ are selected, to set Vovp_LLC = 64V.

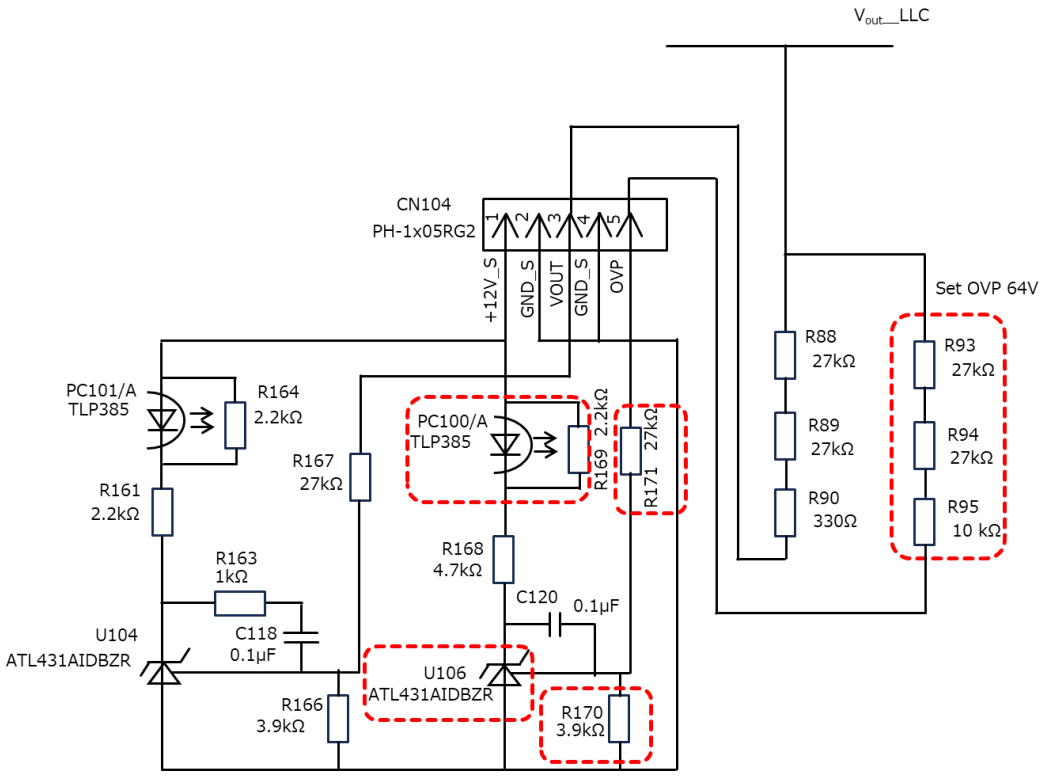


Fig. 4.15 Overvoltage Protection Setting Circuit

Soft start

The soft-start function is required to prevent a large current from flowing during startup. Soft-start capacitor CSS (C110) connected to the Soft-start discharge pin CSS(dis) of LLC controller to set the soft-start duration. When the controller starts to operate, the soft-start capacitor CSS is completely discharged, and its charging starts from Rt pin. Soft-start operation takes place until CSS is fully charged.

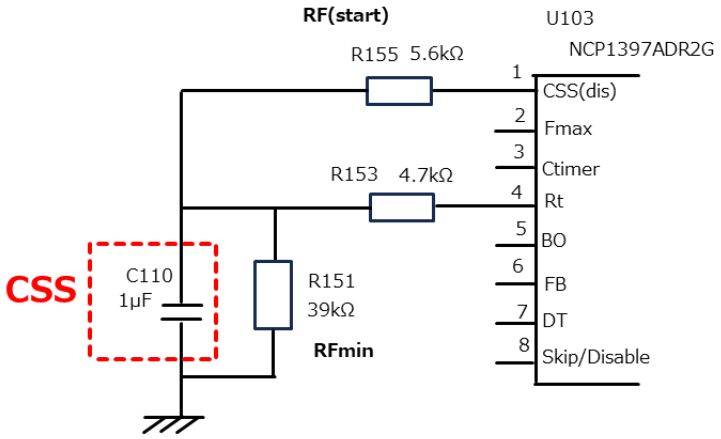


Fig. 4.16 Soft-Start Setting Circuit

Gate drive circuit

Fig. 4.17 shows the gate drive circuit. The gate-series resistors (R59, R60 and R55, R61) can be used to adjust the turn-on speed and turn-off speed of MOSFET independently.

First, the adjustments related to the high-side MOSFET (Q6) are described. The turn-on and turn-off speeds can be reduced at the same time by increasing R59. Only turn-on speed can be reduced by increasing R60. The adjustments for the low-side MOSFET (Q7) can be done in the same way using R55, R61.

Increasing the resistance may reduce the switching speed of MOSFET, which may also reduce the power supply efficiency. Check that the power supply efficiency specifications and heat radiation specifications satisfy the required specifications.

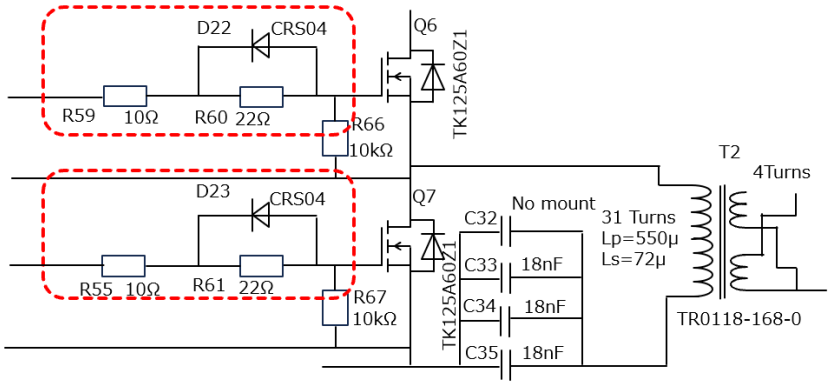


Fig. 4.17 Gate Drive Circuit

Frequency setting

LLC control is capable of switching-frequency operation from 50kHz to 500kHz. The minimum frequency is set using the resistor R_{Fmin} placed between Rt pin and GND, and the maximum frequency is set using the resistor R_{Fmax} placed between Fmax pin and GND.

In this design, R151 = 39kΩ is selected for R_{Fmin} and R148 = 8. 2kΩ is selected for R_{Fmax}, with the minimum frequency setting set to 50kHz and the maximum frequency set to 200kHz.

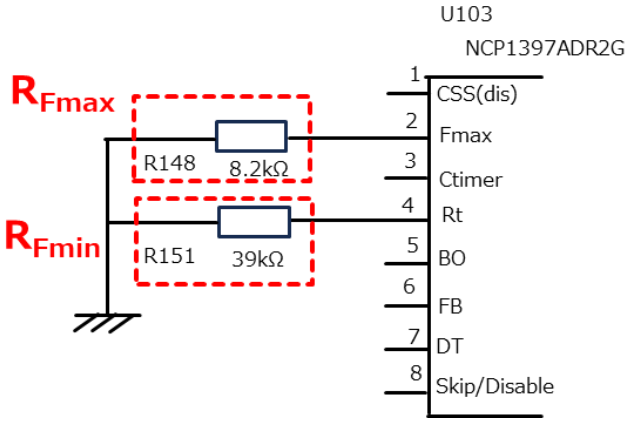


Fig. 4.18 Frequency Setting Circuit

Dead time setting

The dead time is set by the resistor R_{DT} connected between DT pin and GND. In this design, R_{DT} is selected as R147 = 18kΩ, and the deadtime is set to approximately 444ns.

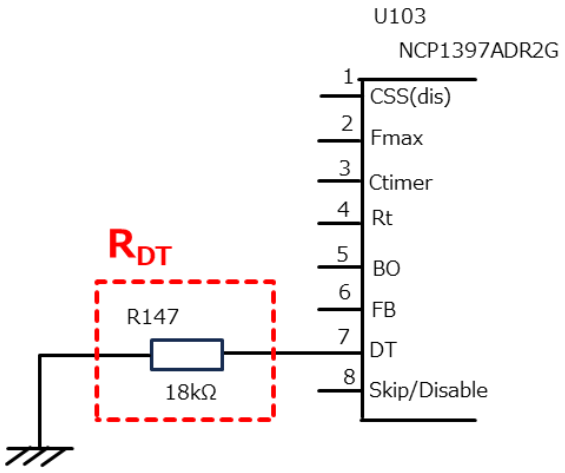


Fig. 4.19 Dead Time Setting Circuit

Output capacitors

Fig. 4.20 shows the output capacitor peripheral circuit. The output capacitor value C_{out} is set so that the output voltage ripple V_{ripple} meets the requirements. When V_{ripple} is 2180mV and the maximum output current is I_{max}, ESR required for the output capacitor is calculated by the following equation.

$$ESR = \frac{V_{ripple}}{\frac{2 \times \pi}{4} \times I_{max}}$$

Because I_{max} is 29.4A, ESR becomes 44.2mΩ.

In this design, three capacitors that capacitance is 1200μF and ESR is 20mΩ are placed in parallel (C68, C69, C70) with a combined ESR of approximately 7mΩ.

Following points must also be checked:

1. The output terminal undershoot/overshoot that occurs when the load changes suddenly is within the specified voltage range.
2. The allowable ripple current of the output capacitor must be secured.
3. Output capacitor tolerances and aging must be considered.

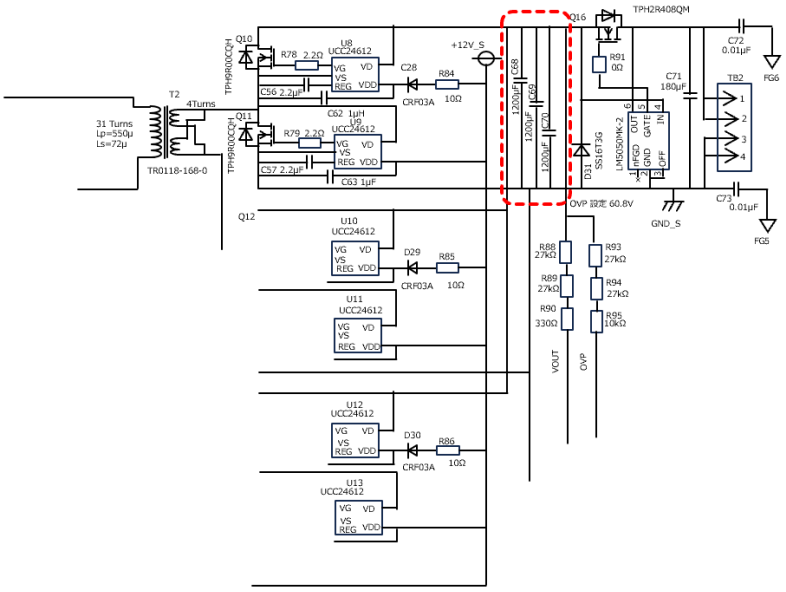


Fig. 4.20 Output Capacitors

4.6. 3-Phase LLC Resonant DC-DC Converter Design

This section describes the design of the 3-phase LLC resonant DC-DC converter section (resonant design, transformer design, etc.).

4.6.1. Calculation of Output Voltage and Output Power of Individual Transformers

Fig. 4.21 shows an outline of the 3-phase LLC resonant DC-DC converter section of this design. The primary side performs half-bridge switching with 120-degree phase shift, and the secondary side is a power supply configuration with Y-connection at the transformer end.

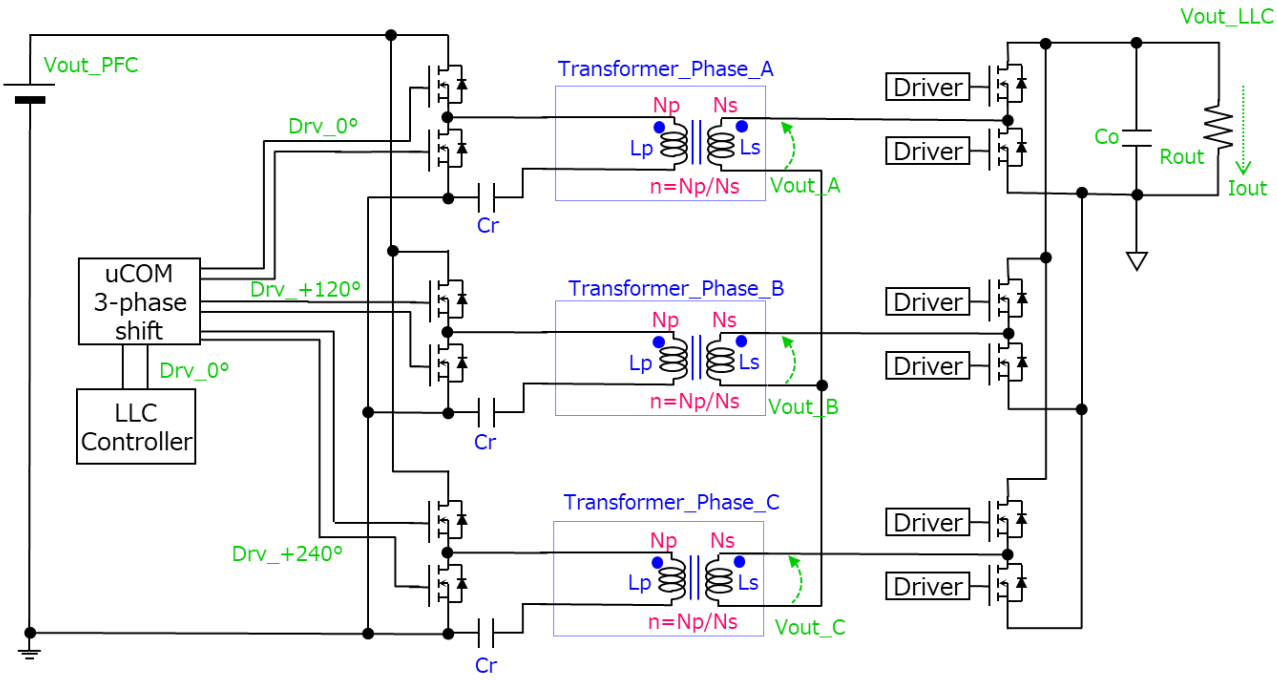


Fig. 4.21 3-Phase LLC resonant DC-DC Converter Circuit

Transformer designs are performed by the First Harmonic Approximation (FHA) method. Since the FHA is designed on the assumption that a single transformer is used for the resonant circuit, the output power and output voltage of the transformer alone in this design are calculated.

The specifications of this design are the output-voltage 54.5V and the max. output power 1600W. As described in 3.2, two-phase transformers are connected in series at all times in a 3-phase Y-connection, and 54.5V is output. Therefore, the secondary-side output of the transformer alone is half 27.25V of 54.5V. The maximum output power 1600W means that the maximum output current is 1600W/54.5V = 29.4A. Since 29.4A is divided into 3 phases, the mean output current of one transformer itself is 29.4A/3 = 9.79A.

From above explanation, for each transformer the output voltage is 27.25V and the output power is 266.67W (= 27.25 x 9.79). This information is used for proceeding with the resonant transformer design with FHA. For designing, Phase_A is used as an example (show in Fig. 4.21). Phase_B and Phase_C have similar design values.

4.6.2. Transformer Design (Resonant Design)

Turn ratio determination

The turn ratio n is calculated by the following equation using the output voltage Vout_PFC of PFC and the output voltage Vout_LLC of LLC (= 2 x Vout_A).

$$n = \frac{Vout\_PFC}{2 \times Vout\_A}$$

Assigning Vout_PFC = 390 V and Vout_A = 27.25V results in n = 7.16. In this design, n = 7.75 is selected.

Resonant circuit voltage gain determination

The FHA is used to develop design based on the gain between the inputs and outputs of the LLC circuit. The voltage-gain required for LLC resonator needs to be calculated. The maximum voltage gain Mg_nom_max required by LLC resonator under normal conditions is calculated using the following equation.

$$Mg\_\mathrm{nom\_max} = \frac{n \times Vout\_A\_max}{Vout\_PFC\_min\ /2}$$

If the accuracy of output voltage Vout_LLC = 54.5V is ±5%, the accuracy of output voltage Vout_A = 27.25V of the transformer alone is also ±5%, and the value of Vout_A_max = 28.61V. And if the accuracy of output voltage Vout_PFC = 390V is ±5%, the minimum voltage value is 370.5V, but by considering the margins Vout_PFC_min = 360V. Since n is 7.75, Mg_nom_max = 1.23. After including margin in maximum load, at 105% load the voltage gain meets Mg_nom_max = 1.23.

Next, calculate the max. voltage-gain Mg_hold_max required by LLC resonating circuit at the momentary power failure of AC. In the event of an instantaneous power failure, if the voltage gain at which LLC output voltage can satisfy the minimum specification at the max. load, it shall be deemed to be satisfactory and calculated using the following equation.

$$Mg\_\mathrm{hold\_max} = \frac{n \times Vout\_A\_min}{Vout\_PFC\_hold\ /2}$$

If n is 7.75, the output voltage Vout_A_min of the transformer alone with the output voltage lower limit of this power supply (rated output-5%) = 25.89V, and PFC output voltage lower limit at instantaneous power failure be Vout_PFC_hold = 300V. Thus, Mg_hold_max = 1.34.

From the above, the required voltage gain for LLC resonant circuit is Mg_nom_max = 1.23 for 105% load and Mg_hold_max=1.34 for 100% load. In the following calculations, the voltage gain required for LLC resonant circuit is set as follows: Mg_nom_max at 105% load = 1.23, and the final stage of the design is to ensure that the voltage gain at 105% load is Mg_nom_max = 1.23.

Next, the minimum-voltage-gain value Mg_min required by LLC resonator is calculated using the following equation.

$$Mg\_min = \frac{n \times Vout\_A\_min}{Vout\_PFC\_max\ /2}$$

If n is 7.75, Vout_A_min = 25.89V, and the maximum value of Vout_PFC Vout_PFC_max = 420 V, then Mg_min = 0.96.

Equivalent load resistance calculation

The FHA transforms LLC resonant circuit into a simple equivalent circuit. Fig. 4.22 shows the circuit diagram for extracting LLC resonant circuit of a single transformer from the 3-phase Y-connection circuit of this design.

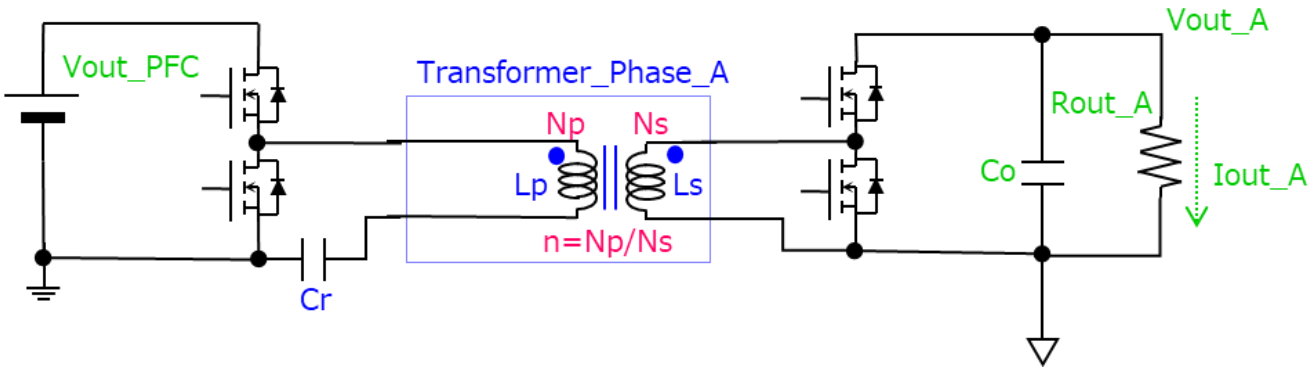


Fig. 4.22 Single LLC Resonant Circuit Extracted from 3-Phase Y-Connection Circuit

Here, Np is the number of windings of the primary winding of the resonant transformer, Ns is the number of turns of the secondary winding, n is the turns ratio, Lp is the primary inductance (open inductance), Ls is the secondary inductance, Cr is the resonant capacitor, Co is the output capacitor, Rout_A is the load resistance of a single transformer, Vout_A is the output voltage, and Iout_A is the output current.The equivalent circuit considering the transformer excitation inductance and leakage inductance is shown in Fig. 4.23.

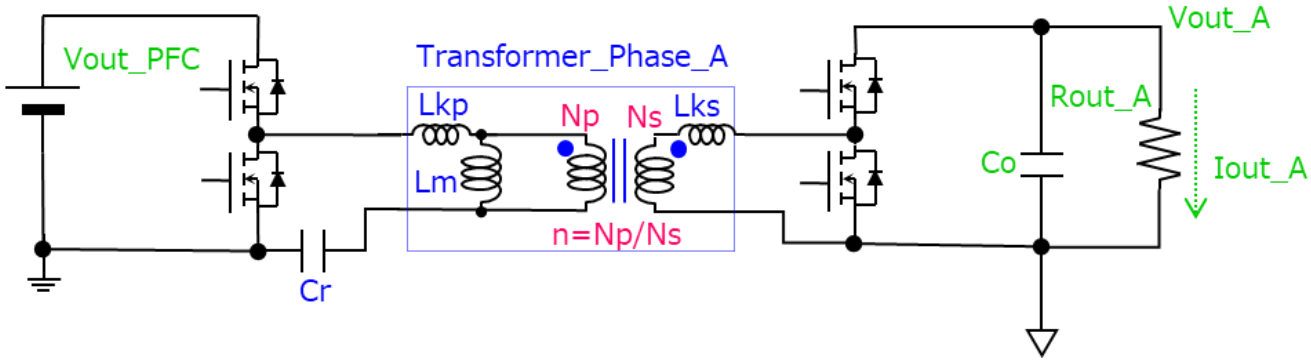


Fig. 4.23 LLC Resonant Circuit Considering Excitation Inductance and Leakage Inductance of Transformer

Since the transformer coupling factor is the same for the primary and secondary sides, the relation between the primary side leakage inductance Lkp and the secondary side leakage inductance Lks is expressed by the following equations.

$$Lkp = n^2 Lks$$

When the excitation inductance is Lm and the short inductance that is measured by shorting the resonant transformer secondary side is taken as Lx, the open inductance Lp and the primary leakage inductance Lkp are expressed by the following equations.

$$Lp = Lm + Lkp$$

$$Lx = Lkp + \frac{Lkp * Lm}{Lkp + Lm}$$

In LLC resonant circuit, there are two resonant frequencies: the resonant frequency fp of the open inductance Lp and the resonant capacitor Cr, and the resonant frequency f0 of the short inductance Lx and the resonant capacitor Cr. The relationship between them is as follows.

$$fp = \frac{1}{2\pi\sqrt{Lp * Cr}}$$

$$f0 = \frac{1}{2\pi\sqrt{Lx * Cr}}$$

In LLC resonant circuit, the switching-frequency fsw operates based on f0. If the switching frequency fsw is less than fp, LLC will deviate from the resonance. This results in hard switching, which may lead to a drop in power conversion efficiency and damage to the devices. Therefore, it must be operated at a switching-frequency higher than fp.

Fig. 4.24 shows an equivalent circuit when the secondary-side leakage inductance Lks is converted to the primary side. Fig. 4.25 shows a simplified equivalent circuit of LLC resonant circuit.

The following shows the relation between the load Rout_A of LLC resonant circuit and the equivalent load resistor RLe in LLC resonant simplified equivalent circuit.

$$RLe = \frac{8n^2}{\pi^2} Rout\_A$$

In LLC resonant simplified equivalent circuit of the single transformer, with the output voltage Vout_A = 27.25V and the output power Pout_A = 266.67W, the equivalent load-resistance RLe is as follows.

$$RLe = \frac{8n^2}{\pi^2} Rout\_A = \frac{8n^2}{\pi^2} * \frac{(Vout\_A)^2}{Pout\_A} = 135.57\Omega$$

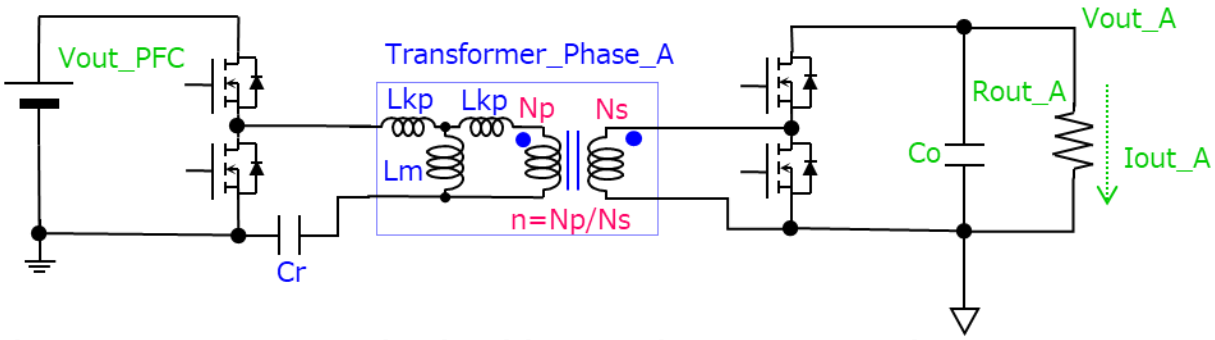


Fig. 4.24 LLC Resonant Circuit With Secondary Leakage Inductance of Resonant Transformer Converted to Primary Side

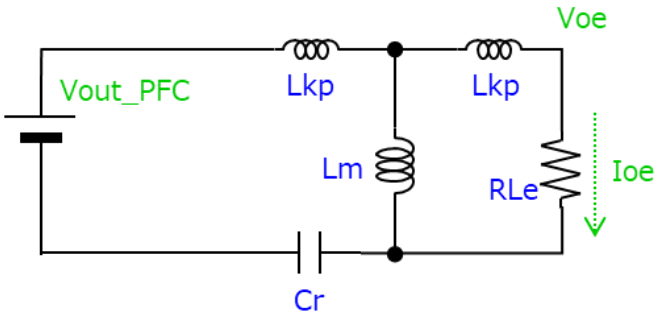


Fig. 4.25 LLC Resonant Simplified Equivalent Circuit

Resonant circuit quality factor derivation

Fig. 4.26 shows the relation between the maximum gain of LLC resonant circuit Mg_max and quality factor Qe of the resonant circuit in the FHA. In this diagram, Ln is the ratio of the exciting inductance Lm of the resonant transformer to the leakage inductance Lk (Ln = Lm/Lk). If Ln = 12, the quality factor Qe is 0.28 when Mg_max = 1.23.

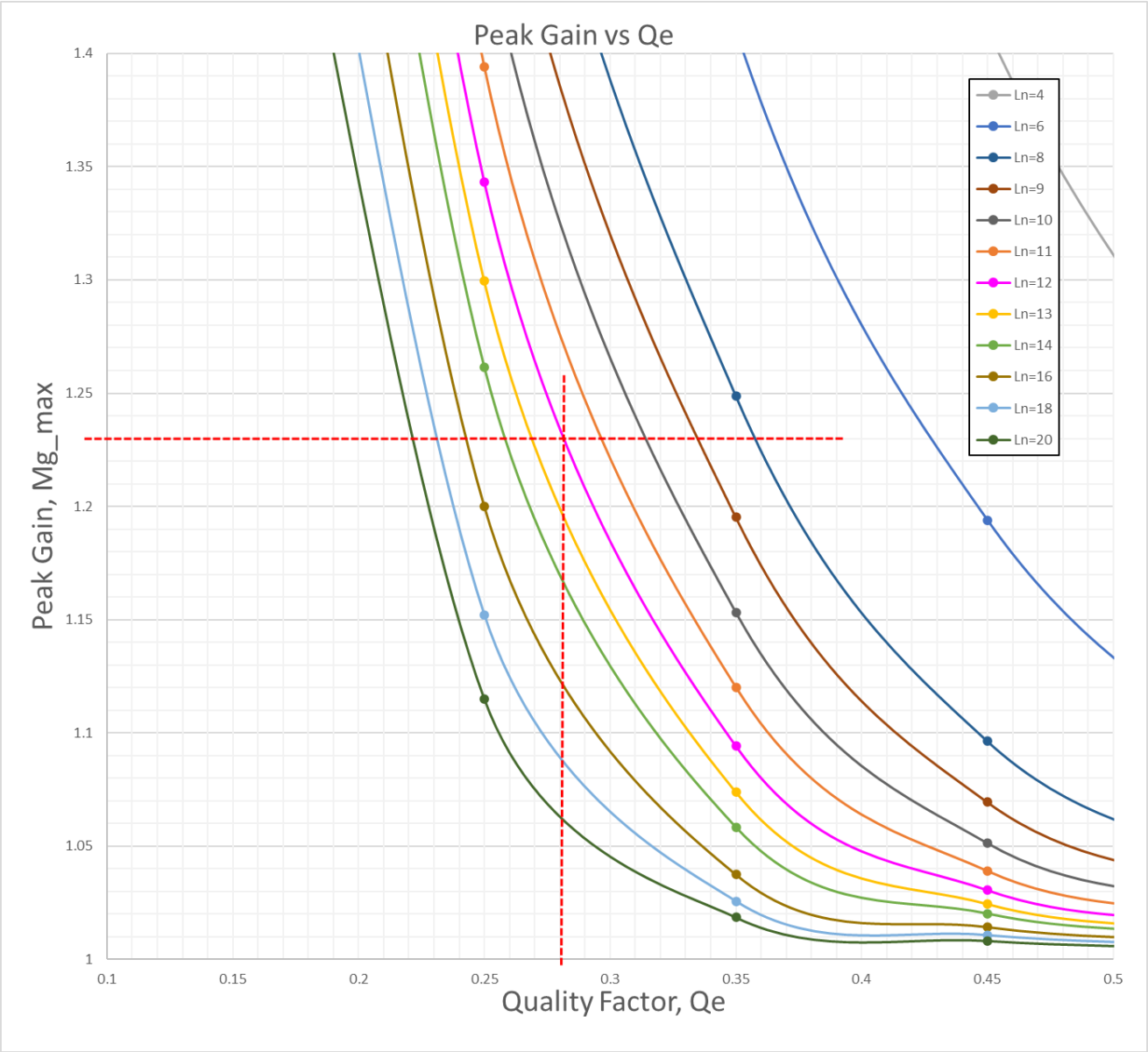


Fig. 4.26 LLC Resonant Circuit: Max. Voltage Gain and Quality Factor Relation Diagram

From the above, the quality factor should be set near Qe = 0.28 to ensure Mg_nom_max = 1.23 at 105% load including margins at maximum load. In the FHA, the resonant transformer is defined as an ideal transformer, so the leakage inductance Lk is assumed to be the same as the short-circuit inductance Lx.

However, when the resonant transformer leakage inductance is used to construct an LLC resonant circuit, the primary leakage inductance Lkp and the short-circuit inductance Lx do not become the same value, but have the relation shown below. Where Lm is the excitation inductance.

$$Lx = Lkp + \frac{Lkp * Lm}{Lkp + Lm}$$

The reference operating switching frequency f0 of LLC resonant circuit is the resonant frequency of the short inductance Lx and the resonant capacitor Cr. Therefore, the ratio between the excitation inductance Lm of the resonant transformer and the leakage inductance Lk (Ln = Lm/Lk) defined in the relation diagram (Fig. 4.26) between Mg_max and the quality factor Qe in the FHA is different from the ratio between the actual excitation inductance Lm and the short-circuit inductance Lx. However, this value is useful for calculating the approximate value of the excitation inductance Lm.

The quality factor Qe is given by the following equation. RLe is the equivalent load-resistance value of the simple equivalent circuit of LLC resonant circuit.

$$Qe = \frac{\sqrt{Lx/Cr}}{RLe}$$

Cr, Lx, Lm, Lkp calculation

Relation between resonant capacitor Cr and short inductance Lx, resonant frequency f0, equivalent load resistance RLe, and quality factor Qe is shown below.

$$Cr = \frac{1}{2 * \pi * f0 * RLe * Qe}$$

When f0 is 80kHz, RLe = 135.57Ω and Qe = 0.28, the Cr is calculated to be Cr = 52.41nF. This time, three 18nF are used in parallel to make Cr = 54nF.

The following shows the relational expression and calculation of the short inductance Lx, Cr, f0.

$$Lx = \frac{1}{(2 * \pi * f0)^2 * Cr} = 73.29(\mu H)$$

The relation between Lx and Lkp is:

$$Lx = Lkp + \frac{Lkp * Lm}{Lkp + Lm} = 73.29(uH)$$

Ln is the ratio of the excitation inductance Lm and primary leakage inductance Lkp set by resonant-circuit quality factor derivation.

$$Ln = \frac{Lm}{Lkp} = 12$$

Relation between open inductance Lp and exciting inductance Lm and primary leakage inductance Lkp is:

$$Lp = Lm + Lkp$$

The excitation inductance Lm, primary leakage inductance Lkp, and open inductance Lp are calculated from these values as shown below.

Lkp = 38.11μH, Lm = 457.33μH, Lp = 495.44μH

n, Lp, Lx, Cr determination, and Lm, Lkp, Lks, k, fp, f0 calculation

The specifications of the resonant transformer and the resonant capacitor based on the above calculation results are determined below.

Resonant transformer turns ratio: n = 7.75 (Np:Ns = 31:4)

Resonant transformer open inductance: Lp = 480μH

Resonant transformer short inductance: Lx = 70μH

Resonant capacitor: Cr = 54nF

Following are the calculation results of excitation inductance, leakage inductance, transformer coupling coefficient, and resonant frequency of the resonant transformer.

Resonant transformer excitation inductance: Lm = 443. 62μH

Resonant transformer primary leakage inductance: Lkp = 36. 38μH

Resonant transformer secondary leakage inductance: Lks = Lkp/n^2 = 605.7nH

Resonant transformer coupling factor: a = Lm/Lp = 0.92

Resonant frequency of a resonant transformer with open inductance Lp and a resonant capacitor Cr: fp = 30.22kHz

Resonant Frequency of a resonant transformer with short inductance L0 and resonant capacitor Cr: f0 = 81.86kHz

4.6.3. Resonant Circuit Voltage Gain Confirmation

It must be confirmed that the switching frequency transitions properly within the assumed range in the resonant circuit using the designed resonant transformer and resonant capacitor. An LLC converter transfer graph is used to describe the relation between the switching frequency and the voltage gain of the resonant circuit.

LLC Converter Transfer Function M calculation

LLC converter transfer function M is calculated by the following equation. The value of M indicates the relationship between the switching frequency of the resonant circuit and the voltage gain according to the load.

$$M = \frac{2n * Voe}{Vout\_PFC} = \frac{1}{\sqrt{(\frac{1}{a}(1 - \frac{1-a^2}{fsw^2} * f0^2))^2 + (\frac{Qe}{a}(\frac{fsw}{f0} - \frac{f0}{fsw}))^2}}$$

Qe in the above equations is the variable-quality factor due to the load. The following shows the relation between Qe and the secondary-side load Pout_A of the transformer.

$$Qe = \frac{\sqrt{Lx/Cr}}{RLe} = \sqrt{Lx/Cr} * \frac{\pi^2}{8n^2 * Rout\_A} = \sqrt{Lx/Cr} * \frac{\pi^2}{8n^2} * \frac{Pout\_A}{(Vout\_A)^2}$$

Where no-load Pout_A_min = 0W, max-load Pout_A_max = 266.67W,
The calculation result of Qe at each load is shown from Pout_A_max +5% at the maximum load +5% = 280W.

At no-load: Qe_min = 0

At maximum load: Qe_max = 0.27

At maximum load at +5%: Qe_max+5% = 0.28

From the above calculation, Qe transits between 0.00 and 0.28. In addition, in the Resonant Circuit Quality Factor Derivation section, it is approximated to Qe = 0.28 calculated at maximum load, which confirms that it is appropriate for LLC resonant designs.

In the next section, the relation between LLC converter transfer function M and the switching frequency fsw for each Qe is used to check whether the switching frequency transition area is appropriate.

Resonant circuit voltage gain confirmation and switching frequency transition range confirmation

Fig. 4.27 shows the relation between the switching-frequency fsw and the voltage gain of a resonant circuit using a transformer and a resonant capacitor.

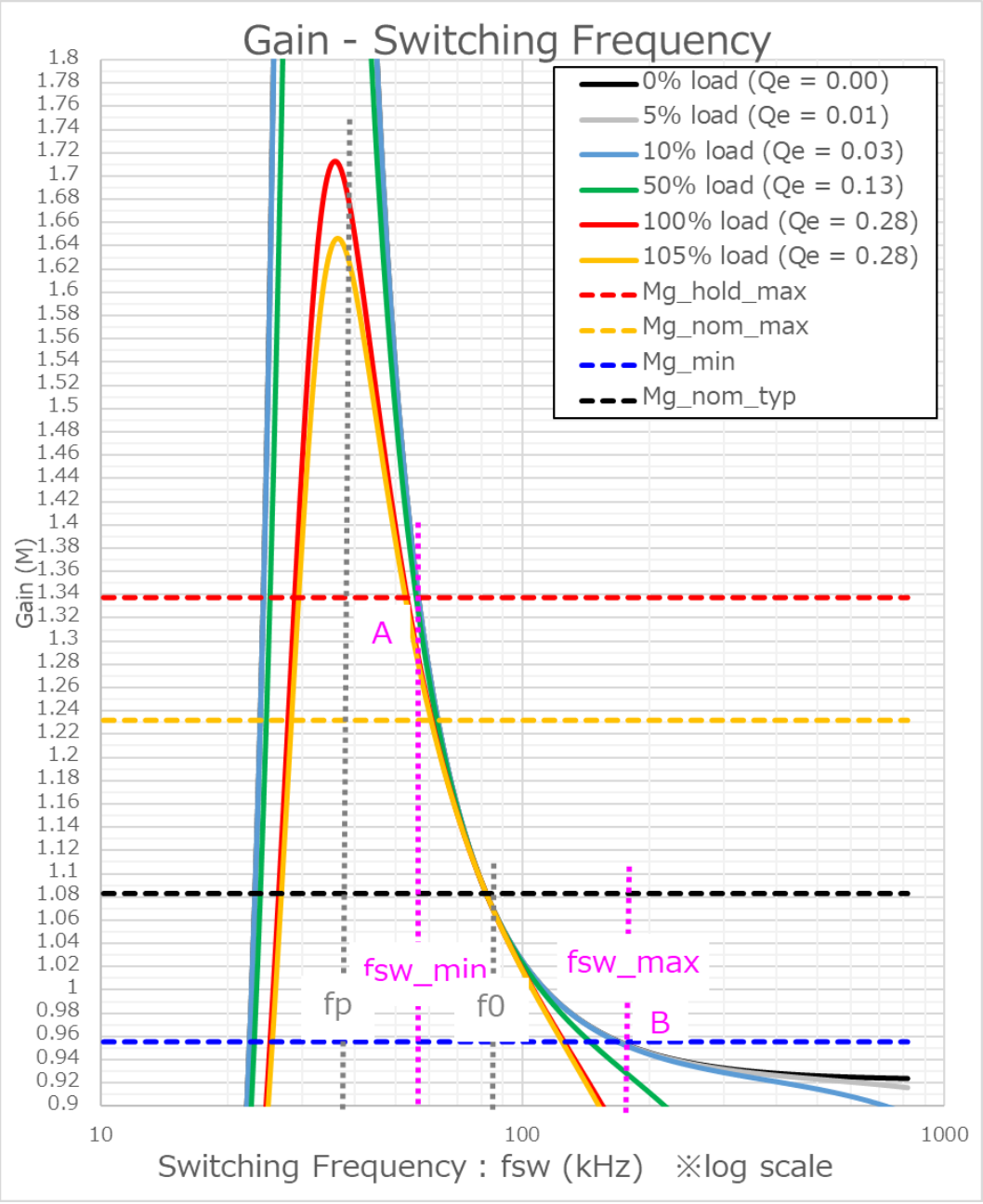


Fig. 4.27 LLC Resonant Circuit Voltage Gain and Switching Frequency Relation Diagram

Since the gain curve of Qe = 0.28 at 105% load including the margin for the maximum load reaches the maximum required voltage gain Mg_nom_max = 1.23, so it can be confirmed that the required gain is secured at the maximum load +5%. In addition, since the gain curve Qe = 0.27 at the maximum load reaches the required gain at instantaneous power failure Mg_hold_max = 1.34, it is also possible to confirm that the required voltage gain is secured at the instantaneous power failure under the maximum load condition. The switching frequency obtained at the intersection of the gain curve and Mg_hold_max (point A in the diagram) is the minimum switching frequency fsw_min of LLC power supply. Since fsw_min is smaller than the resonant frequency fp of the

resonant transformer with open inductance Lp and resonant capacitor Cr, it can be confirmed that this LLC power supply does not deviate from the soft-switching operation area due to resonance at both maximum load and instantaneous stop.

The maximum switching frequency fsw_max of LLC power supply is obtained at the intersection of the gain curve Qe = 0.00 at the minimum load and the minimum required gain Mg_min = 0.96 (point B in the diagram).

Fig. 4.28 shows the relation between the switching frequency (fsw) and the voltage gain near the required maximum voltage gain.

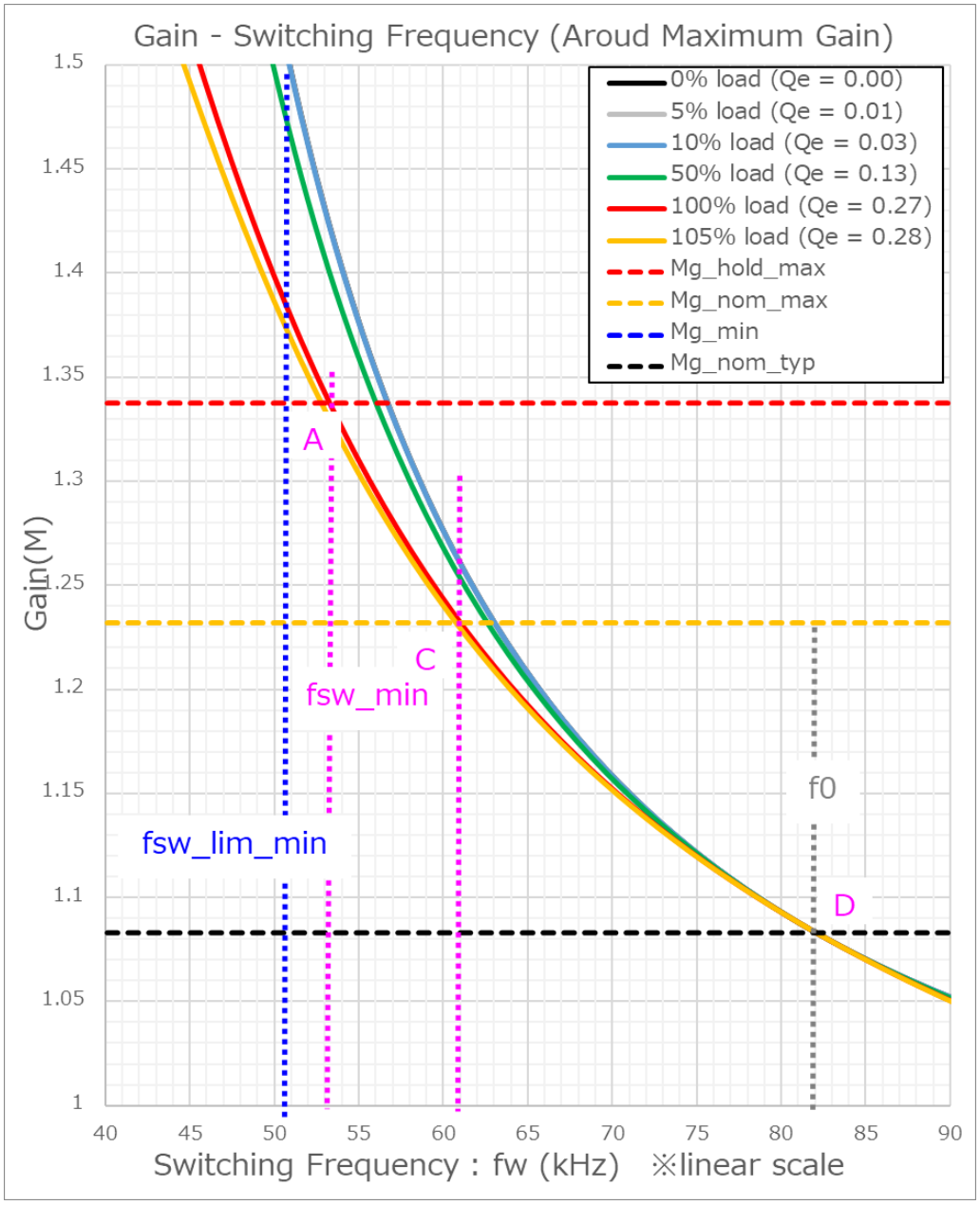


Fig. 4.28 LLC Resonant Circuit Voltage Gain and Switching Frequency Relation Diagram (Expansion Near Required Maximum Gain, Frequency Axis in Linear Scale)

The minimum switching frequency in the steady state is 60.5kHz from the intersection of the gain curve (Point C in figure) between the maximum voltage gain required at maximum load +5% in steady state Mg_nom_max = 1.23 and the gain curve of Qe = 0.28 at the maximum load +5% in the steady state. Also, since the required voltage-gain at instantaneous power failure Mg_hold_max = 1.34 is larger than that of Mg_nom_max, the minimum switching frequency fsw_min of the LLC poiwer supply is 53.0kHz from the intersection of the gain curves Qe = 0.27 and Mg_hold_max = at maximum load (point A in the diagram).It is confirmed that this circuit operates correctly in designated condition, because the 53kHz is higher than the 50kHz which is the minimum switching frequency set by the LLC controller.

The intersection of the voltage gain Mg_nom_typ = 1.08 and the gain curve Qe = 0.27 at full load (point D in the figure) at the center value of Vout_PFC_typ = 390 V and Vout_A_typ = 27.25 V for both input voltage and output voltage is almost the same as the resonant frequency f0 of the resonant transformer with short inductance L0 and the resonant capacitor Cr. In the LLC resonant circuit, the most stable operation is achieved when the switching frequency fsw is f0, so it can be confirmed that the input / output voltage center value is set so that the current LLC power supply operation is set to be the most stable.

Fig. 4.29 shows the relation between the switching frequency (fsw) and the voltage gain in the vicinity of the required minimum voltage gain.

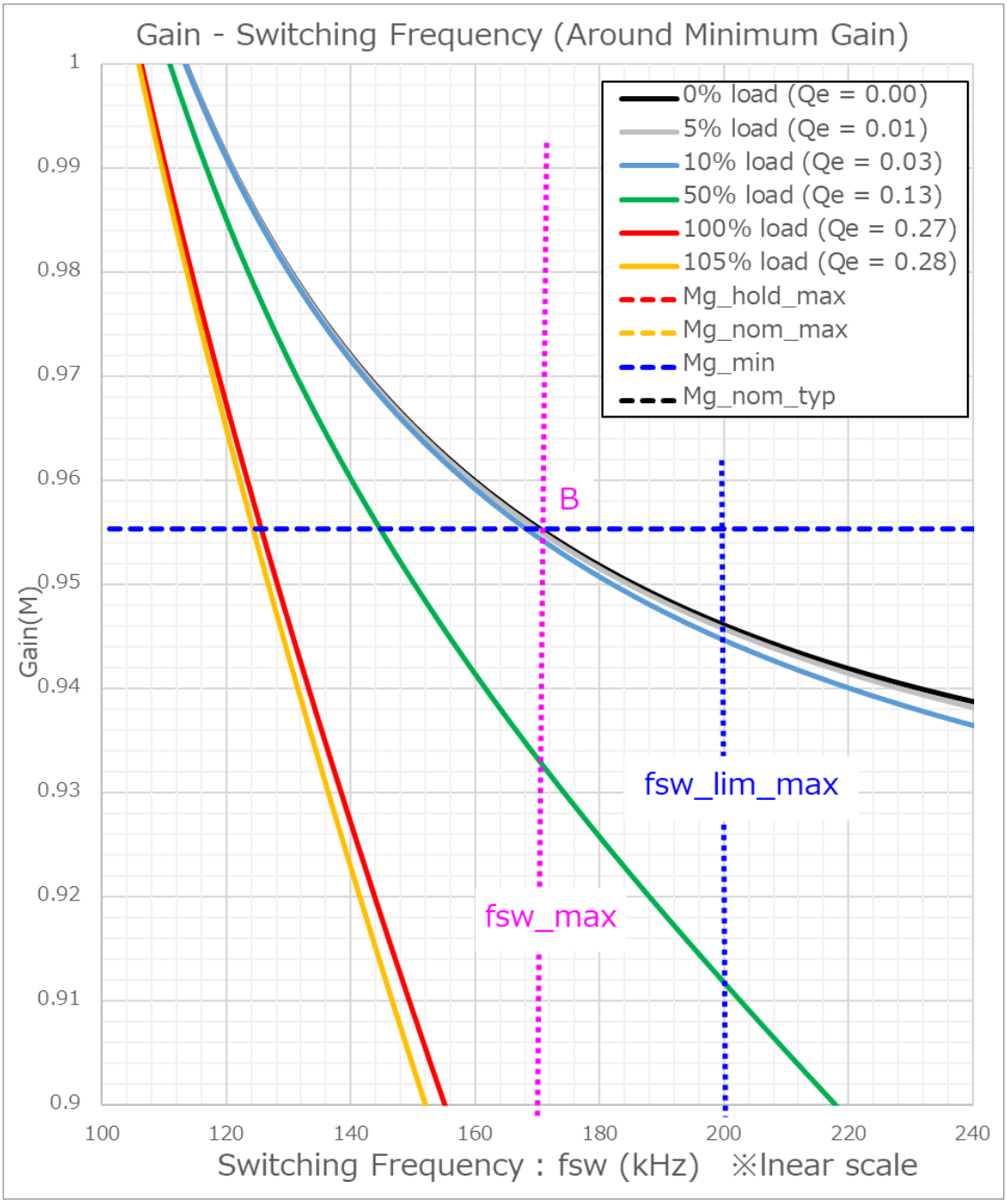


Fig. 4.29 LLC Resonant Circuit Voltage Gain and Switching Frequency Relation Diagram (Near Required Minimum Gain Expansion, Frequency Axis in Linear Scale)

From the intersection of the gain curve of Mg_min = 0.96 required for the minimum load in steady state and Qe = 0.00 at minimum load (point B in the diagram), the maximum switching frequency fsw_max of the LLC power supply is 170.0kHz. It is below the upper limit of the switching frequency of the LLC part of this design, which is fsw_lim_max 200.0 kHz, which was set in the LLC controller peripheral circuit design, and normal operation within the limit range can be confirmed.

From the above confirmation, it can be confirmed that the switching frequency transition range of LLC resonant power supply is as follows, and is within the switching frequency limit range set in the LLC controller peripheral design.

Minimum switching frequency: fsw_min = 53kHz

Maximum switching frequency: fsw_max = 170kHz

4.6.4. Resonant Transformer Current Calculation and ZVS (Zero Volt Switching) Confirmation

This section shows the calculation of the current of the designed resonant transformer and the confirmation of the ZVS establishment conditions of soft switching.

Current calculation of the resonant transformer

Calculation of the maximum current Iout_A_max in Fig. 4.24. In this case, the output voltage accuracy is ±5%, the minimum output voltage Vout_A_min = 25.89V, and the maximum power Pout_A_max = 266.67 x 1.05 = 280W, including a margin of +5% at the maximum load.

$$Iout\_A\_max = \frac{Pout\_A\_max}{Vout\_A\_min} = 10.81(A)$$

The peak load current value Is_A_peak_max flowing in the secondary winding and the peak load current value Ip_A_peak_max flowing in the primary winding are calculated on the assumption that sinusoidal current flows in the secondary winding.

$$Is\_A\_peak\_max = \frac{\pi}{2} * Iout\_A\_max = 16.98(Apeak)$$

$$Ip\_A\_peak\_max = \frac{\pi}{2n} * Iout\_A\_max = 2.19(Apeak)$$

The load current effective value Is_A_rms_max that flows in the secondary winding and the load current effective value Ip_A_rms_max that flows in the primary winding are calculate below.

$$Is\_A\_rms\_max = \frac{1}{\sqrt{2}}\ Is\_A\_peak\_max = \frac{\pi}{2\sqrt{2}} * Iout\_A\_max = 12.01(Arms)$$

$$Ip\_A\_rms\_max = \frac{1}{\sqrt{2}}\ Ip\_A\_peak\_max = \frac{\pi}{2n\sqrt{2}} * Iout\_A\_max = 1.55(Arms)$$

The primary side has an excitation current that flows through the excitation inductor in addition to the above. The peak value Im_A_peak_max and the rms value Im_A_rms_max of the excitation current is calculated using the following formula. In this case, the maximum output voltage Vout_A_max = 28.61V from the excitation inductance Lm = 443.62μH, the minimum switching frequency fsw_min = 53.00kHz, and the output voltage accuracy is ±5%.

$$Im\_A\_peak\_max = \frac{n}{4 * Lm * fsw\_min} * Vout\_A\_max = 2.36(Apeak)$$

$$Im\_A\_rms\_max = \frac{1}{\sqrt{2}}\, Im\_A\_peak\_max = \frac{n}{4\sqrt{2} * Lm * fsw\_min} * Vout\_A\_max = 1.67(Arms)$$

The total peak current Itotal_A_peak_max and the total rms current Itotal_A_rms_max on the primary side are calculated as follows.

$$Itotal\_A\_peak\_max = \sqrt{(Ip\_A\_peak\_max)^2 + (Im\_A\_peak\_max)^2} = 3.22(Apeak)$$

$$Itotal\_A\_rms\_max = \sqrt{(Ip\_A\_rms\_max)^2 + (Im\_A\_rms\_max)^2} = 2.28(Arms)$$

Itotal_A_peak_max and Itotal_A_rms_max are equivalent to the maximum current flowing through the resonant capacitor.

Zero volt switching confirmation

LLC resonant power supply achieves high-efficiency ZVS by charging and discharging the switching MOSFET's output capacitance with the energy stored by the excitation current of the transformer. In order to achieve ZVS in a wide range of loading conditions, ZVS condition must be satisfied even under the condition that the excitation current Im_A_rms is minimal. ZVS is satisfied when the energy stored by the exciting current of the transformer exceeds the energy required to charge/discharge MOSFET output capacitance. When the excitation current is at minimum, the maximum switching frequency fsw_max = 170.00kHz, and the minimum output voltage Vout_A_min = 25.89V, the minimum excitation current Im_A_rms_min is calculated as follows.

$$Im\_A\_rms\_min = \frac{1}{\sqrt{2}}\, Im\_A\_peak\_min = \frac{n}{4\sqrt{2} * Lm * fsw\_max} * Vout\_A\_min = 0.47(Arms)$$

At this time, the minimum energy value Ep_min stored in the transformer on the primary side is calculated as follows.

$$Ep\_min = \frac{1}{2} Lp * (Im\_A\_rms\_min)^2 = 53.09(\mu J)$$

ZVS can be achieved if the output capacitance of the switching MOSFET can be charged and discharged with the energy calculated above. The maximum energy required for charging/discharging a single MOSFET TK125A60Z1 Ezvs_max is calculated as follows when the output capacitance energy equivalent effective capacitance value Co_er = 70pF and the input maximum voltage Vout_PFC_max = 420V.

$$Ezvs\_max = \frac{1}{2} Co\_er * (Vout\_PFC\_max)^2 = 6.17(\mu J)$$

There are two switching MOSFETs, one on high side and another on low side. Therefore, in order to achieve ZVS with this LLC resonant power supply, it is necessary to double the maximum energy required for charging/discharging Ezvs_max. Since the minimum energy stored in the primary side of the transformer Ep_min = 53.09μJ, is more than 2 times the maximum energy required for charging and discharging the switching MOSFET TK125A60Z1 Ezvs_max x 2 = 12.34μJ, it can be confirmed that ZVS can be established even under the worst situation with the minimum excitation current and maximum energy required for ZVS.

4.7. ORing Circuit

Fig. 4.30 shows ORing circuit. ORing Controller LM5050-1 (made by Texas Instruments) operates as an ideal diode rectifier in conjunction with an external MOSFET when connected in series with a power supply. GATE is deactivated if V_{IN}>V_{OUT}. In addition, the MOSFET can be turned off by setting the OFF pin high.

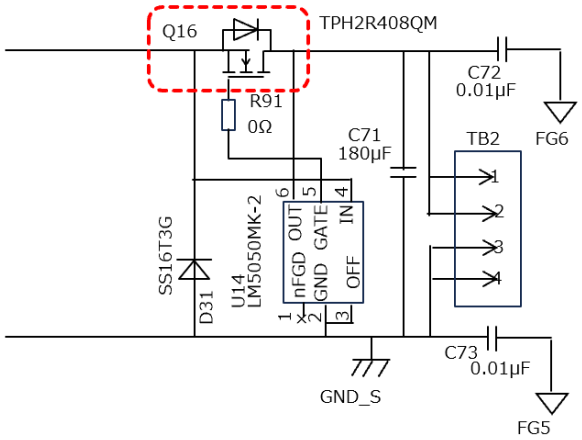


Fig. 4.30 ORing Circuit

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