3-Phase AC 400V Input
Vienna Rectifier PFC Power Supply
Design guide

RD207-DGUIDE-01

Toshiba Electronic Devices & Storage Corporation

Table of Contents

1. Introduction

This design guide describes the circuit design of various sections of the 3-Phase AC Input Vienna Rectifier PFC Power Supply (hereinafter referred to as “this Design”).

3-phase AC power is provided to industrial facilities, etc., and 400V (line voltage) systems are widely used outside Japan. When using such 3-phase AC 400V system inputs for EV chargers and other equipment, a PFC (Power Factor Correction) power supply that rectifies AC to DC with a high power-factor is essential. This design is a PFC power supply that inputs a 3-phase AC 400V and outputs a DC 750V. A Vienna rectifier topology is used to achieve high-efficiency in 3-level operation, and power can be supplied to 5kW.

The bi-directional switching section uses 650V a power MOSFET TK065N65Z, and the rectifier section uses a 1200V SiC Schottky barrier diode TRS15N120HB. Thanks to hose our latest power devices, it achieves low power-loss. In addition, the driver coupler TLP5774H is used for the insulated drive of MOSFET, and the isolation amplifier TLP7920F is used for the insulated sensing of the input and output voltages.

2. Main Components Used

This chapter describes the main components used in this design.

2.1. Power MOSFET TK065N65Z

A 650V N-channel MOSFET TK065N65Z is used for the center point bi-directional switching section. The main features of TK065N65Z are as follows.

- Low drain-source on-resistance: $R_{DS(ON)}$ = 0.054Ω (Typ.)
- High-speed switching properties with lower capacitance.
- Enhancement mode: V_{th} = 3 to 4V (V_{DS} = 10V, I_D = 1.69mA)

Appearance and Pin Layout

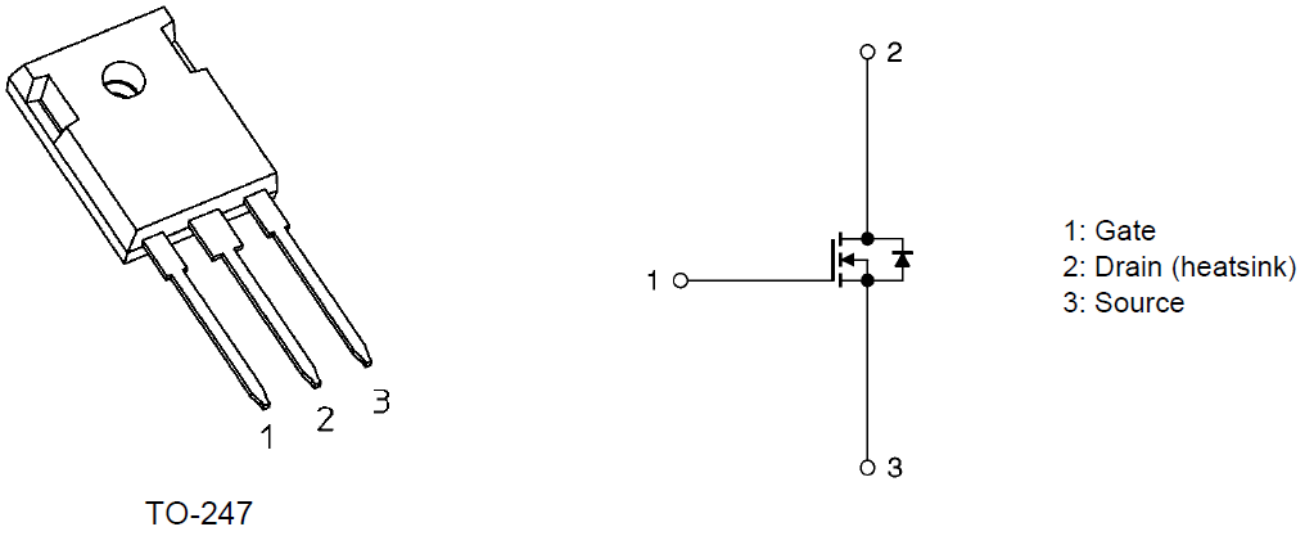


Fig. 2.1 Appearance and Pin Layout of TK065N65Z

2.2. SiC Schottky Barrier Diode TRS15N120HB

A 1200V diode TRS15N120HB is used for the rectification section on input-side. The main features of TRS15N120HB are as follows.

- Chip design of 3rd generation
- Low forward voltage: V_F (Per Leg) = 1.27V (Typ.)
- Low total capacitive charge: Q_C (Per Leg) = 43nC (Typ.)
- Low reverse current: I_R (Per Leg) = 0.7μA (Typ.)

Appearance and Terminal Layout

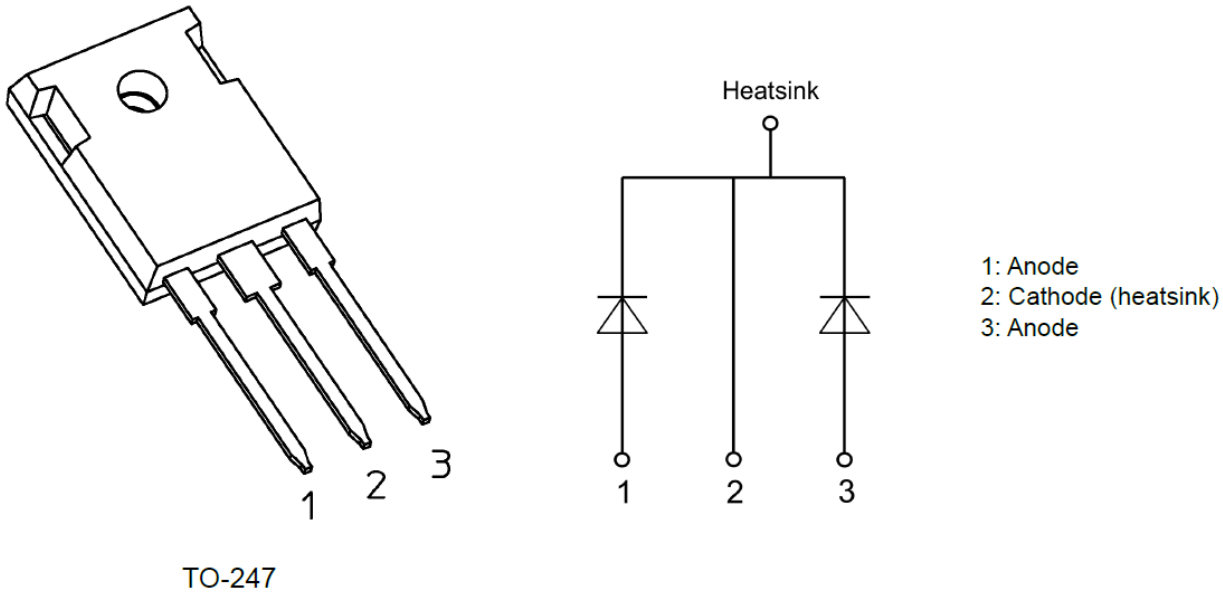


Fig. 2.2 Appearance and Pin Layout of TRS15N120HB

2.3. Driver Coupler TLP5774H

A gate driver coupler TLP5774H is used for the gate driver of MOSFET. The main features of TLP5774H are as follows.

- Buffer logic type (totem pole output)
- Output peak current: ±4.0A (Max.)
- Operating temperature: -40 to 125℃
- Supply current: 3mA (Max.)
- Supply voltage: 10 to 30V
- Threshold input current: 2mA (Max.)
- Propagation delay time: 150ns (Max.)
- Common-mode transient immunity: ±35kV/μs (Min.)
- Isolation voltage: 5000Vrms (Min.)
- Complies with safety standards

Appearance and Pin Layout

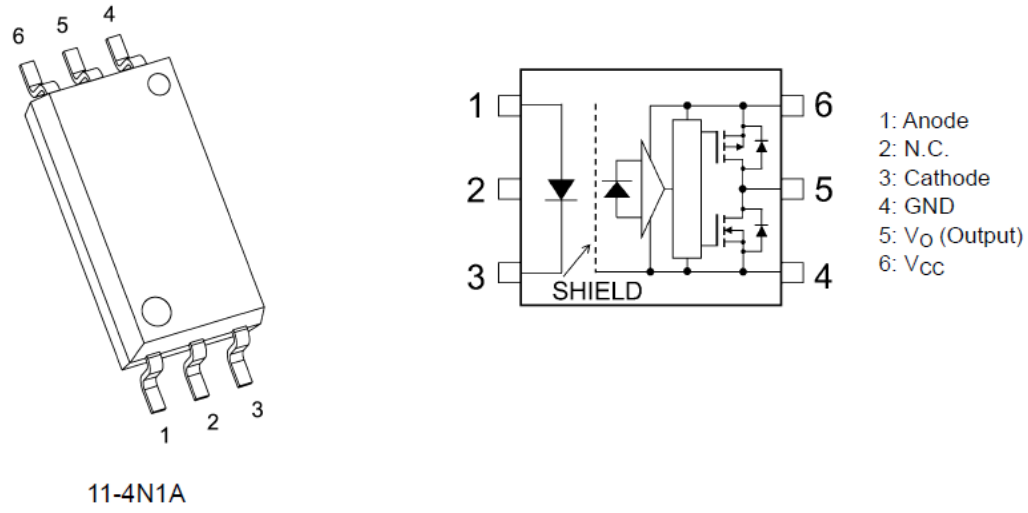


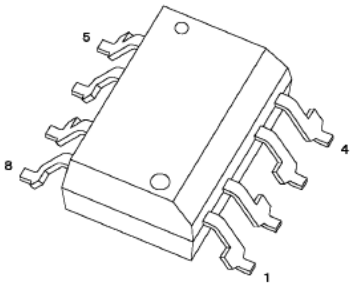
Fig. 2.3 Appearance and Pin Layout of TLP5774H

2.4. Isolation Amplifier TLP7920F

An optically isolation amplifier TLP7920F is used for isolated sensing of the input/output voltage. The main features of TLP7920F are as follows.

- Ooutput side supply voltage: 3.0 to 5.5V
- Output side supply current: 6.2mA (Typ.)
- Operating temperature range: -40 to 105℃
- Common-mode transient immunity: 15kV/μs (Min.)
- Complies with safety standards

Appearance and Pin Layout



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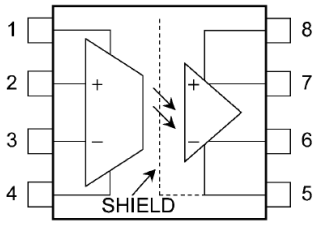


Pin No.	Symbol	Description
1	V_{DD1}	Input side supply voltage
2	V_{IN+}	Positive input
3	V_{IN-}	Negative input
4	GND1	Input side ground
5	GND2	Output side ground
6	V_{OUT-}	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Output side supply voltage

Fig. 2.4 Appearance and Pin Layout of TLP7920F

3. Vienna Rectifier Circuit

This chapter describes an outline of the operation of Vienna rectifier circuit, in particular, the circuit method adopted in this design (Vienna PFC circuit).

3.1. Vienna PFC Circuit

Fig. 3.1 shows the configuration of Vienna PFC circuit adopted in this design. This is a 3-phase and 3-level AC-DC converter.

Whereas the two-level circuit controls the two-level voltage of the power supply voltage and GND, the 3-level circuit creates a potential at the mid-point between the power supply voltage and GND, and controls the 3-level voltage of the power supply voltage, the mid-point, and GND. This Vienna PFC circuit is used in high-power, 3-phase applications such as chargers for EV (electric vehicles). 3-level control of the control voltage amplitude reduces the voltage amplitude at switching to half that at 2-level control, and it is possible to use a device with lower withstand voltage compared to the 2-level circuit. Generally, the lower the withstand voltage of a switching element of the same size, the smaller the loss at the operation, enabling highly efficient operation compared to a 2-level circuit.

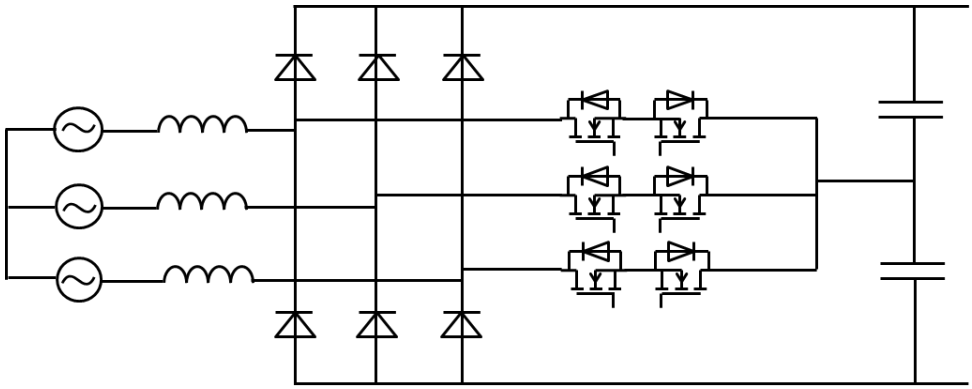
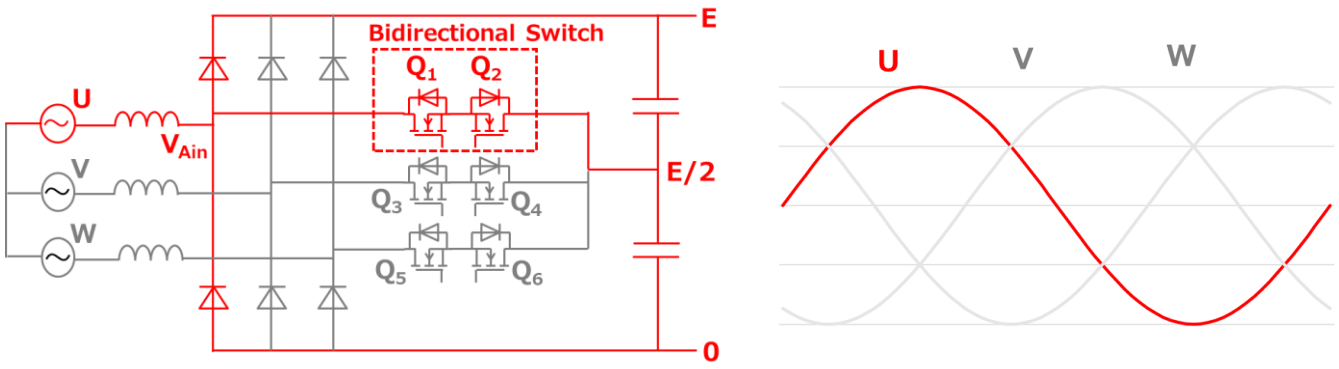


Fig. 3.1 Vienna PFC Basic Circuit

3.2. Vienna PFC Circuit Operation

Fig. 3.2 shows the Vienna PFC circuit and the input V_{in} voltage waveforms. Fig. 3.2 (a) shows the operation circuit for 1-phase, and Fig. 3.2 (b) shows the input waveform in red. 1-phase of Vienna PFC circuit operates by turning Q_1 and Q_2 on/off in the circuit shown in Fig. 3.2 (a), and by controlling the voltage of V_{Ain} of the circuit with 3-level voltages of 0, E/2, and E, the input current is approximated to a sine wave. Each phase performs the same operation with a phase difference of 120°.



(a) Vienna PFC 1-Phase Operation Circuit

(b) 3-Pphase Input-Waveform

Fig. 3.2 Vienna PFC Circuit and Input V_{in} Waveforms

The circuit operation for 1-phase of Vienna PFC circuit shown in Fig. 3.2 is explained in Fig.3.3.

[When the input voltage V_{in} is positive]

Q_1 and Q_2 are turned on/off as shown in Fig. 3.3. When the Q_1 and Q_2 are off, current flows the path shown in Mode 1 and V_{Ain} voltage is E. When they are on, current flows the path shown in Mode 2 and V_{Ain} voltage is E/2. Mode 1 and Mode 2 repeat. The gate-voltage, V_{Ain} voltage, and input-current waveform images of Q_1 and Q_2 are shown in Fig. 3.5.

[When the input voltage V_{in} is negative]

Q_1 and Q_2 are turned on/off as shown in Fig. 3.3. When the Q_1 and Q_2 are off, current flows the path shown in Mode 3 and V_{Ain} voltage is 0. When they are on, current flows the path shown in Mode 4 and V_{Ain} voltage is E/2. Mode 3 and Mode 4 repeat. The gate-voltage, V_{Ain} voltage, and input-current waveform images of Q_1 and Q_2 are shown in Fig. 3.5.

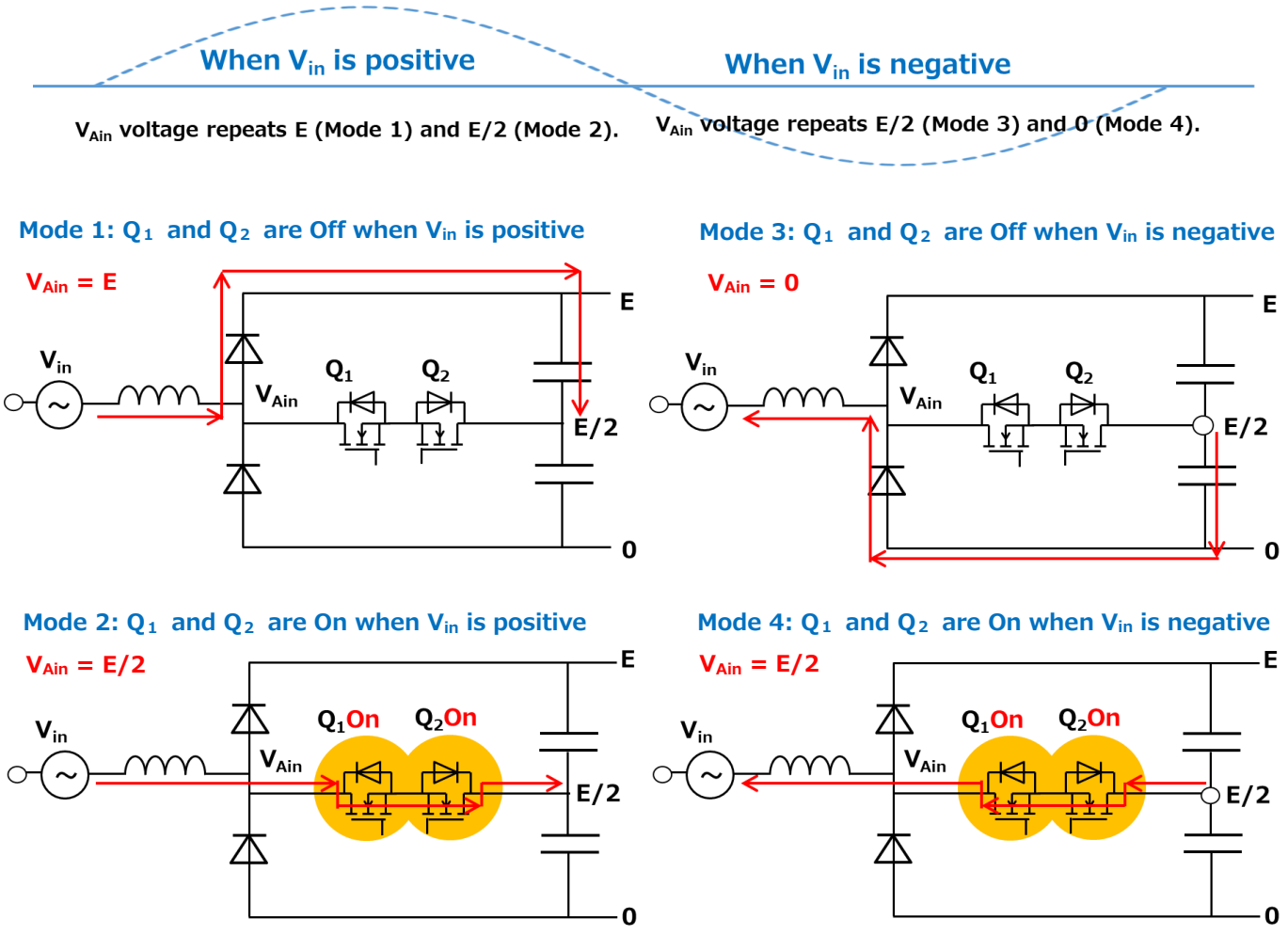


Fig. 3.3 Vienna PFC Circuit Operation

PFC operation has the 3-mode, Continuous Current Mode (CCM), Boundary Current Mode (BCM) and Discontinuous Current Mode (DCM), based on the inductor current waveform as shown in Fig. 3.4. Figure shows a comparative image of the inductor current when the input currents of the three modes are equal. CCM has the lowest peak current and DCM has the highest peak current. Because of this, the CCM which can make peak current low is common when the output power is high, and CCM is also used in this design.

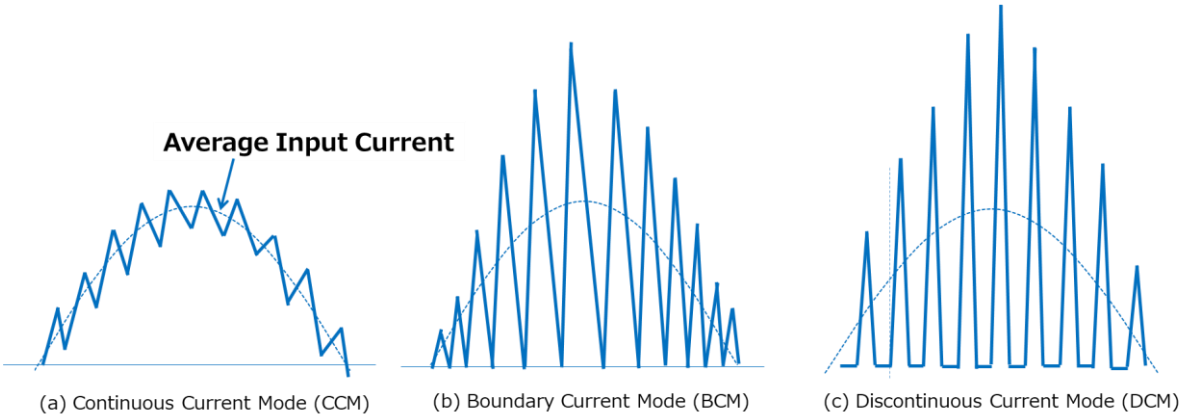


Fig. 3.4 Inductor Current Waveforms

Fig. 3.5 shows the timing of Mode 1 to 4 circuit operation in CCM (Fig. 3.3) and the image of V_{Ain} voltage and current waveforms at that time. In CCM, the on-period of MOSFET is narrowed as the input V_{in} voltage (phase voltage) becomes larger in PWM control.

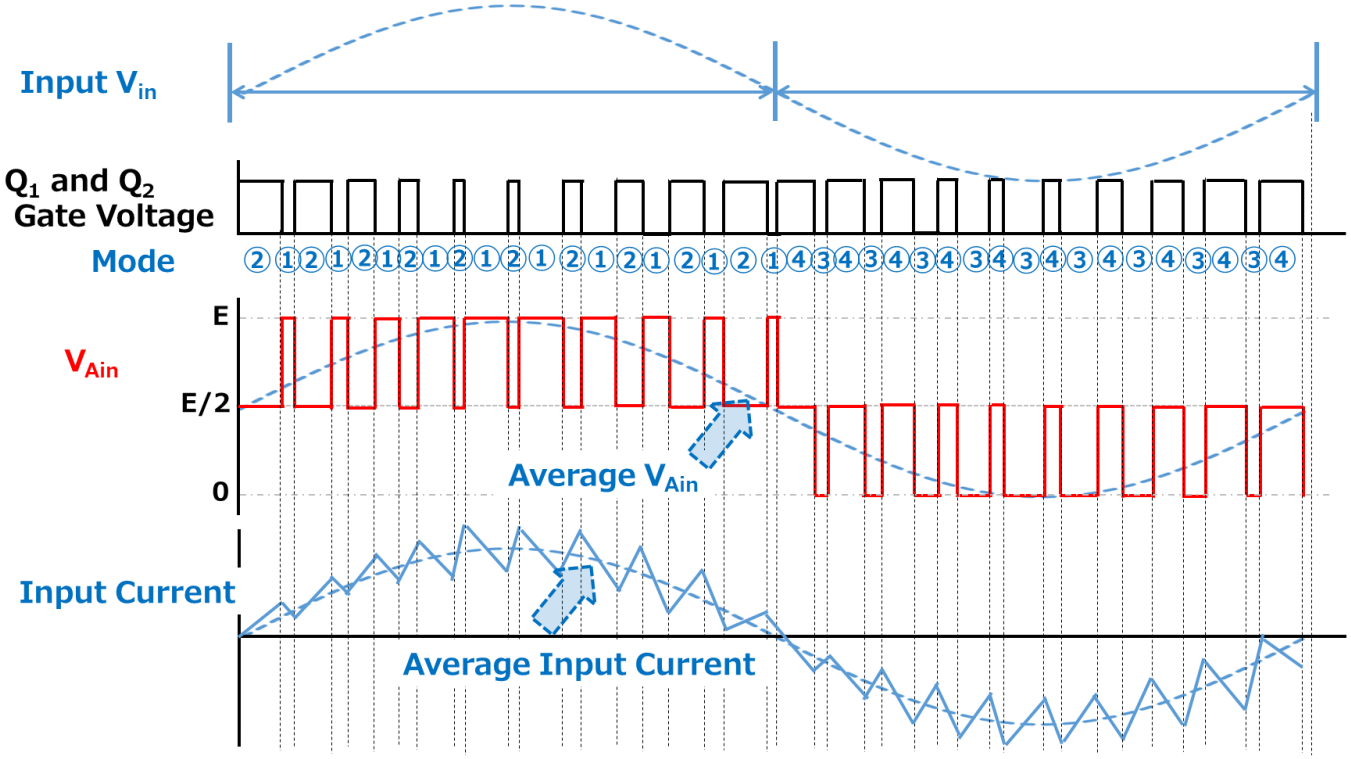


Fig. 3.5 Vienna PFC Circuit Continuous Current Mode Waveform Images

Fig. 3.6 shows MOSFET on/off timing of each phase. Each phase has a phase difference of 120°. The on-period decreases as the phase voltage increases. Because of the reduced harmonic content, it is common to center the pulse waveform. (The two identically colored arrows in the pulse are the same width.)

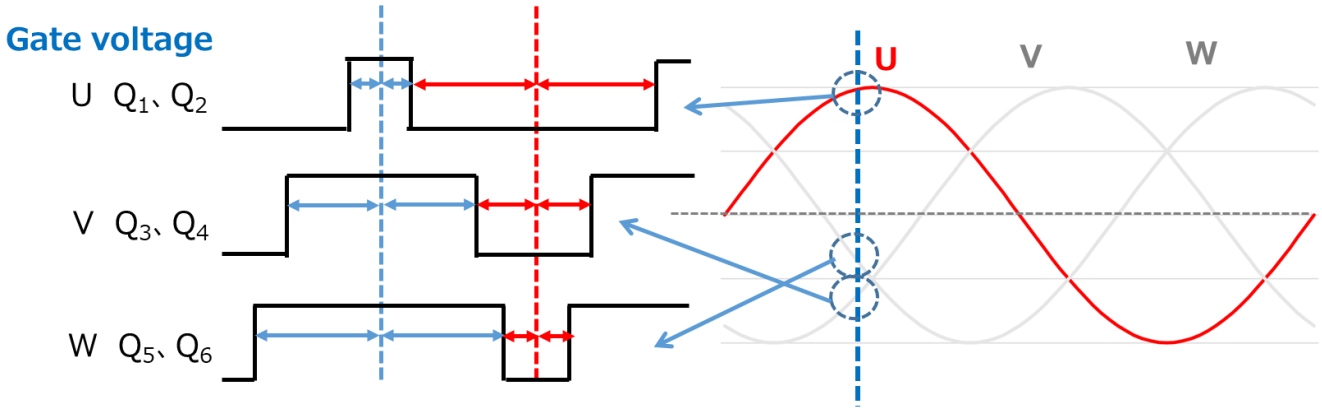


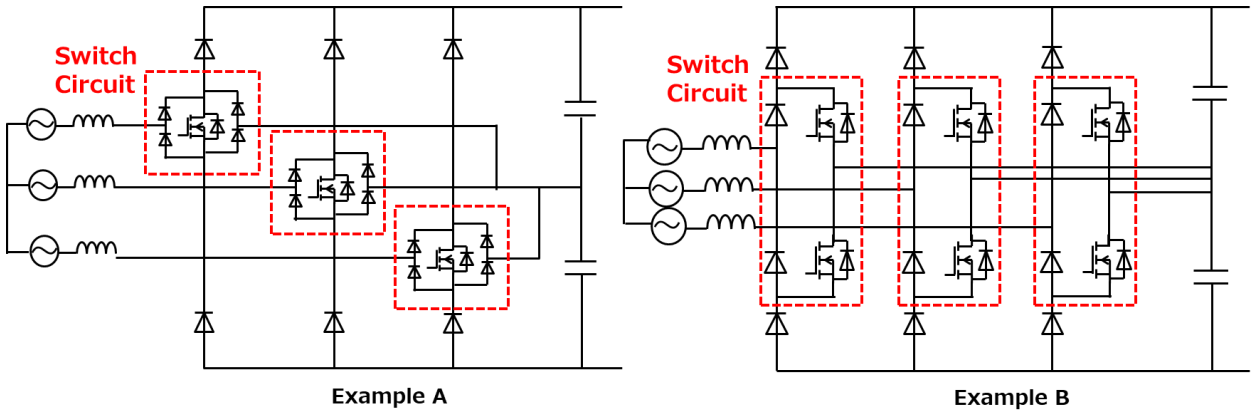
Fig. 3.6 MOSFET On/Off Timing of Each Phase

3.3. Other Vienna Rectifiers

Fig. 3.7 shows examples of other Vienna rectifiers. The concept of basic operation is the same as that shown in Fig. 3.2 and Fig. 3.3, but each circuit has a different switch circuit. Fig. 3.8 shows the operation of each switch circuit.

The switching circuit of the Example A controls the input current by turning on/off the Q regardless of whether the input is positive or negative, and by making the input and the midpoint between output capacitors conductive or non-conductive, PFC operation is performed.

Example B switches on/off Q_a when the input is positive (Q_b off) and Q_b when the input is negative (Q_a off) to control the input current by making the input and the midpoint between output capacitors conductive or non-conductive, PFC operation is performed.



Fog. 3.7 Other Vienna Rectifiers

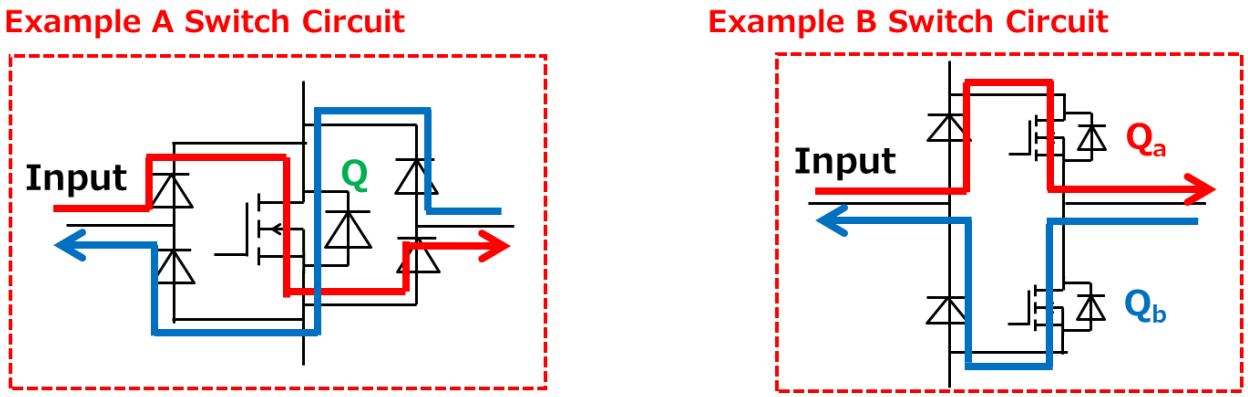


Fig. 3.8 Switching Operation of the Other Vienna Rectifiers

4. 3-Phase AC 400V Input Vienna Rectifier PFC Power Supply

This chapter provides an overview of the configuration of this design and the circuit design of each part. Fig. 4.1 shows the configuration diagram of this design. Fig. 4.2 shows the circuit diagram of the main circuit.

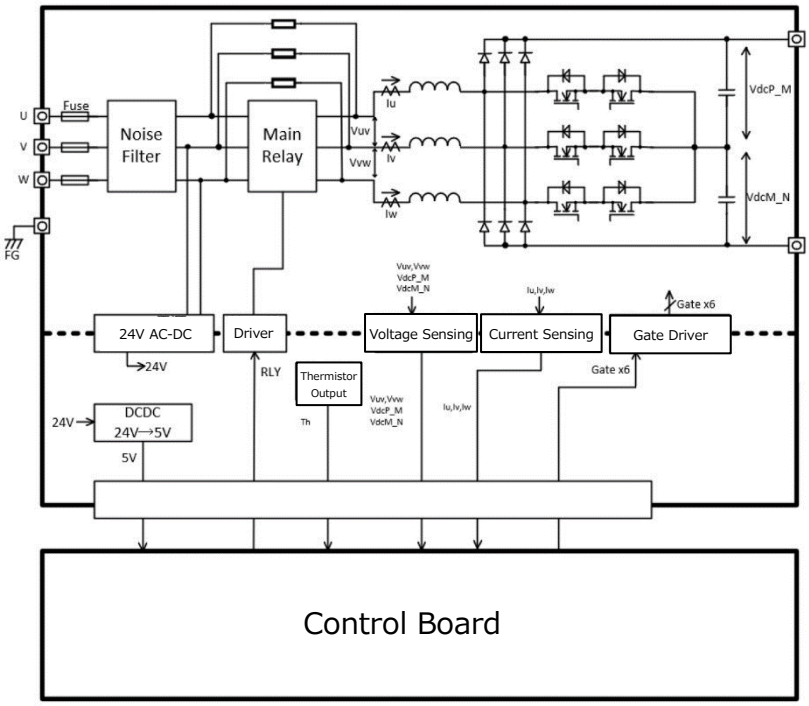


Figure 4.1 Configuration Diagram of This Design

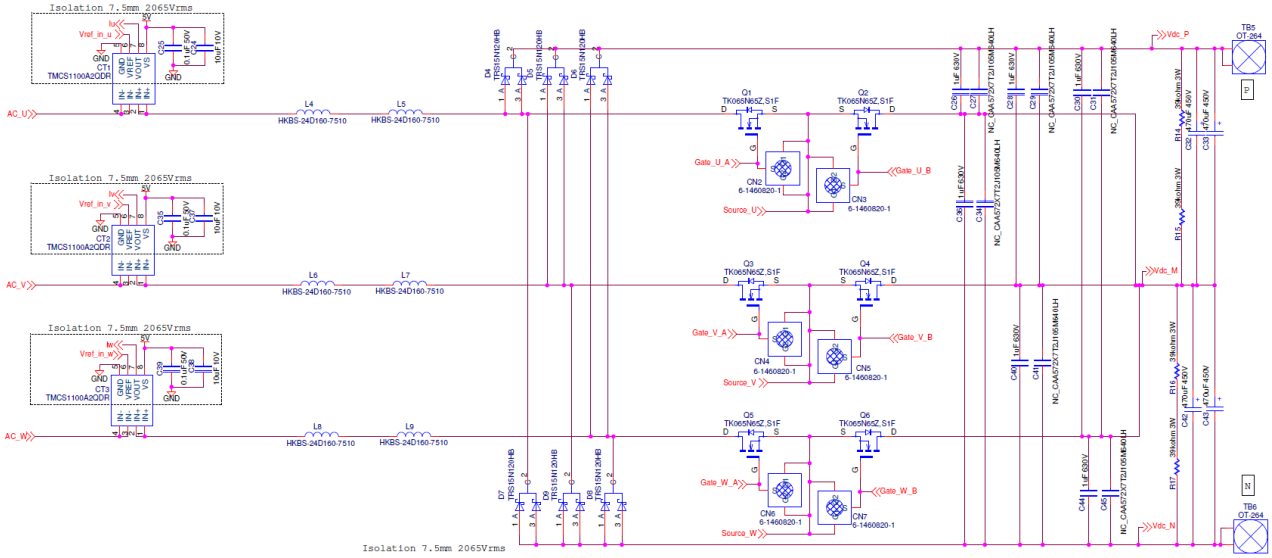


Fig. 4.2 Main Circuit

4.1. Specifications

Table 4.1 lists the main specifications of this design.

Table 4.1 Specifications of This Design

Item	Conditions	Min.	Typ.	Max.	Unit
Input AC voltage (rms)	3-phase AC	360	400	440	V
Input AC current (rms)	3-phase AC			8.2	A
Input frequency	3-phase AC	49.8	50	50.2	Hz
	3-phase AC	59.7	60	60.3	Hz
Output voltage		740	750	760	V
Maximum output power				5	kW
Switching frequency			200		kHz
Protection function	Input overcurrent protection, input overvoltage protection, and output overvoltage protection				
Board layer configuration	FR-4 4 layered configuration, copper foil thickness: 70μm				

Table 4.2 lists the specifications of each protection function.

Table 4.2 Protection Functions

Item	Specifications
Input overcurrent protection	When the detected AC current (phase current) exceeds ±18A, all MOSFETs are turned off.
Input overvoltage protection	When the detected AC voltage (line voltage) exceeds ±653V, all MOSFETs are turned off.
Output overvoltage protection	When the detected DC-side voltage (output-midpoint voltage or GND-midpoint voltage) exceeds 413V, all MOSFET are turned off.

Input overcurrent protection: Set to 18A (8.2 x √2 x 1.55) because of the maximum input AC current 8.2Arms.
Input overvoltage protection: Set to 653V (440 x √2 x 1.05) because of the maximum input AC voltage 440Vrms.
Output overvoltage protection: Set to 413V (750 ÷ 2 x 1.1) because of the rated output voltage 750V.

4.2. Inrush Current Prevention Circuit

This design has an inrush current prevention circuit to prevent inrush current at startup. First, the current is limited by the inrush current prevention resistor, then the relay connected in parallel to the inrush current prevention resistor is turned on, and the current path is switched via the relay. Select an inrush prevention resistor that has a resistance and adequate withstand capacity based on the power dissipation, AC voltage peak value, output capacitor capacitance, and ambient temperature.

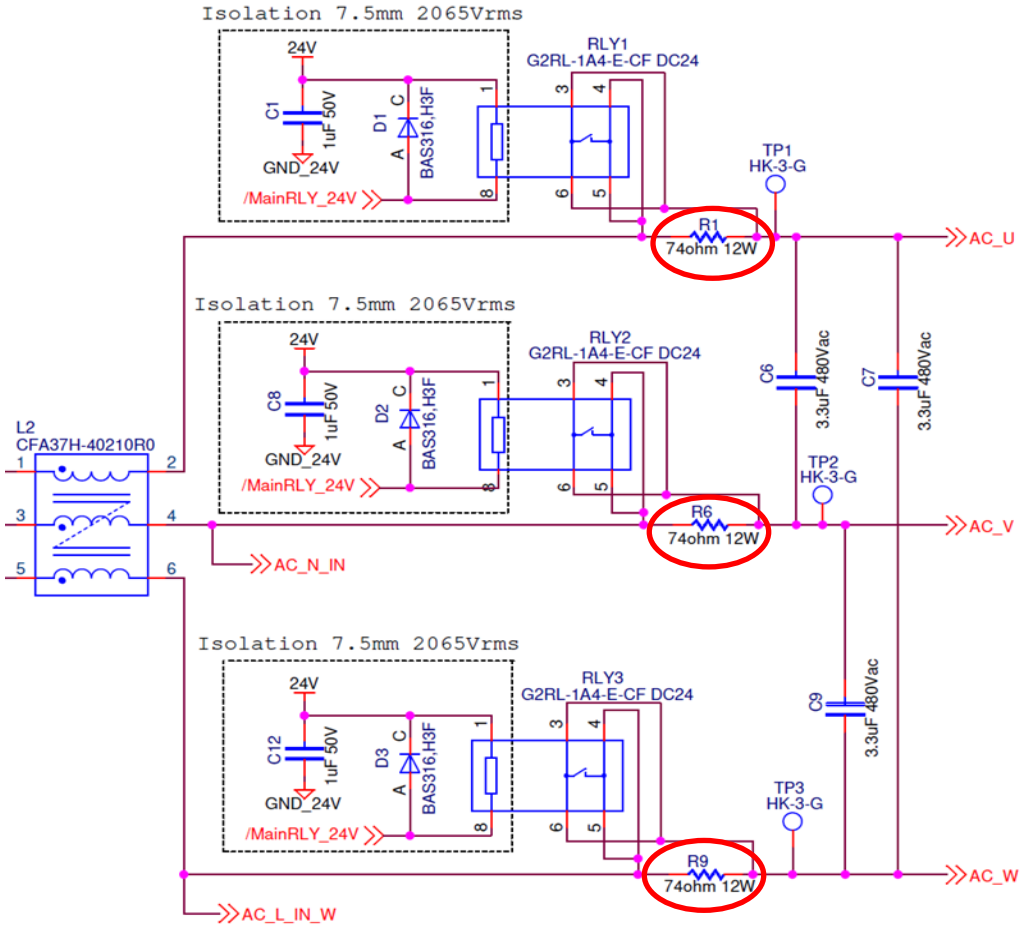


Fig. 4.3 Inrush Current Prevention Circuit

4.3. Fuse

Assuming that the power factor is 100%, the effective value of the input AC current is calculated by the following formula.

Input AC current effective value

= Output power / (power supply efficiency × input AC voltage effective value × √3)

The maximum input AC current is obtained when the output power is maximum, and the input AC voltage is minimum. Assuming that the power supply efficiency is 98%,

5.1kW / (0.98 x 360V x √3) = 8.2A is calculated.

Given the margins in this 8.2A, this design chooses 12A rated fuses.

4.4. Varistor

A varistor is mounted to protect the system from surge voltage when an inductive lightning surge or the like is applied to the AC line. A varistor with maximum allowable circuit voltage 460V and varistor voltage 750V (675V to 825V) is selected considering margins from the AC maximum voltage 440V. The varistor is placed between each line of the AC input circuit, and a current fuse is placed in series in the pre-varistor stage.

4.5. Current Sensing Circuit

The current measuring area is designed to be ±18.5A using a TMCS1100A2QDR (Texas Instruments product (hereafter referred to as the current sensor) with enough margin of the peak-value 11.6A because of the maximum input current 8.2Arms. Fig. 4.4 shows the current sensing circuit. Refer to TMCS1100A2QDR datasheet and related documents for more information on the current sensor.

Apply 2.5V to VREF terminal of the current sensor. Set the output to 2.5V when the current is 0A. Since sensitivity of the current sensor is 100mV/A, the output-voltage of the current sensor when measuring the current ±18.5A is calculated in 2.5V±(100mV/A × 18.5A) and the result is 2.5V±1.85V. The signal is amplified by a differential amplifier (29.4kΩ / 22kΩ) in order to the output-voltage range make 0 to 5V. 2.5V±2.472V(-18.5A to 18.5A) is being applied to the controller's AD converter.

12bit's AD converter is used and its resolution is as follows.

(5V / 4096) × (18.5A / 2.472V) = 9.134mA

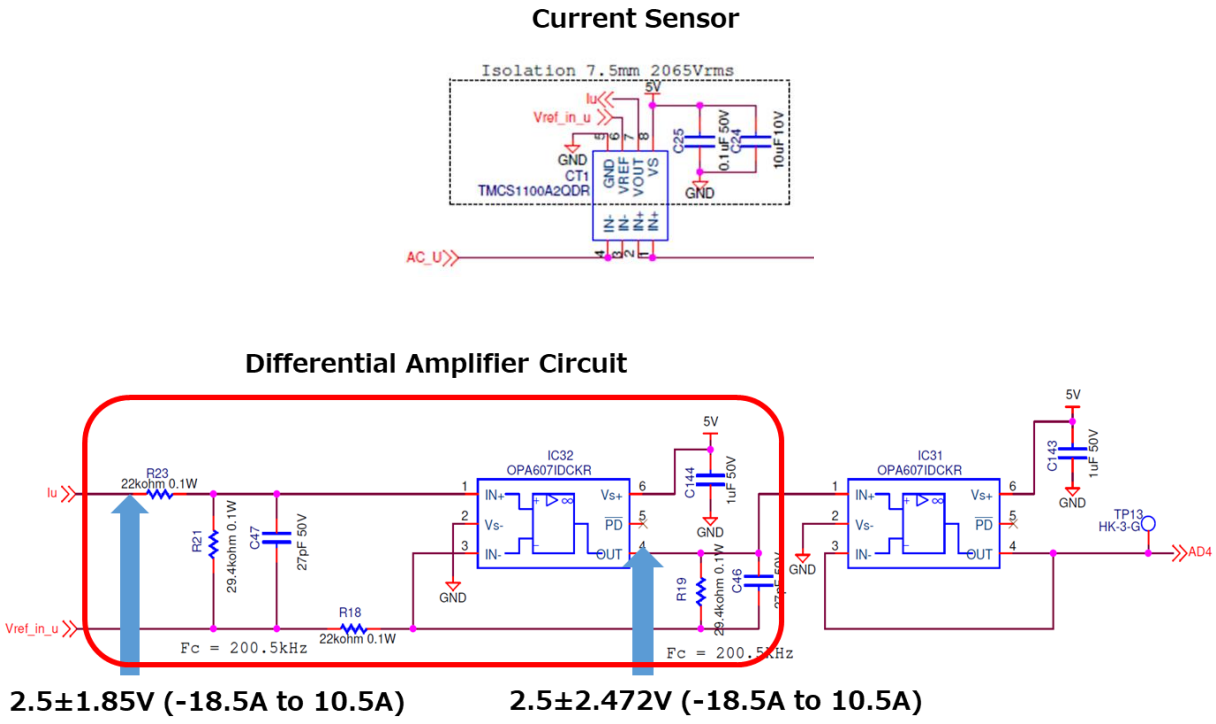


Fig. 4.4 Current Sensing Circuit

4.6. Voltage Sensing Circuit

The input AC voltage and output DC voltage are measured by the circuit shown in Fig. 4.5. Each voltage divided by a voltage dividing circuit is amplified by TLP7920F and the amplifier circuit, and inputted to AD converter of the controller. Set the overall amplification factor so that each voltage is within the range of 0 to 5V. By dividing the detection circuit output voltage 0 to 5V by the total amplification factor, it is possible to know how much V the detection circuit output voltage corresponds to the actual voltage. Table 4.3 shows the amplification factor, measurement range, and resolution of this circuit.

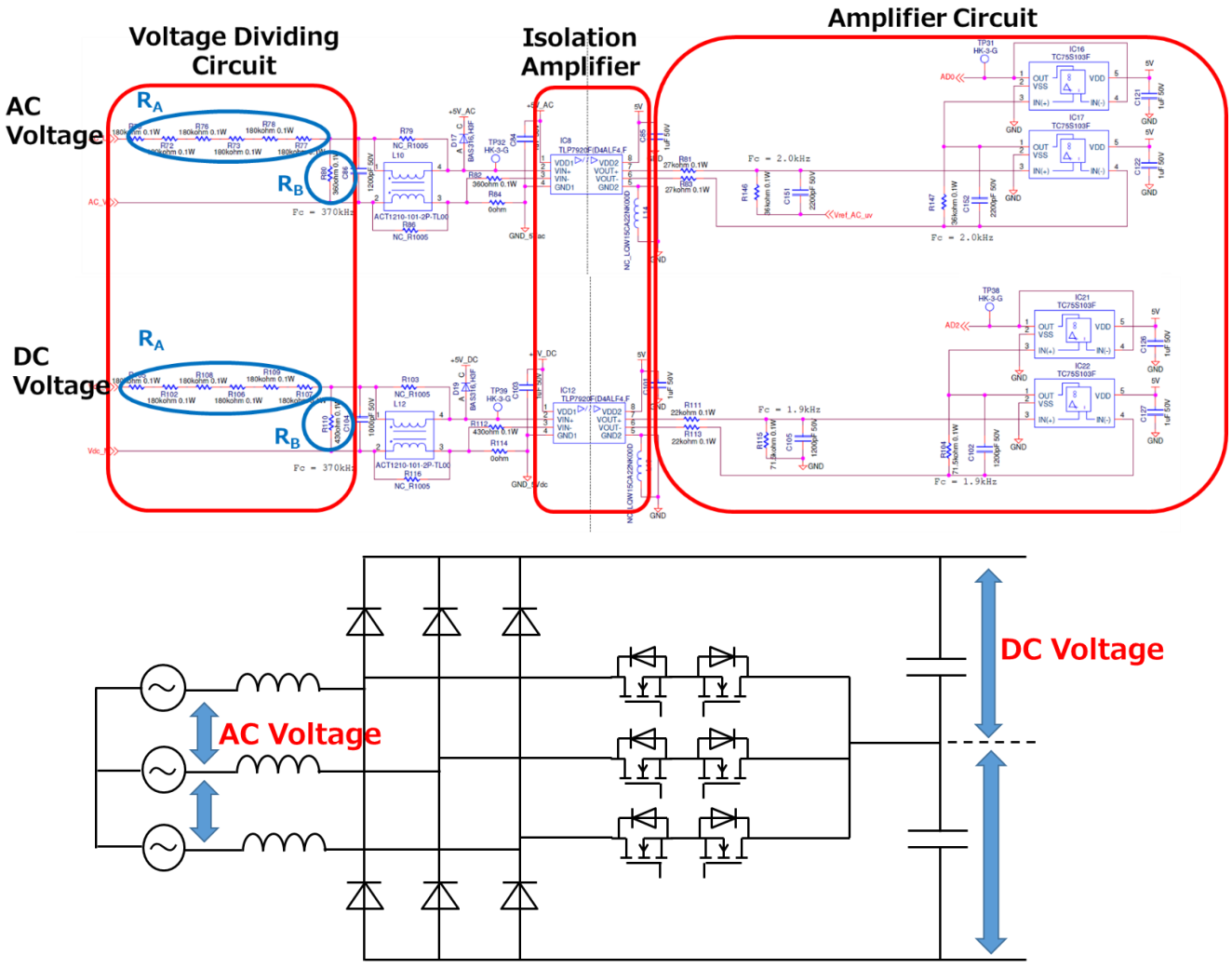


Fig. 4.5 Voltage Sensing Circuit

Table 4.3 Voltage Sensing Circuit Design Values

	(1) Dividing Ratio $R_B/(R_A+R_B)$	(2) Isolation Amplifier Amplification Factor	(3) Amplifier Circuit Amplification Factor	(4) Overall Amplification Factor (1) x (2) x (3)	(5) Measurement Range (V) 5V / (4) (Note 1)	Resolution V/bit (5) / 4096 (Note 2)
AC Voltage	3.33E-04	8.2	1.33	3.64E-03	±686.2	0.335
DC Voltage	3.98E-04	8.2	3.25	1.06E-02	471.4	0.115

Note 1: Input voltage range that output voltage of the sensing circuit becomes 0 to 5V

Note 2: Using 12bit converter, 12bit = 4096

4.7. Temperature Sensing Circuit

Fig. 4.6 shows the temperature sensing circuit. A NTC thermistor is used for the temperature sensing, enabling sensing the temperature of heatsink section where MOSFET is connected. If the resistance value of the thermistor at temperature T_0 (K) is R_0 and the resistance value at temperature T (K) is R, the following equation is established. This indicates that the logarithm of the resistance value of the thermistor and the reciprocal of the absolute temperature have a linear relationship. B is called the B constant of the thermistor, and is a physical property value that indicates the thermistor's sensitivity for temperature change (rate of change in resistance value), and differs for each thermistor.

$$B = \frac{log_e R - log_e R_0}{\frac{1}{T} - \frac{1}{T_0}}$$

From the above equation, the resistance value R of the thermistor at temperature T (K) is expressed by the following equation.

$$R = R_0 \times e^{\left(B\left(\frac{1}{T} - \frac{1}{T_0}\right)\right)}$$

This time, a thermistor with the following characteristics is used.

Resistance valueR_{25} @298K (25℃) :10kΩ±1%

B constant:3435 (K) ±1%

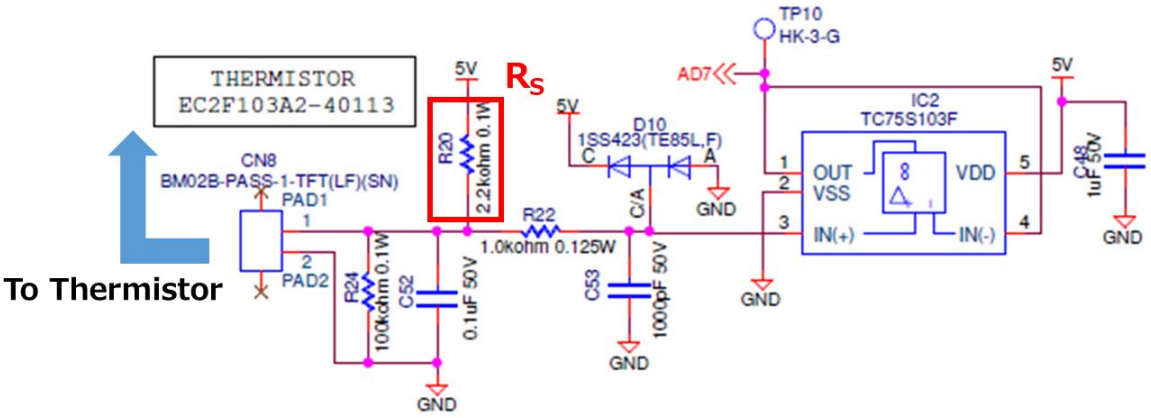


Fig. 4.6 Temperature Sensing Circuit

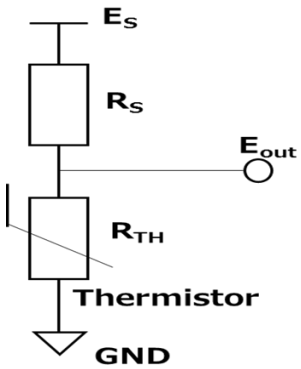


Fig. 4.7 Thermistor Connection Circuit

The circuit shown in Fig. 4.7 is a circuit that uses a thermistor to convert temperature changes into voltage changes. Consider three temperature points (T_1, T_2, T_3) with equal temperature spacing, and set E_{out} voltage as (E_1, E_2, E_3) and R_S so that the temperature and E_{out} are linearly aligned (E_{out} is proportional to the temperature). The relation between E_{out} and temperature is represented by a linear approximation, and the temperature can be sensed by E_{out} voltage.

[R_S Settings]

As a $T_1 < T_2 < T_3$

When $\Delta T_{32} = (T_3-T_2) = \Delta T_{21} = (T_2-T_1)$ is set, consider R_S that will be $(E_2-E_1) = (E_3-E_2)$.

When R_{TH} (thermistor resistor) at T_1, T_2, T_3 is R_1, R_2, R_3, E_{out} (E_1, E_2, E_3 in Fig. 4.6) is expressed by the following equation.

$E_1 = E_S \times R_1 / (R_1+R_S)$

$E_2 = E_S \times R_2 / (R_2+R_S)$

$E_3 = E_S \times R_3 / (R_3+R_S)$

The following equation holds because the difference between the three equal-spaced points in a straight line is the same as that of the detect-voltage E_{out} (E_1, E_2, E_3).

$E_S \times R_1 / (R_1+R_S) - E_S \times R_2 / (R_2+R_S) = E_S \times R_2 / (R_2+R_S) - E_S \times R_3 / (R_3+R_S)$

Solving the above for R_S gives the following equation:

$$R_S = \frac{R_2(R_1 + R_3) - 2R_1R_3}{R_1 + R_3 - 2R_2}$$

Next, calculate R_{30}, R_{60}, and R_{90} of thermistor resistance when T is 30°C, 60°C, and 90℃ (303 K, 333K, and 363K).

Substitute the thermistor resistance value of 10kΩ for T_0 (298K, 25°C) and the thermistor B-constant of 3435 (K) for thethermistor into thetemperature resistance equation to find the thermistor resistance R_{30}, R_{60}, R_{90} when T is 30°C, 60°C, or 90°C.

$$R_{TH} = R_0 \times e^{\left(B\left(\frac{1}{T}-\frac{1}{T_0}\right)\right)}$$

Where T and T_0 are expressed in Kelvin (K).

$R_1 = R_{30}$ = 8.27kΩ (R_{TH}), $R_2 = R_{60}$ at 30°C = 2.98kΩ (R_{TH}), $R_3 = R_{90}$ at 60°C = 1.27kΩ (R_{TH} at 90°C)), and substituting these values into R_S equation

$$R_S = \frac{2.98(8.27 + 1.27) - 2 \times 8.27 \times 1.27}{8.27 + 1.27 - 2 \times 2.98}$$

R_S is calculated as 2.1kΩ. In this design, R20 = 2.2 Ω is selected.

In addition, E_{out} is expressed by the following equation.

$$E_{out} = E_s \times \frac{R_{TH}}{R_s + R_{TH}}$$

$$= E_s \times \frac{1}{\frac{R_s}{R_{TH}} + 1}$$

The thermistor resistance R_{TH} is obtained from the theoretical formula of the thermistor resistance value, and an approximate formula for the following temperature T and E_{out} can be derived by substituting the above formula for the thermistor resistance R_{TH} at various temperatures.

$$E_{out} = -0.035T + 4.99$$

4.8. Gate Drive Circuit

Fig. 4.8 shows the gate drive circuit of the U-phase MOSFET (Q_1, Q_2) in Fig. 4.2. The gate drive voltage is 10V, and gate resistance value can be changed separately for turn-on and turn-off. Taking Q_1 gate-drive as an example, the turn-on resistor is R36, and the turn-off resistance is the parallel resistance between R34 and R36. The same configuration applies to the other phases.

A 10V is generated by the gate drive power supply shown in Fig. 4.9 and applied to the gate when it is on.

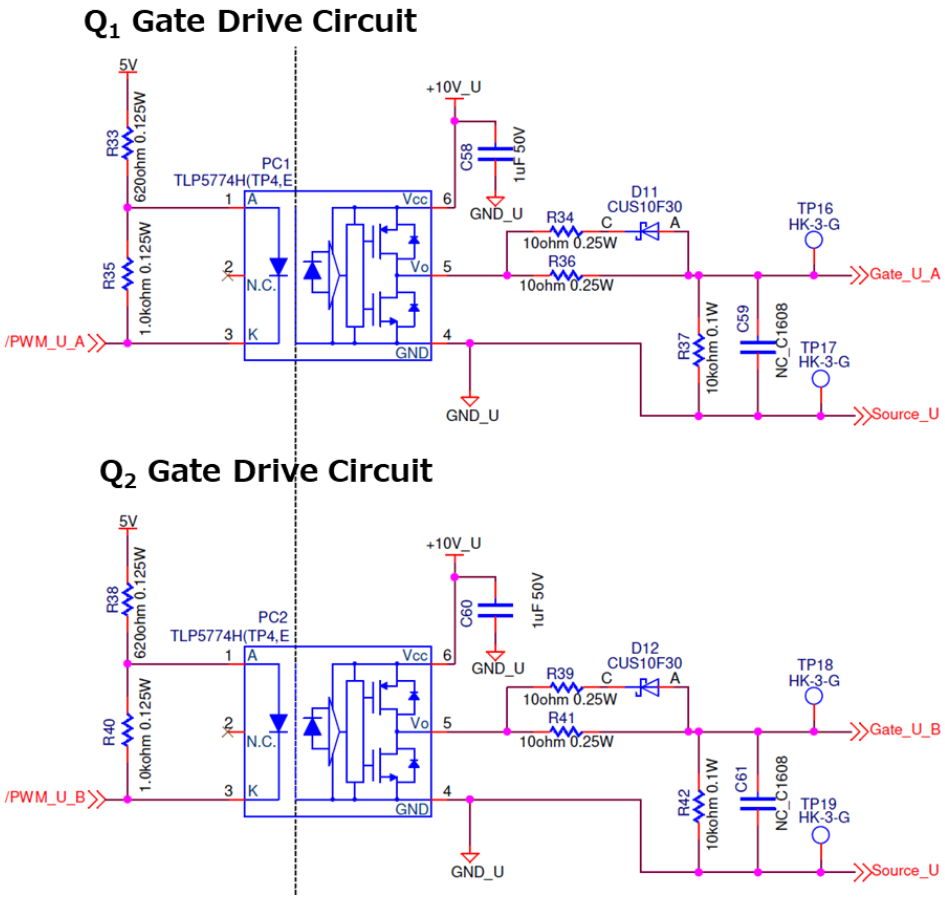


Fig. 4.8 Gate Drive Circuit

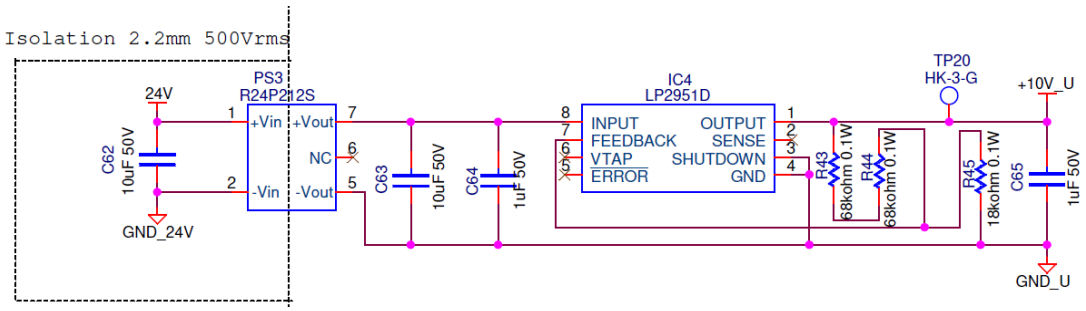


Fig. 4.9 Gate Drive Power Supply Circuit

4.9. Inductors

The inductance value of the inductor (L4 to L9) of this design was examined by calculating the ripple current by simulation. Table 4.4 shows the simulation results when the inductance value is 750μH. This indicates that an inductance of at least 750μH is required to achieve a ripple rate (P-P) of less than 30%. Considering the current superposition characteristics of the actual inductor, it is necessary to select an inductor such that the inductance value becomes 750μH or more at the input current value. This design uses two inductors rated at 750μH in series with considering some margin.

Table 4.4 Results of Inductor Examination

Output DC Voltage	V_{out}	750			V
Output Power	P_{out}	5000			W
Output DC Current	I_{out}	6.667			A
Input AC Line Voltage	V_{in}	360	400	440	V
Efficiency (Target Value)	η	0.98			-
Input AC Power	P_{in}	5102			W
Input AC Current	I_{in}	8.2	7.4	6.7	A
Ripple Ratio	M	0.3	0.3	0.3	-
Ripple Current (P-P)	I_{ripple}	2.455	2.209	2.008	A
Switching Frequency	f_{sw}	50			kHz

4.10. Output capacitor

The capacitance of the output capacitor (C_{32}, C_{33}, C_{42}, C_{43}) in the circuit shown in Fig. 4.2 is calculated based on the hold-up time (T_{hold})※ requirement. If the output capacitor is C_{out}, the output voltage is V_{out}, the required minimum output voltage is V_{out_min} after the input is shut down, and the output power set after the input is shut down P_{out}, then the energy emitted from the output capacitor when the output voltage drops from V_{out} to V_{out_min} is equal to the energy of P_{out} between the hold-up time T_{hold}, and the following equation is established.

$$\frac{1}{2}C_{out}{V_{out}}^2-\frac{1}{2}C_{out}{V_{out\_min}}^2=P_{out}\times T_{hold}$$

From this expression, T_{hold} is calculated as follows:

$$T_{hold}=C_{out}\times\frac{({V_{out}}^2-{V_{out\_min}}^2)}{2\times P_{out}}$$

In this design, V_{out_min} was designed with a 563V, 75% of V_{out} (750V), Pout of with a 2.5kW, 50% of rated power, Thold of with a 20ms, one cycle of 50Hz AC, and Cout was calculated to be 407μF, and 470μF was selected.

In addition, when the output ripple specification is defined, the capacity required to satisfy the output ripple specification must be calculated and compared with the capacity satisfying the hold-up time, and a larger capacity value must be used. Tolerances and aging must also be considered when selecting capacitors.

※:Hold-up time (T_{hold})

Time from when the input power is cut off until the output voltage goes out of the set range

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