

TW092V65C

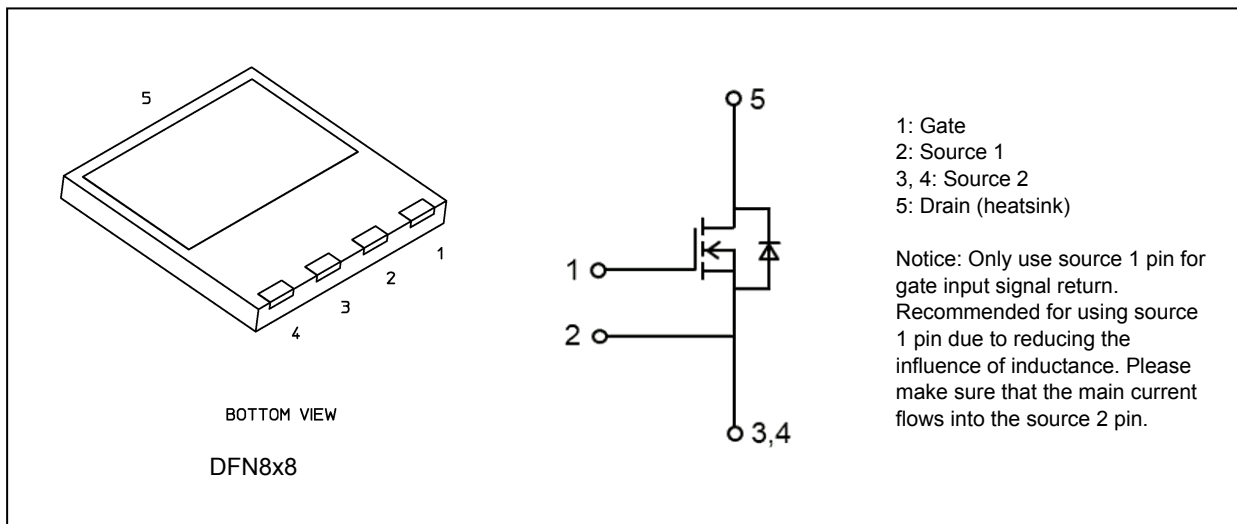
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Chip design of 3rd generation (Built-in SiC schottky barrier diode)
- (2) Low diode forward voltage: $V_{DSF} = -1.35 \text{ V}$ (typ.)
- (3) High voltage: $V_{DSS} = 650 \text{ V}$
- (4) Low drain-source on-resistance: $R_{DS(ON)} = 92 \text{ m}\Omega$ (typ.)
- (5) Less susceptible to malfunction due to high threshold voltage: $V_{th} = 3.0 \text{ to } 5.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 0.6 \text{ mA}$)
- (6) Recommended gate - source drive voltage: $V_{GS_{on}} = 18 \text{ V}$, $V_{GS_{off}} = 0 \text{ V}$
- (7) Enhancement mode.

3. Packaging and Internal Circuit



Start of commercial production
2025-02

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	+25/-10	
Drain current (DC) ($T_c = 25\text{ }^\circ\text{C}$) (Note 1)	I_D	27	A
Drain current (DC) ($T_c = 100\text{ }^\circ\text{C}$) (Note 1)	I_D	19	
Drain current (pulsed) ($T_c = 25\text{ }^\circ\text{C}$) (Note 1)	I_{DP}	64	
Drain current (pulsed) ($T_c = 100\text{ }^\circ\text{C}$) (Note 1)	I_{DP}	50	
Power dissipation ($T_c = 25\text{ }^\circ\text{C}$)	P_D	111	W
Channel temperature	T_{ch}	175	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	1.350	$^\circ\text{C}/\text{W}$

Note 1: Ensure that the channel temperature does not exceed $175\text{ }^\circ\text{C}$.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care. It should be used for switching applications.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = +25/-10\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 0.1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	—	3.0	37	
		$T_a = 150\text{ }^\circ\text{C},$ $V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	—	14	—	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 4\text{ mA}, V_{GS} = 0\text{ V}$	650	—	—	V
Gate threshold voltage (Note 2)	V_{th}	$V_{DS} = 10\text{ V}, I_D = 0.6\text{ mA}$	3.0	—	5.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 18\text{ V}, I_D = 15\text{ A}$	—	92	136	$\text{m}\Omega$
		$T_a = 150\text{ }^\circ\text{C},$ $V_{GS} = 18\text{ V}, I_D = 15\text{ A}$	—	100	—	

Note 2: Please be sure to apply I_{GSS} ($V_{GS} = 25\text{ V}$) before the V_{th} test.

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 100\text{ kHz}$	—	873	—	pF
Reverse transfer capacitance	C_{rss}		—	3.4	—	
Output capacitance	C_{oss}		—	110	—	
Effective output capacitance (energy related)	$C_{o(er)}$		—	125	—	
Effective output capacitance (time related)	$C_{o(tr)}$		—	180	—	
Output charge	Q_{oss}		—	72	—	
C_{oss} stored energy	E_{oss}	—	10	—	μJ	
Gate resistance	r_g	$V_{DS} = \text{OPEN}, f = 1\text{ MHz}$	—	4.4	—	Ω
Turn-on delay time	$t_{d(on)}$	See Fig. 6.2.1	—	21	—	ns
Switching time (rise time)	t_r		—	14	—	
Turn-off delay time	$t_{d(off)}$		—	28	—	
Switching time (fall time)	t_f		—	14	—	
Turn-on switching loss	E_{on}		—	98	—	
Turn-off switching loss	E_{off}	—	38	—	μJ	

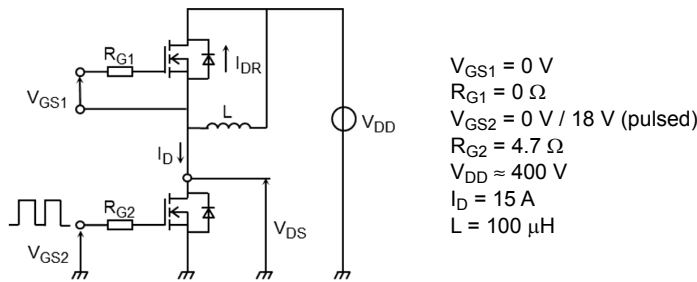


Fig. 6.2.1 Switching Time Test Circuit

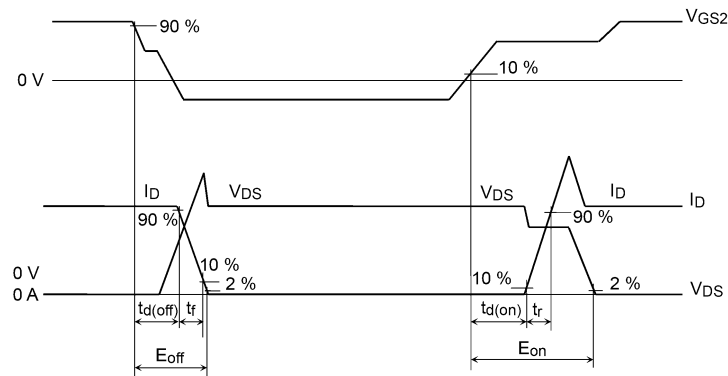


Fig. 6.2.2 Timing Diagrams

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400\text{ V}$, $V_{GS} = 18\text{ V}$, $I_D = 15\text{ A}$	—	28	—	nC
Gate-source charge 1	Q_{gs1}		—	14	—	
Gate-drain charge	Q_{gd}		—	3.9	—	

6.4. Source · Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC) (Note 3)	I_{DR}	$T_c = 25\text{ }^\circ\text{C}$, $V_{GS} = -5\text{ V}$	—	—	26	A
		$T_c = 100\text{ }^\circ\text{C}$, $V_{GS} = -5\text{ V}$	—	—	17	
		$T_c = 25\text{ }^\circ\text{C}$, $V_{GS} = 18\text{ V}$	—	—	27	
		$T_c = 100\text{ }^\circ\text{C}$, $V_{GS} = 18\text{ V}$	—	—	19	
Reverse drain current (pulsed) (Note 3)	I_{DRP}	$T_c = 25\text{ }^\circ\text{C}$, $V_{GS} = -5\text{ V}$	—	—	64	
		$T_c = 100\text{ }^\circ\text{C}$, $V_{GS} = -5\text{ V}$	—	—	29	
		$T_c = 25\text{ }^\circ\text{C}$, $V_{GS} = 18\text{ V}$	—	—	64	
		$T_c = 100\text{ }^\circ\text{C}$, $V_{GS} = 18\text{ V}$	—	—	50	
Diode forward voltage	V_{DSF}	$I_{DR} = 8\text{ A}$, $V_{GS} = -5\text{ V}$	—	-1.35	-1.80	V
		$T_a = 150\text{ }^\circ\text{C}$, $I_{DR} = 8\text{ A}$, $V_{GS} = -5\text{ V}$	—	-1.57	—	
Reverse recovery time	t_{rr}	$I_{DR} = 10\text{ A}$, $V_{GS} = 0\text{ V}$, $V_{DD} = 400\text{ V}$, $-dI_{DR}/dt = 1000\text{ A}/\mu\text{s}$	—	45	—	ns
Reverse recovery charge	Q_{rr}		—	189	—	nC
Peak reverse recovery current	I_{rr}	$I_{DR} = 10\text{ A}$, $V_{GS} = 0\text{ V}$, $V_{DD} = 400\text{ V}$, $-dI_{DR}/dt = 1000\text{ A}/\mu\text{s}$	—	8.4	—	A

Note 3: Ensure that the channel temperature does not exceed $175\text{ }^\circ\text{C}$.

7. Marking

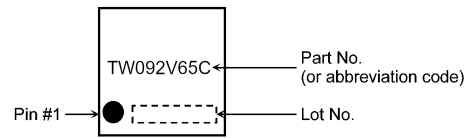


Fig. 7.1 Marking

8. Characteristics Curves (Note)

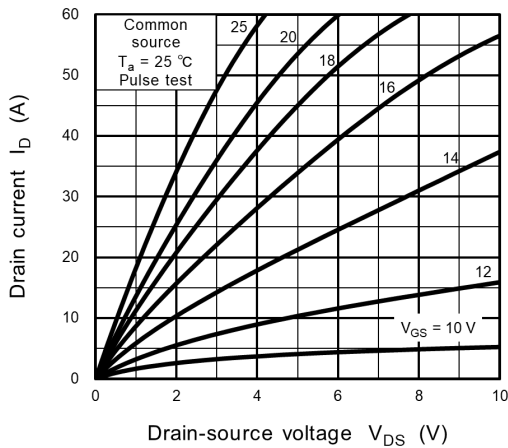


Fig. 8.1 $I_D - V_{DS}$

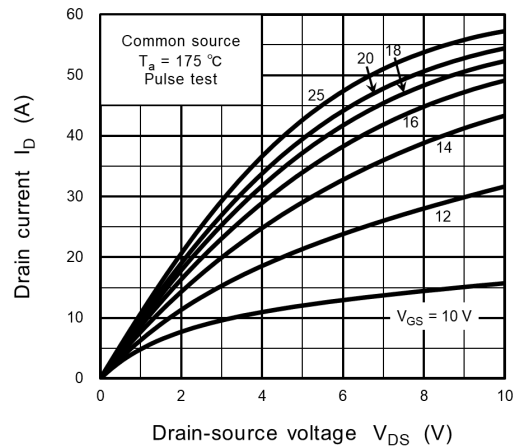


Fig. 8.2 $I_D - V_{DS}$

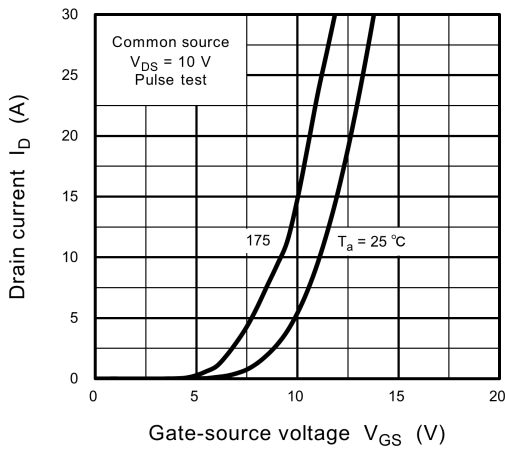


Fig. 8.3 $I_D - V_{GS}$

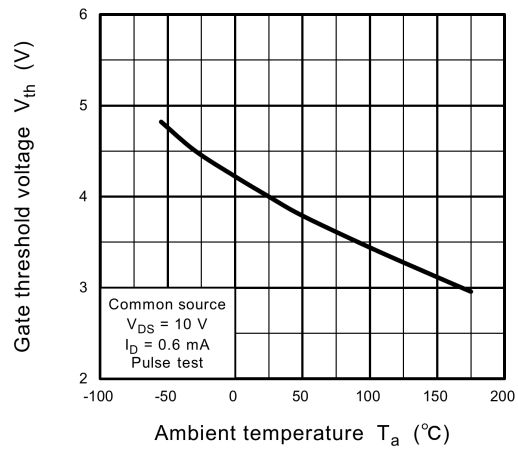


Fig. 8.4 $V_{th} - T_a$

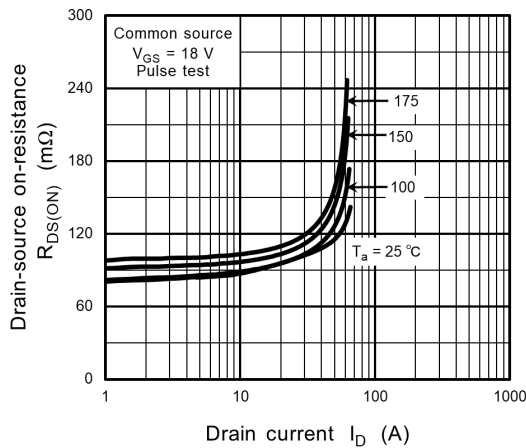


Fig. 8.5 $R_{DS(ON)} - I_D$

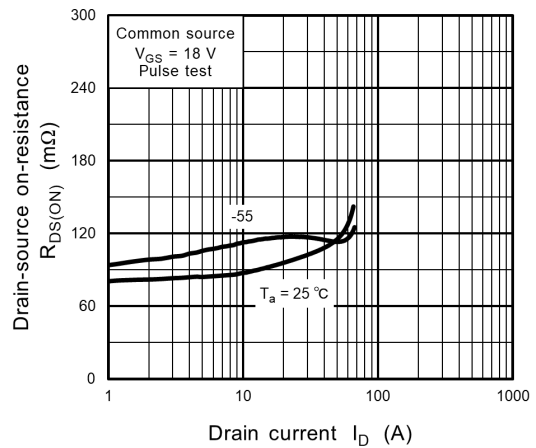


Fig. 8.6 $R_{DS(ON)} - I_D$

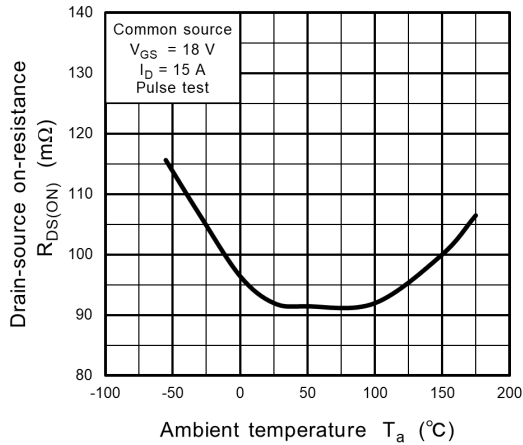


Fig. 8.7 $R_{DS(ON)} - T_a$

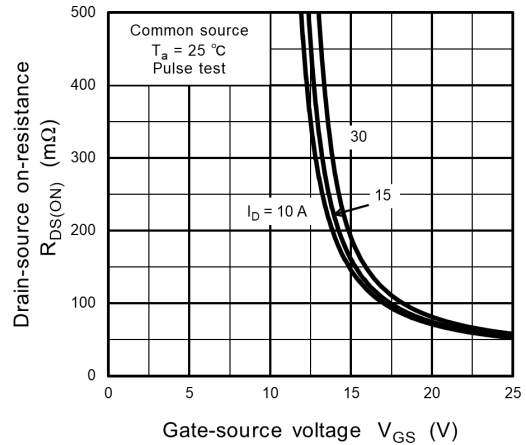


Fig. 8.8 $R_{DS(ON)} - V_{GS}$

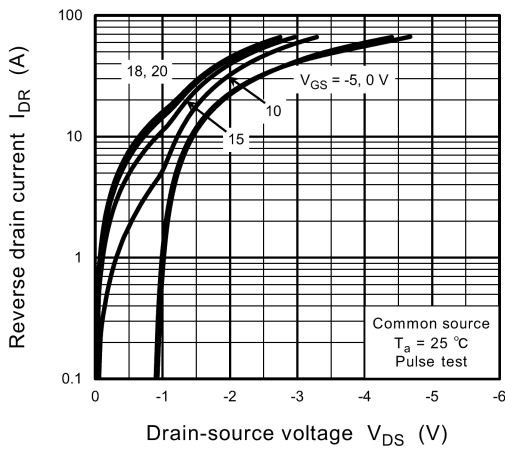


Fig. 8.9 $I_{DR} - V_{DS}$

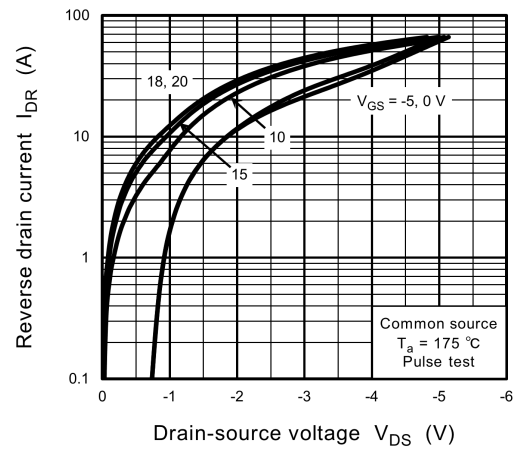


Fig. 8.10 $I_{DR} - V_{DS}$

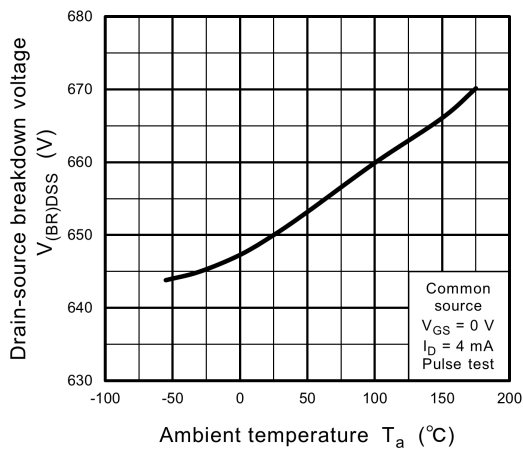


Fig. 8.11 $V_{(BR)DSS} - T_a$

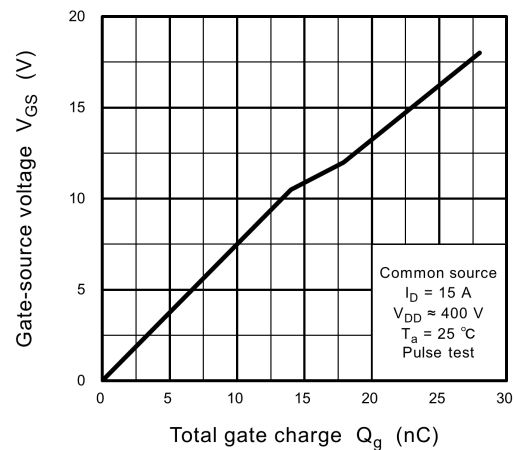


Fig. 8.12 Dynamic Input Characteristics

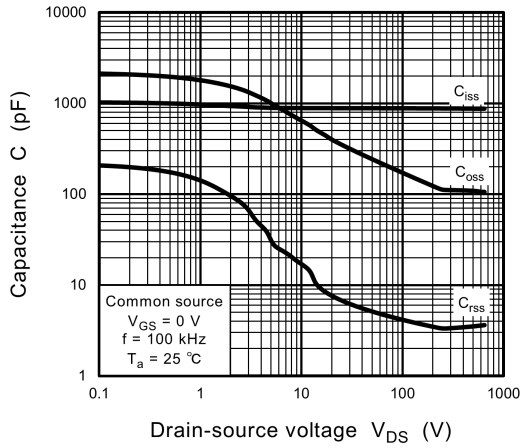


Fig. 8.13 C - V_{DS}

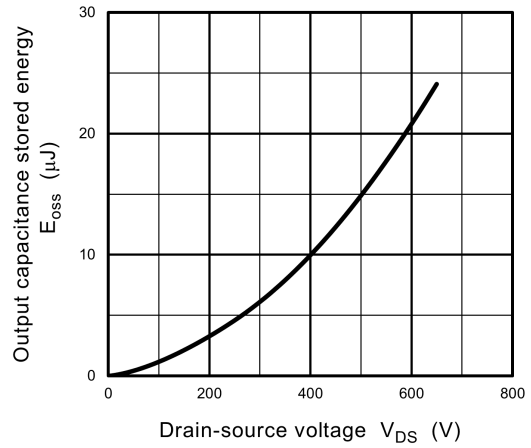


Fig. 8.14 E_{oss} - V_{DS}

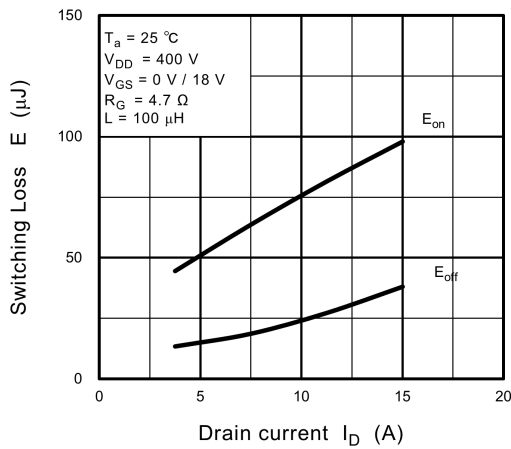


Fig. 8.15 E - I_D

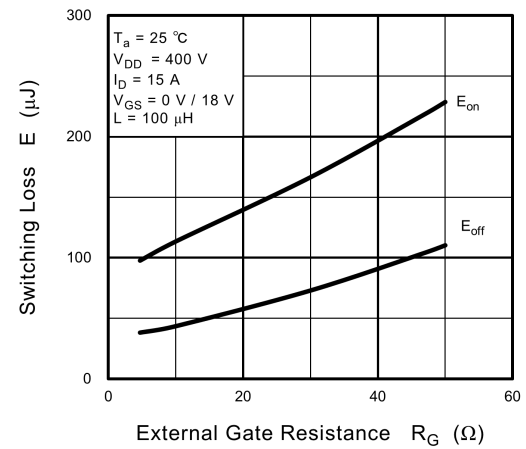
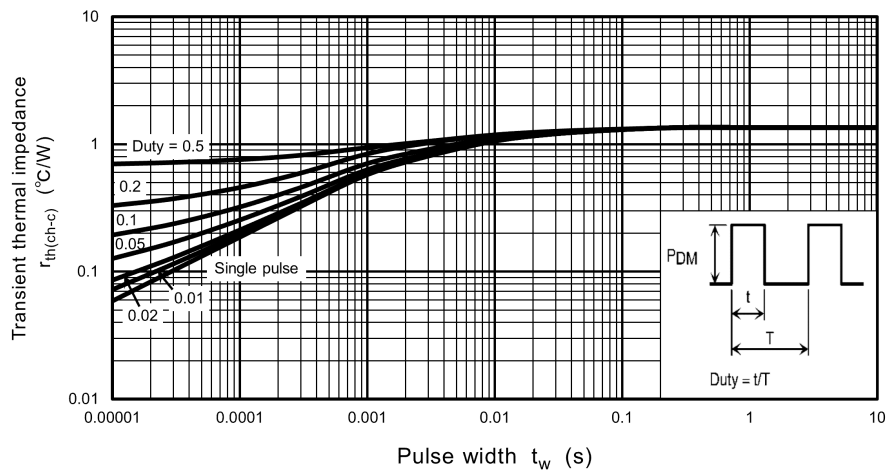


Fig. 8.16 E - R_G



**Fig. 8.17 $r_{th(ch-c)} - t_w$
(Guaranteed Maximum)**

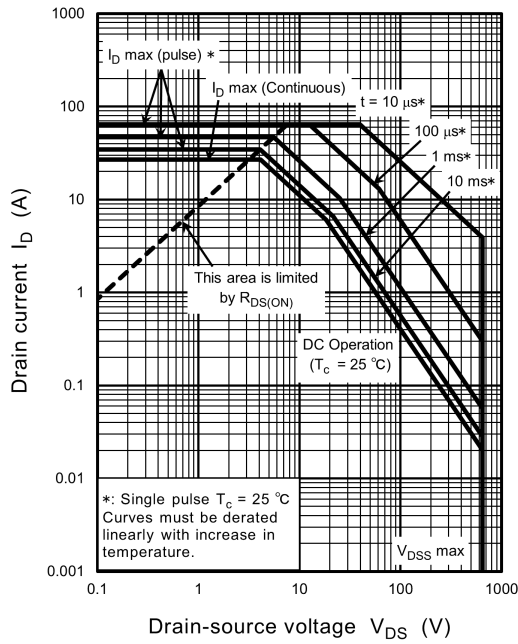


Fig. 8.18 Safe Operating Area (Guaranteed Maximum)

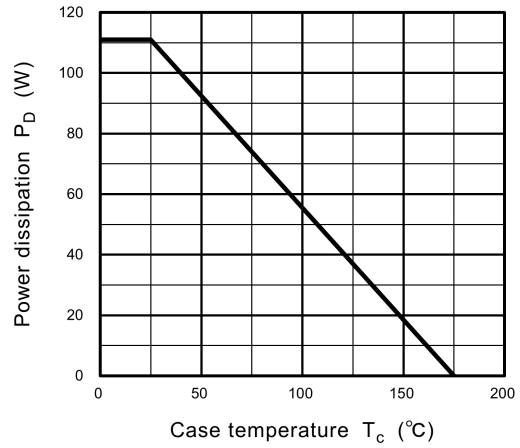


Fig. 8.19 $P_D - T_c$ (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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