Standard digital Isolators

DCM321C00

Dual - channel High speed Logic for Automotive equipment, Default Low output

1. Description

The DCM321C00 is a 8-pin SOIC package default Lowoutput, quad-channel high-speed digital isolator with the primary and secondary sides insulated and coupled by a magnetic coupling structure.

With a high isolation voltage of 3000 V_{rms}, it is suitable for control applications such as in-vehicle communication line insulation.

2. Applications

- Battery Control in Automotive Equipment •
- Fuel Battery Control in Automotive Equipment
- **Application for Electrical Vehicle**
- **Date Converter Isolation**

3. Features

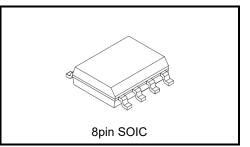
- Data rate 50 Mbps (Max) •
- Default Output •
- Number of channels • Suitable operating voltage •
- 3.3 V or 5 V
- Isolation voltage •
- Common-Mode Transient Immunity : ±100 kV/µs (Typ.) •
- Safetv standards
 - AEC-Q100 (Grade1 qualified)
 - UL : UL1577, File No. E519997
 - cUL: CSA Component Acceptance Service Notice No. E519997

Note: Typical test conditions: $V_{DD1} = V_{DD2} = 3.3V$ or 5V, $T_a = 25$ °C; unless otherwise specified.

4. Mechanical Parameters

Characteristics	Symbol	unit	Unit
Creepage distances	CPG	3.8 (Min)	mm
Clearance distances	CLR	4 (Min)	mm
Distance Through the Insulation	DTI	17	μm

Table 4.1 Mechanical parameters



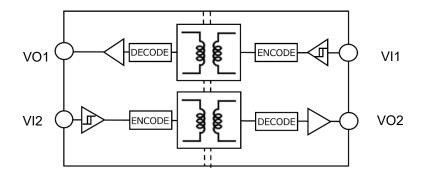
Weight: 0.07 g (typ.)

Low

- 2 channels (Forward 1: Reverse 1)
- 3000 V_{rms}

5. Block Diagram

DCM321C00



Note: Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.



6. Pin Assignments

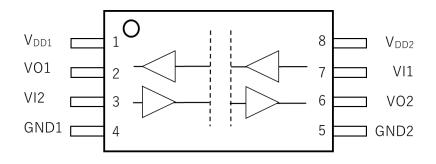


Figure 6.1 Pin Assignments (top view)

7. Pin Description

Pin No	Pin name	I/O	Description
1	V _{DD1}		Power Supply, side 1
2	VO1	OUT	Logic Output, Channel1
3	VI2	IN	Logic Input, Channel2
4	GND1	—	GND connection for VDD1, side 1
5	GND2	—	GND connection for VDD2, side 2
6	VO2	OUT	Logic Output, Channel2
7	VI1	IN	Logic Input, Channel1
8	V _{DD2}		Power Supply, side 2

Table 7.1 Pin Description

8. Functional Description

8.1. Specifications of External Components

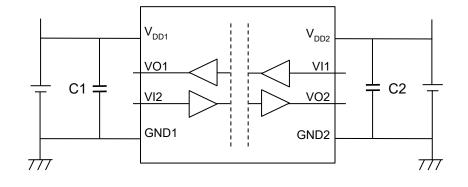


Figure 8.1 Pin Assignments (top view)

Table 8.1	External comp	ponent s	pecification	Note)	

Component Name	Recommended Value	Pin	Description
C1	0.1 µF	V_{DD1}	—
C2	0.1 µF	V _{DD2}	_

Note: Use Ceramic capacitors (C1,C2) with good high frequency characteristics.

Note: Ceramic capacitors (C1,C2) should be connected between pin 1 (V_{DD1}) and pin 2 (GND1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND2) for V_{DD2}, and should be the layout on the IC as close as possible (less than 10mm). Otherwise, the IC may not switch properly.

8.2. IC Startup Procedure

8.2.1. Functional description

	V _{DDI} Input side V _{DD}	V _{DDO} Output side V _{DD}	Input (VI1,VI2)	Output (VO1 , VO2)	State Description
1	PU	PU	Low	Low	Normal Operation
2	PU	PU	High	High	Normal Operation
3	PU	PU	OPEN	Low	Default mode
4	PD	PU	Low or OPEN	Low	Default mode
5	PU	PD	Undetermined	Undetermined	When V _{DD2} is
6	PD	PD	Low or OPEN	Underennined	unpowered, a channel output is undetermined

Table 8.2 Pin Functional Description (Note)

Note: PU = Powered Up ($V_{DD} \ge 2.25 \text{ V}$), PD = Powered Down ($V_{DD} \le 1.7 \text{ V}$) Note: V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}

9. Absolute Maximum Ratings (Note)

(T _a = 25°C unless otherwise specifie							
Characteristics	Condition	Symbol	Rating	Unit			
Junction temperature		TJ	-40 to 150	°C			
Storage temperature range	_	T _{stg}	-65 to 150	°C			
Operation temperature range		T _{opr}	-40 to 125	°C			
Soldering temperature	10 s	T _{sol}	260	°C			
Supply voltage (DC)	_	Vdd1,Vdd2	-0.5 to 6.0	V			
		VI1,VI2	-0.5 to V _{DDI} + 0.5 (Note 1)	V			
		VO1,VO2	0.5 to V _{DDO} + 0.5 (Note 1)	V			
Output Current	_	lo	±15	mA			
Isolation voltage	1min	BVs	3000	Vrms			
Output current	V _{DD1} = V _{DD2} = 5.5 V, Tj = 150 °C, Ta = 25 °C	I _{S1}	255	mA			
	V _{DD1} = V _{DD2} = 3.6 V, Tj = 150 °C, Ta = 25 °C	I _{S2}	390	mA			
Power dissipation	Tj = 150 °C, Ta = 25 °C	P _{d Max}	1403	mW			

Table 9.1 Absolute Maximum Ratings (Note)

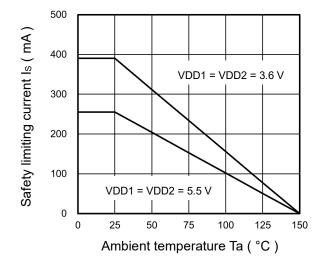
Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered, and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Note 1: Maximum voltage must not exceed 6V.

9.1. Power Dissipation





10. Recommended operating conditions

Characteristics	Symbol	Min	Max	Unit
Operation voltage	V_{DD1} , V_{DD2}	3.0	5.5	V
Junction temperature	TJ	-40	150	°C
Operating temperature	T _{opr}	-40	125	°C

 Table 10.1
 Recommended Operating Ranges (Note)

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

11. Electrical Characteristics

11.1. DC characteristics – 5V Supply

Table 11.1 DC characteristics – 5V Supply (Note)

(1/22) = 1/222 = 4 E 1/42 E E 1/2000	recommended energing	aanditiana unlaaa	athomy ice noted)
(VDD1 = VDD2 =4.5 V to 5.5 V over	recommended operating (conditions unless	otherwise noted)

Characteristics	Symbol	Test condition	Min	Тур.	Max	Unit
Vpp Under Voltage	$VDD_{xUV^{+}}$	Positive VDDx Threshold	—	2.1	2.25	
Lockout threshold	VDD _{xUV-}	Negative VDDx Threshold	1.7	1.9	—	V
VDD Under Voltage Lockout thresholdVD VOL VDVoltageVDLogic High-level output voltageVDLogic Low-level output voltageVDOutput ImpedanceVDLogic High-level input Threshold voltageVDLogic Low-level input Threshold voltageVDLogic Low-level input Threshold voltageVDLogic Low-level input Threshold voltageVDLogic Low-level input Threshold voltageVDLogic Input threshold voltage hysteresisVD	VDD _{xUVH}	VDDx Hysteresis	0.1	0.2	—	
Logic High-level	V _{он}	V_{Ix} = H , I_{OH} = -20 μ A	V _{DDO} - 0.1	V _{DDO}	—	V
	VOH	V_{Ix} = H , I_{OH} = -4 mA	V _{DDO} - 0.4	V _{DDO} - 0.2	—	v
Logic Low-level	V _{OL}	V_{Ix} = H , I_{OL} = 20 μ A	—	0	0.1	V
output voltage		V_{Ix} = H , I_{OL} = 4 mA	—	0.2	0.4	v
Output Impedance	Zo	_	—	50	—	Ω
	VIH	_	0.7 x V _{DDI}	—	—	V
	VIL	_	_	—	0.3 x V _{DDI}	V
	V _{HYS}		_	0.37	_	V
Input current	h	$V_I = V_{DDI} \text{ or } 0 V$		—	±10	μA

Note: V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}

11.2. Switching Characteristics – 5 V Supply

Table 11.2 Switching Characteristics – 5 V Supply

(•D		0 1 10 0.0 1	v over recommended operating		13 unic33		
Charact	teristics	Symbol	Test condition	Min	Тур.	Мах	Unit
Data Rate		t _{bps}	—	DC	—	50	Mbps
Propagation	Delay	t _{PHL} , t _{PLH}	50 kHz, Duty = 50 %, C∟= 15 pF	_	10.9	18.3	ns
Pulse Width	Distortion	PWD	tphl — tplh	_	0.8	5.1	ns
Propagation (Between any	•	tрsк	(Note1)		_	13	ns
Channel Matching	Opposing Direction	t _{skOD}	_		_	4.5	ns
Output signa rise time	l	tr	10% to 90%	_	0.9	_	ns
Output signa fall time	I	tŗ	90% to 10%		0.9		ns
Common-Mo Transient Im		CMTI	V_{I} = V_{DDI} or 0 V , V_{CM} = 1500 V		100		kV/µs

(V_{DD1} = V_{DD2} =4.5 V to 5.5 V over recommended operating conditions unless otherwise noted)

Note1: The Propagation delay skew, t_{PSK}, is equal to the magnitude of the difference in propagation delay.

That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

11.3. Supply Current Characteristics – 5 V Supply

Table 11.3 Supply Current Characteristics – 5 V Supply

(VDD) - VDD2 -4.5 V to 5.5 V over recommended operating conditions unless otherwise noted)								
Characteristics		Symbol	Test condition	Min	Тур.	Мах	Unit	
		Primary side	I _{DDQ1(0)5}	V _I = Low	_	2.0	3.0	mA
DC Supp	ly	Fillinally side	I _{DDQ1(1)5}	V _I = High	_	7.2	10.4	ША
Current	-	Secondary	IDDQ2(0)5	V _I = Low	—	2.0	3.0	mA
		side	IDDQ2(1)5	Q2(1)5 VI = High		7.2	10.4	ША
	t _{bps} =	Primary side	I _{DD1(1)5}	f _{CLK} = 500 kHz, Duty = 50 %	_	4.6	6.8	
	1 Mbps	Secondary side	IDD2(1)5	square wave, $C_L = 15 \text{ pF}$	_	4.6	6.8	mA
Supply Current	t _{bps} =	Primary side	IDD1(25)5	f _{CLK} = 12.5 MHz, Duty = 50 %	_	6.1	8.5	
(AC signal)	25 Mbps	Secondary side	I _{DD2(25)5}	square wave, $C_L = 15 \text{ pF}$	—	6.1	8.5	mA
	t _{bps} =	Primary side	IDD1(50)5	f _{CLK} = 25 MHz, Duty = 50 %	_	7.1	9.9	
	50 Mbps	Secondary side	IDD2(50)5	square wave, $C_L = 15 \text{ pF}$	_	7.1	9.9	mA

(V_{DD1} = V_{DD2} =4.5 V to 5.5 V over recommended operating conditions unless otherwise noted)

11.4. Supply Current Characteristics – 3.3 V Supply

Table 11.4 Supply Current Characteristics – 3.3 V Supply (Note)

(V_{DD1} = V_{DD2} = 3.0 V to 3.6 V over recommended operating conditions unless otherwise noted)

Characteristics	Symbol	Test condition	Min	Тур.	Max	Unit
Vpp Under Voltage	VDD _{xUV+}	Positive VDDx Threshold	—	2.1	2.25	
V _{DD} Under Voltage Lockout threshold	VDD _{xUV-}	Negative VDDx Threshold	1.7	1.9	—	V
Voltage Logic High-level	VDD _{xUVH}	VDDx Hysteresis	0.1	0.2	—	
Logic High-level output voltage	Vон	V _{Ix} = H , I _{OH} = - 20 µA	V _{DDO} - 0.1	Vddo	_	V
	VOH	V_{Ix} = H , I_{OH} = - 4 mA	V _{DDO} - 0.4	V _{DDO} -0.2	_	v
Logic Low-level	Vol	V_{Ix} = H , I_{OL} = 20 μ A	—	0	0.1	V
output voltage	VOL	V_{Ix} = H , I_{OL} = 4 mA	—	0.2	0.4	v
Output Impedance	Zo		_	50	_	Ω
Logic High-level input Threshold voltage	VIH	_	0.7 x V _{DDI}	_	—	V
Logic Low-level input Threshold voltage	Vı∟	_	_	_	0.3 x V _{DDI}	V
Logic Input threshold voltage hysteresis	V _{HYS}			0.32		V
Input current	lı	$V_{I} = V_{DDI} \text{ or } 0 V$			±10	μA

Note: V_{DDI} = Input-side V_{DD} , V_{DDO} = Output-side V_{DD}

11.5. Switching Characteristics – 3.3 V Supply

Table 11.5 Switching Characteristics – 3.3 V Supply

$(V_{DD1} = V_{DD2} = 3.0 \text{ V to } 3.6 \text{ V}$	over recommended operating	conditions unless otherwise noted)

Characteristics		Symbol	Test condition	Min	Тур.	Мах	Unit
Data Rate		t _{bps}	_	DC	_	50	Mbps
Propagation D	elay	t _{PHL} , t _{PLH}	50 kHz, Duty = 50 %, C∟= 15 pF		11.6	19.1	ns
Pulse Width D	istortion	PWD	tphl — tplh	_	0.8	5.1	ns
Propagation D (Between any	•	tрsк	(Note1)		_	13	ns
Channel Matching	Opposing Direction	t _{skOD}	_	_	—	4.5	ns
Output signal rise time		tr	10% to 90%	_	0.8	_	ns
Output signal fall time		t _f	90% to 10%	—	0.8	_	ns
Common-Mod Transient Imm	-	CMTI	$V_{\rm I}$ = $V_{\rm DDI}$ or 0 V , $V_{\rm CM}$ = 1500 V	_	100		kV/µs

Note1: The Propagation delay skew, t_{PSK}, is equal to the magnitude of the difference in propagation delay.

That will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

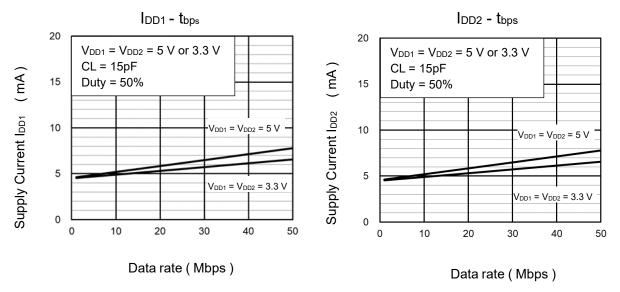
11.6. Supply Current Characteristics – 3.3 V Supply

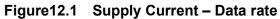
Table 11.6 Supply Current Characteristics – 3.3 V Supply

Characteristics		Symbol	Test condition	Min	Тур.	Max	Unit		
DC Supply		Drimony side	IDDQ1(0)3	V ₁ = Low —		2.0	2.8	m۸	
		Primary side	IDDQ1(1)3	V _I = High	—	7.1	10.2	mA	
		Secondary	IDDQ2(0)3	V _I = Low	_	2.0	2.8	mA	
		side	IDDQ2(1)3	V _I = High	_	7.1	10.2	ША	
Supply	t _{bps} = 1 Mbps	Primary side	IDD1(1)3	f _{CLK} = 500 kHz, Duty = 50 % square wave, C _L = 15 pF	—	4.5	6.6	mA	
		Secondary side	IDD2(1)3		—	4.5	6.6		
	t _{bps} = 25 Mbps	Primary side	IDD1(25)3	f _{CLK} = 12.5 MHz, Duty =	_	5.5	7.6	mA	
		Secondary side	I _{DD2(25)3}	50 % square wave, C∟ = 15 pF	—	5.5	7.6		
U ,	t _{bps} = 50 Mbps	Primary side	IDD1(50)3	f _{CLK} = 25 MHz, Duty = 50 % square wave, C _L = 15 pF	_	6.1	8.5	mA	
		Secondary side	IDD2(50)3			6.1	8.5		

12. Characteristic Chart (Note)

12.1. Supply Current vs Data rate





12.2. Output Voltage vs Output Current

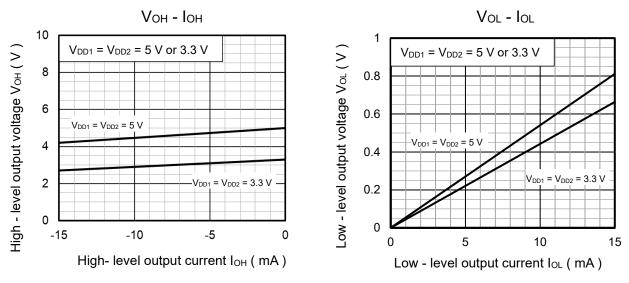


Figure12.2 Output Voltage – Output Current

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

DCM321C00

12.3. Propagation Delay Time vs Ambient Temperature

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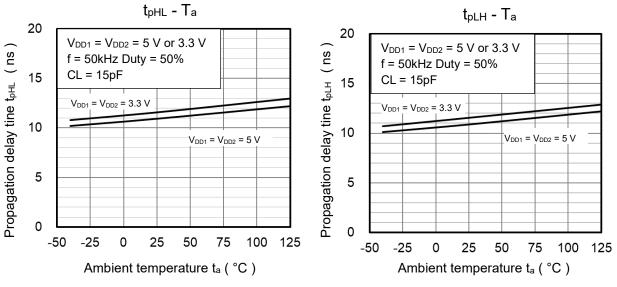


Figure12.3 Propagation Delay Time vs Ambient Temperature

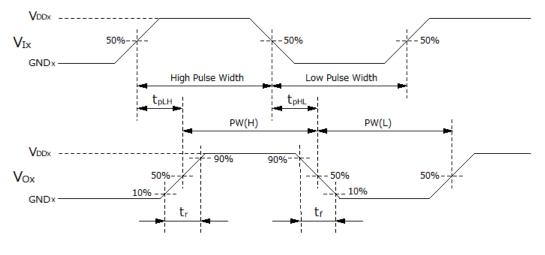


Figure12.4 Switching Waveforms

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Package Information

Parameters	Symbol	DCM321C00	Unit
Minimum clearance	CLR	4.0	mm
Minimum creepage distance	CPG	3.8	mm
Minimum insulation thickness	DTI	17	μm
Comparative tracking index	CTI	550	V

Table 13.1 Insulation Related Specifications (Note)

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g., at a standard distance between soldering eye centers of 3.8 mm). If this is not permissible, the user shall take suitable measures.

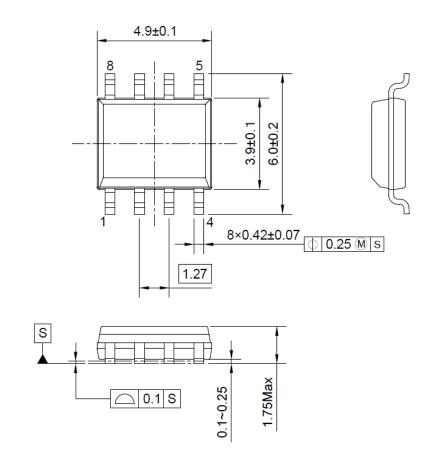
Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

14. Package Information

14.1. Package Dimensions

8pin SOIC (P-SOP8-0405-1.27-002)

UNIT: mm

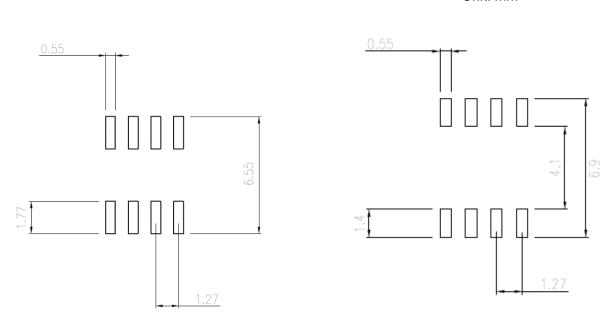


Weight: 0.07 g (typ.)



14.2. Land Pattern Dimensions for Reference only





Complies with JEITA ET-7501 Level 3 Normal

Isolation option

Unit: mm



Notes.

- Unless otherwise indicated, dimensions are given in millimeters.
- This document is a reference drawing in accordance with JEITA ET-7501 Level 3. The Company does not guarantee the accuracy or completeness of the diagrams and information.
- The customer should fully evaluate the various conditions (soldering conditions, etc.) and adjust at their own risk.
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- When designing and using the product, check the latest information on the product and the operating instructions of the equipment in which the product is to be used, and follow these instructions.

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