32-bit RISC Microcontroller
Reference Manual

Advanced Encoder Input Circuit (32-bit) (A-ENC32-A)

Revision 1.5

2024-10

Toshiba Electronic Devices & Storage Corporation

Contents

List of Figures

List of Tables

Preface

Related Documents

Document name
Exception
Clock Control and Operation Mode
Product Information
Advanced Programmable Motor Control Circuit
Programmable Motor Control Circuit Plus

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this Reference Manual.

A-PMD	Advanced Programmable Motor Control Circuit
ADC	Analog to Digital Converter
BLDC	Brushless DC
BEMF	Back Electromotive Force
CCW	Counter Clockwise
CW	Clockwise
PMD+	Programmable Motor Control Circuit Plus
PWM	Pulse Width Modulation

1. Outlines

One unit of Advanced encoder input circuit (32-bit) (hereafter A-ENC32-A operates as one channel input circuit (ENCxA/ENCxB/ENCxZ). The list of the functions is shown in the following table.

Function category	Function	Operation
Sensor input	Encoder mode	An incremental encoder of AB or ABZ type is connected in this mode. ● The rotation edge is detected and the rotation direction is judged by combination of ENCxA and ENCxB inputs. ● The counter counts up or down depending on the rotation direction. ● The maximum count number per cycle is 2^{32}. ● ENCxZ input logic is selectable.
	Sensor mode (Event count)	2-phase or 3-phase Hall IC (U, V, or W) is connected in this mode. ● The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. ● The counter counts up or down depending on the rotation direction. ● The maximum count number is 2^{32}.
	Sensor mode (Timer count)	2-phase or 3-phase Hall IC (U, V, or W) is connected in this mode. ● The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. ● The interval of the rotation edge detection can be measured by the 32-bit counter. ● Comparison function: Commutation trigger of PMD circuit synchronous with the edge detection can be generated. ● Sensor-less control of a pulse driven brushless DC (BLDC) motor is supported by PWM synchronous sampling.
	Sensor mode (Phase count)	2-phase or 3-phase Hall IC (U, V, or W) is connected in this mode. ● The rotation edge is detected and the rotation direction is judged by combination of 2-phase or 3-phase signals. ● The interval of the rotation edge detection can be measured by the 32-bit counter. ● The counter operates with any frequency clock and the count-up and count-down can be selected.
General purpose timer	Timer mode	This circuit is used as a 32-bit timer operating with the system clock (fsys) in this mode. ● ENCxZ input edge detection can be done. ● The interval of the rotation edge detection can be measured by the 32-bit counter. ● An interrupt can be generated by the comparison function.
Phase counter	Phase counter mode (Phase measurement)	This circuit is used as a 32-bit counter operating with any frequency clock in this mode. ● ENCxZ input edge detection can be done. ● The interval of the rotation edge detection can be measured by the 32-bit counter. ● An interrupt can be generated by the comparison function.
	Phase counter mode (Phase difference measurement)	This circuit is used as a 32-bit counter operating with any frequency clock in this mode. The phase difference between the general purpose timer output and ENCxZ input can be measured.
Noise cancellation	Input circuit	The sampling by fsys division clock or a signal synchronous with PWM signal can be done. ● The width of the noise cancellation can be selected.

Table 1.1 Signal Input Pin

Signal name		Encoder A, B, or Z	Hall sensor U, V, or W
Connection pin	ENCxA	A	U
	ENCxB	B	V
	ENCxZ	Z	W

2. Configuration

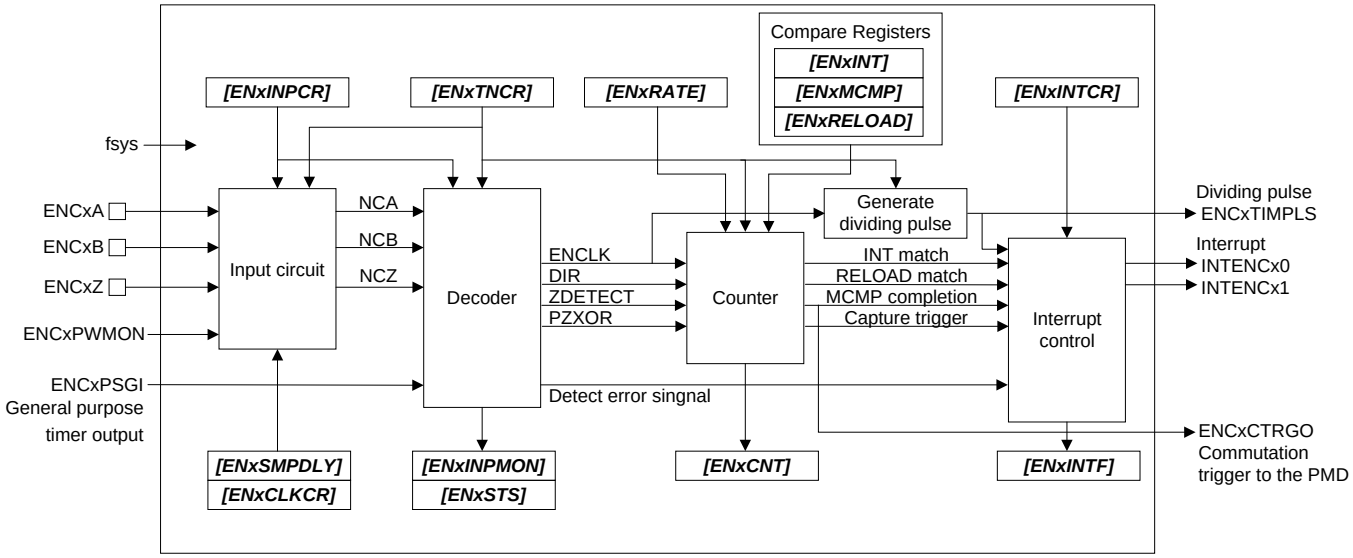

Figure 2.1 Block Diagram of A-ENC32-A

Table 2.1 List of Signals

No	Symbol	Signal name	I/O	Reference manual
1	fsys	System clock	Input	Clock Control and Operation Mode
2	ENCxA	Encoder input A pin	Input	Product Information
3	ENCxB	Encoder input B pin	Input	Product Information
4	ENCxZ	Encoder input Z pin	Input	Product Information
5	ENCxPWMON	PWM signal for sampling	Input	Product Information
6	ENCxCTRGO	Commutation trigger for PMD	Output	Product Information
7	ENCxPSGI	General purpose timer output signal	Input	Product Information
8	ENCxTIMPLS	Division pulse signal	Output	Product Information
9	INTENCx0	Encoder input interrupt 0	Output	Exception, Product Information
10	INTENCx1	Encoder input interrupt 1	Output	Exception

3. Function and Operation

3.1. Clock Supply

When A-ENC32-A is used, the corresponding clock enable bits should be set to "1" (Clock supply) in fsys supply stop register A (***[CGFSYSENA]*** and ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]*** and ***[CGFSYSMENB]***), fsys supply stop register C (***[CGFSYSMENC]***), and fc supply stop register (***[CGFCEN]***). The registers and the bit locations depend on each product. Some products do not have all registers. For the details, refer to the reference manual "Clock control and operation mode".

3.2. Operation Mode

There are 13 operation modes in A-ENC32-A. The mode is determined by the setting of ***[ENxTNCR]*** <MODE[2:0]>, <P3EN>, and <ZEN>. The other combinations should not be set.

The operation modes are shown in the following table.

Table 3.1 Operation Modes

[ENxTNCR]			**Input pin**	**Mode**
<MODE[2:0]>	**<ZEN>**	**<P3EN>**		
000	0	0	ENCxA and ENCxB	Encoder mode (without ENCxZ signal)
	1		ENCxA, ENCxB, and ENCxZ	Encoder mode (with ENCxZ signal)
001	0	0	ENCxA and ENCxB	Sensor mode (Event count: 2-phase input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Event count: 3-phase input)
010	0	0	ENCxA and ENCxB	Sensor mode (Timer count: 2-phase input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Timer count: 3-phase input)
011	0	0	-	Timer mode
	1		ENCxZ	Timer mode (with capture input)
110	0	0	ENCxA and ENCxB	Sensor mode (Phase count: 2-phase input)
		1	ENCxA, ENCxB, and ENCxZ	Sensor mode (Phase count: 3-phase input)
111	0	0	-	Phase counter mode (Phase count)
	1		ENCxZ	Phase counter mode (Phase count: with capture input)
	1	1	ENCxZ	Phase counter mode (Phase difference measurement)

3.2.1. Encoder Mode

This mode supports High-speed position sensor (Phase judgment). The incremental encoder (AB and ABZ) should be used.

- Using the rotation edge detection, divided pulse and an interrupt can be generated.
- Using the rotation edge pulse count, an interrupt can be generated at any counter value.
- Rotation direction judgment
- 32-bit up- and down-count (controlled by the rotation direction judgment)
- The setting of the counter value is available.
- The setting of the detected rotation direction is available.
- Abnormal state detection flag

(1) ENCxZ input is valid. Positive logic input: (***[ENxTNCR]***<ZEN> = 1 and ***[ENxTNCR]***<ZEACT> = 0)

In the case of ***[ENxRELOAD]***<RELOAD[31:0]> = 0x00000380 and ***[ENxINT]***<INT[31:0]> = 0x00000002;

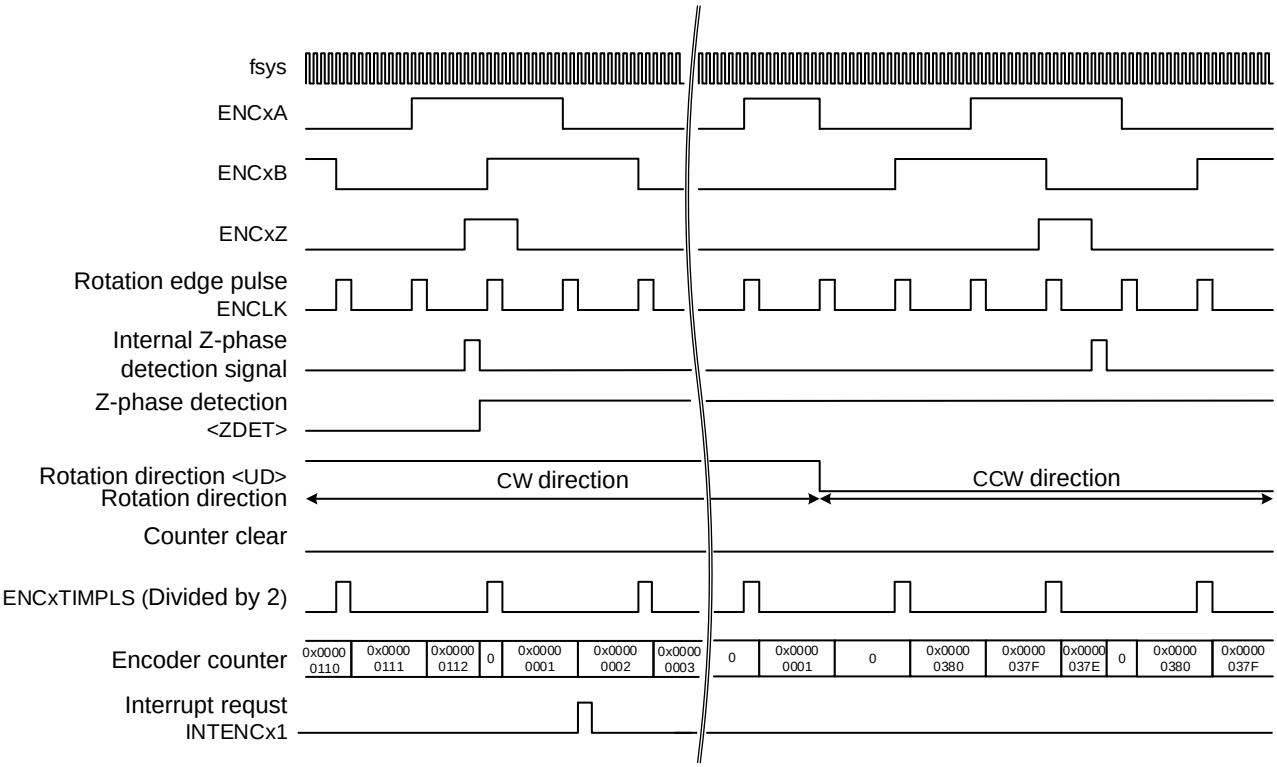

Figure 3.1 ENCxZ Input is Valid (*[ENxTNCR]*<ZEN> = 1)

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN> = 0)

In the case of ***[ENxRELOAD]***<RELOAD[31:0]> = 0x00000380 and ***[ENxINT]***<INT[31:0]> = 0x00000002;

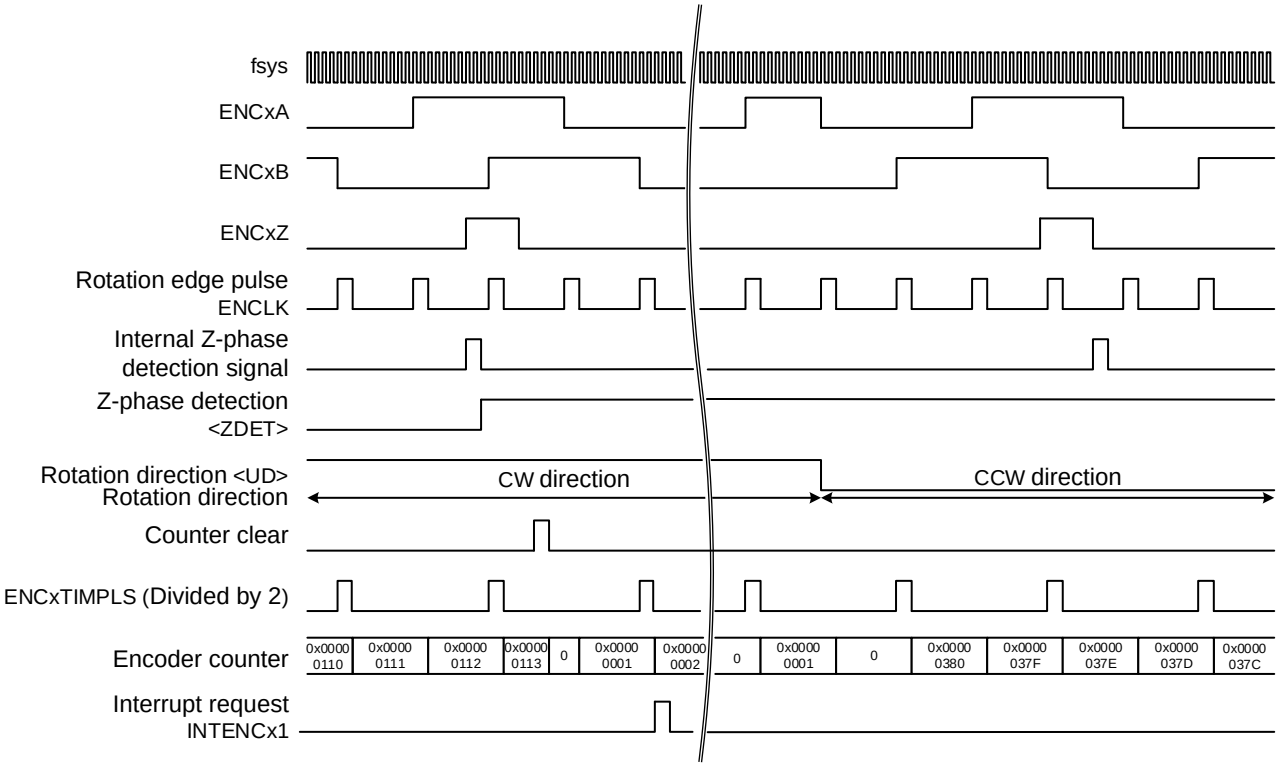

Figure 3.2 ENCxZ Input is Invalid (*[ENxTNCR]*<ZEN> = 0)

In the encoder mode, incremental encoder signals should be connected to ENCxA, ENCxB, and ENCxZ pins. The frequencies of ENCxA and ENCxB signals are multiplied by 4. Then, the rotation edge pulses are counted.

When the rotation is in CW direction (ENCxA is 90 degrees ahead comparing with ENCxB), the counter value increments. After the counter value matches the value in ***[ENxRELOAD]***<RELOAD[31:0]>, the counter is cleared to "0x00000000" at the next ENCLK.

When the rotation is in CCW direction (ENCxA is 90 degrees late comparing with ENCxB), the counter value decrements. After the counter value equals to "0x00000000", the counter value is set to the value in ***[ENxRELOAD]***<RELOAD[31:0]> at the next ENCLK.

When <ZEN> is set to "1", ENCxZ pin input is valid.

When <ZEN> = 1 and <ZEACT> = 0 (Input positive logic), the counter is cleared to "0x00000000" by the rising edge of ENCxZ in the CW-direction rotation, and by the falling edge of ENCxZ in the CCW-direction rotation.

When <ZEN> = 1 and <ZEACT> = 1 (Input negative logic), the counter is cleared to "0x00000000" by the falling edge of ENCxZ in the CW-direction rotation, and by the rising edge of ENCxZ in the CCW-direction rotation.

If ENCLK timing coincides with ENCxZ detection timing, the counter is cleared to "0x00000000" without counting.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0x00000000".

When the rotation direction is detected as CW direction, ***[ENxSTS]***<UD> is set to "1", and detected as CCW direction, cleared to "0".

[ENxTNCR]<DECMD[1:0]> can set the detecting direction to CW direction only or CCW direction only. And, when <DECMD[1:0]> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]*** <DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

ENCxTIMPLS is a signal which ENCLK is divided, and the division ratio is selected by ***[ENxTNCR]*** <ENDEV[2:0]>.

When ***[ENxINTCR]***<CMPIE> = 1 and the counter value becomes ***[ENxINT]***<INT[31:0]> value, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE> = 1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value, INTENCx1 interrupt occurs.

When <ZEN> = 1, however, the coincidence interrupt does not occur during the period of ***[ENxSTS]*** <ZDET> = 0.

<ZDET> is set to "1" when the first ENCxZ signal is detected after the encoder input is enabled.

<ZDET> and ***[ENxSTS]***<UD> are cleared to "0" when ***[ENxTNCR]***<ENRUN> = 0.

3.2.2. Sensor Mode

The low-speed position sensor (Zero-cross judgment) is supported to use 2-phase Hall sensor input and 3-phase Hall sensor input. There are three sensor modes, Event count mode, Timer count mode, and Phase count mode.

In the timer count mode and the phase count mode, when PMD circuit drives BLDC motor with the pulse signal, the zero-cross detection of the induced voltage can be supported by using PWM synchronous sampling. (BEMF detection control)

3.2.2.1. Event Count

The count is done by the rotation edge detection.

- Using the rotation edge detection, a division pulse and an interrupt can be generated.
- Using the rotation edge pulse count, an interrupt can be generated at any counter value.
- Rotation direction judgment
- 32-bit up- and down-count (controlled by the rotation direction judgment)
- The setting of the detected rotation direction is available.
- Abnormal state detection flag

(1) 3-phase decode (***[ENxTNCR]***<P3EN> = 1)

In the case of ***[ENxINT]***<INT[31:0]> = 0x00000002;

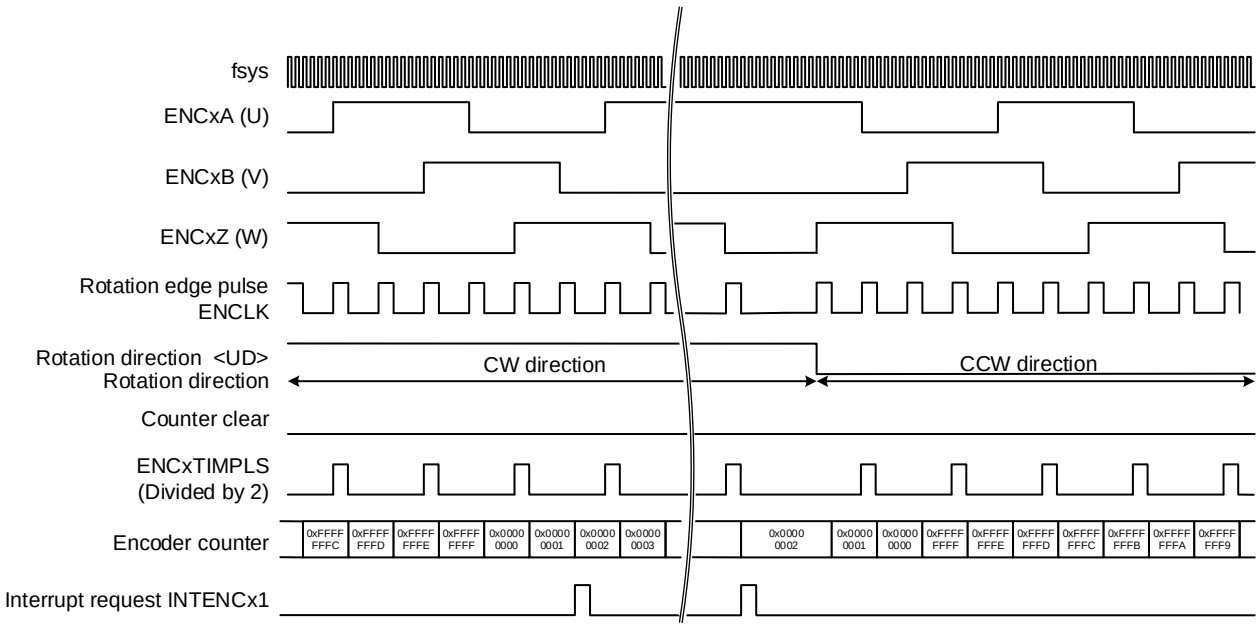

Figure 3.3 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN> = 0)

In the case of ***[ENxINT]***<INT31:0]> = 0x00000002;

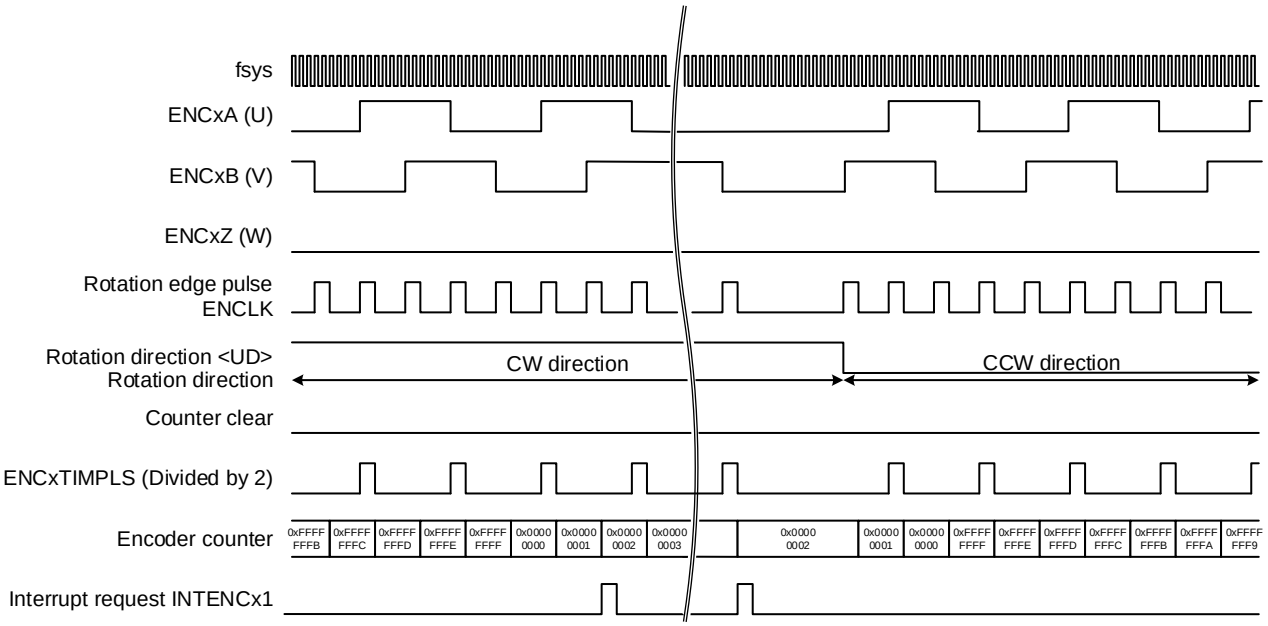

Figure 3.4 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

The outputs of Hall sensor (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN> = 0, the frequency of 2-phase inputs (ENCxA and ENCxB) is multiplied by 4, and when <P3EN> = 1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) is multiplied by 6. Then, the rotation edge pulses are counted.

When the rotation is in CW direction (i.e., ENCxA has 90-degree (2-phase input) or 120-degree (3-phase input) phase lead to ENCxB), the counter value increments. After the counter value matches the value "0xFFFFFFFF", the counter is cleared to "0x00000000" at the next ENCLK.

When the rotation is in CCW direction (i.e., ENCxA has 90-degree (2-phase input) or 120-degree (3-phase input) phase lag to ENCxB), the counter value decrements. After the counter value equals to "0x00000000", the counter value is set to the value "0xFFFFFFFF" at the next ENCLK.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0x00000000".

When the rotation direction is detected as CW direction, ***[ENxSTS]***<UD> is set to "1", and detected as CCW direction, cleared to "0". <UD> is cleared to "0" when ***[ENxTNCR]***<ENRUN> = 0.

[ENxTNCR]<DECMD> can set the rotation direction to CW direction only or CCW direction only. When <DECMD> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

ENCxTIMPLS is a division of ENCLK, and the division ratio is selected by ***[ENxTNCR]***<ENDEV[2:0]>.

When ***[ENxINTCR]***<CMPIE>=1 and the counter value becomes ***[ENxINT]***<INT[31:0]> value, INTENCx1

interrupt occurs.

When ***[ENxINTCR]***<MCMPIE>=1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value, INTENCx1 interrupt occurs.

3.2.2.2. Timer Count

(1) 3-phase decode (***[ENxTNCR]***<P3EN> = 1)

In the case of ***[ENxINT]***<INT[31:0]> = 0x00000002;

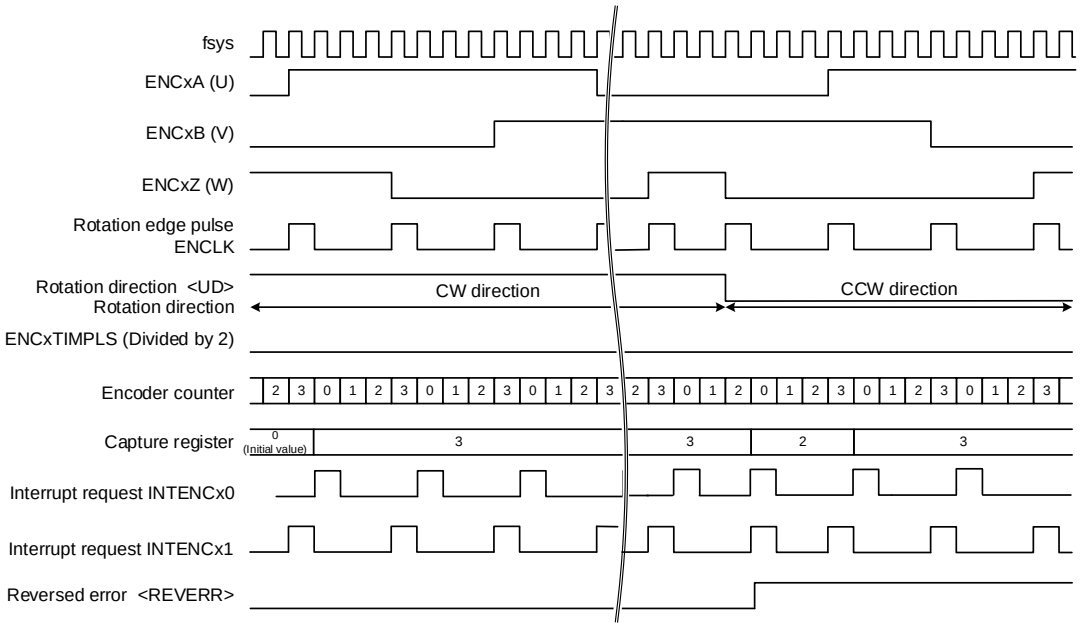

Figure 3.5 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN> = 0)

In the case of ***[ENxINT]***<INT[31:0]> = 0x00000002;

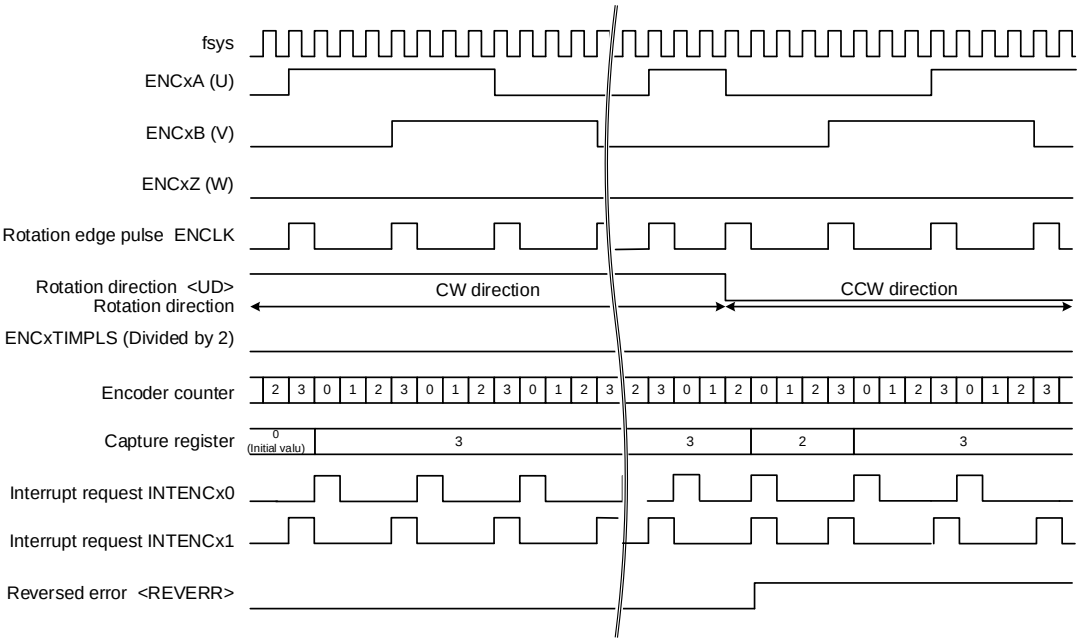

Figure 3.6 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

The outputs of Hall sensor (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN> = 0, the frequency of 2-phase inputs (ENCxA and ENCxB) is multiplied by 4, and when <P3EN> = 1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) is multiplied by 6. Then, the rotation edge pulses (ENCLK) are generated.

The counter always increments. It is cleared to "0x00000000" by ENCLK. When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0x00000000".

The counter value is captured by ENCLK. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

The value in ***[ENxCNT]***<CNT[31:0]> (the captured value) is kept regardless of the value of ***[ENxTNCR]*** <ENRUN>.

When the rotation direction is detected as CW direction, ***[ENxSTS]***<UD> is set to "1", and detected as CCW direction, cleared to "0". <UD> is cleared to "0" when <ENRUN> = 0. When the rotation direction changes, ***[ENxSTS]***<REVERR> = 1 is set. The flag is cleared by reading itself.

[ENxTNCR]<DECMD[1:0]> can set the rotation direction to CW direction only or CCW direction only. When <DECMD[1:0]> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

When ***[ENxINTCR]***<RLDIE> = 1 and the counter value becomes ***[ENxRELOAD]***<RELOAD[31:0]> value, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<CMPIE> = 1 and the counter value becomes ***[ENxINT]***<INT[31:0]> value, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE> = 1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value, INTENCx1 interrupt occurs. When ***[ENxTNCR]***<MCMPMD> = 1 is set and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value or more, INTENCx1 interrupt occurs.

3.2.2.3. Phase Count

(1) 3-phase decode (***[ENxTNCR]***<P3EN> = 1)

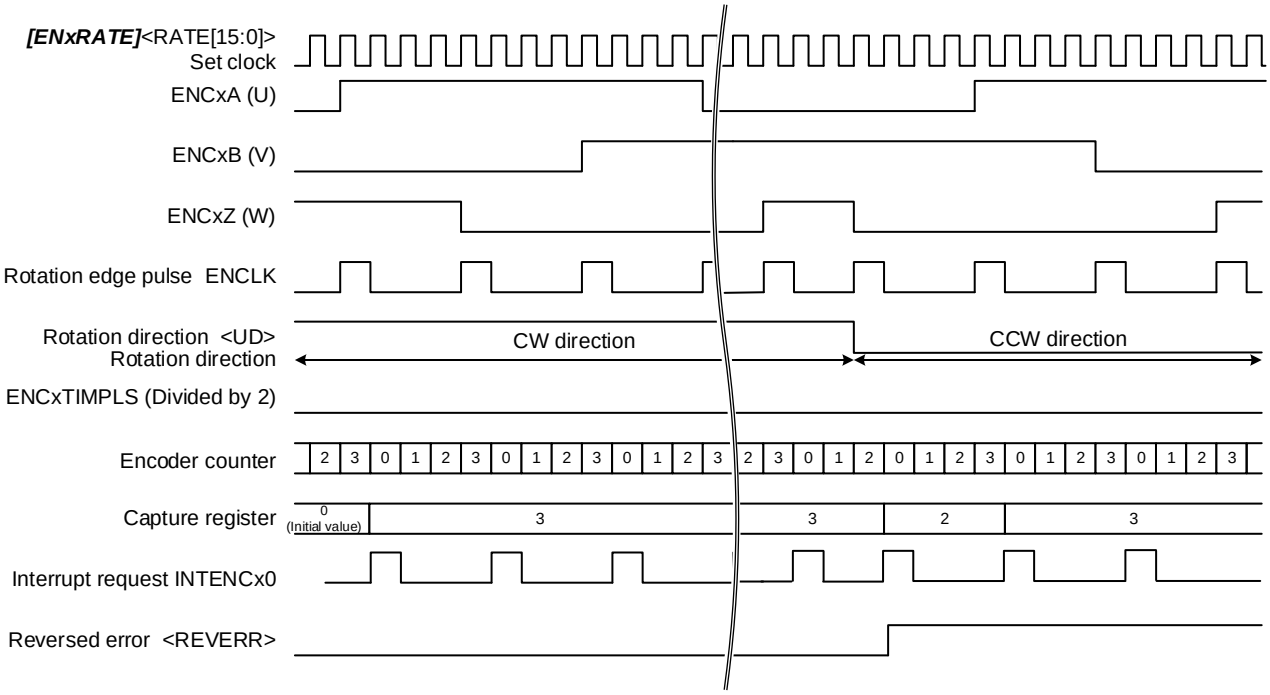

Figure 3.7 3-phase Decode (*[ENxTNCR]*<P3EN> = 1)

(2) 2-phase decode (***[ENxTNCR]***<P3EN> = 0)

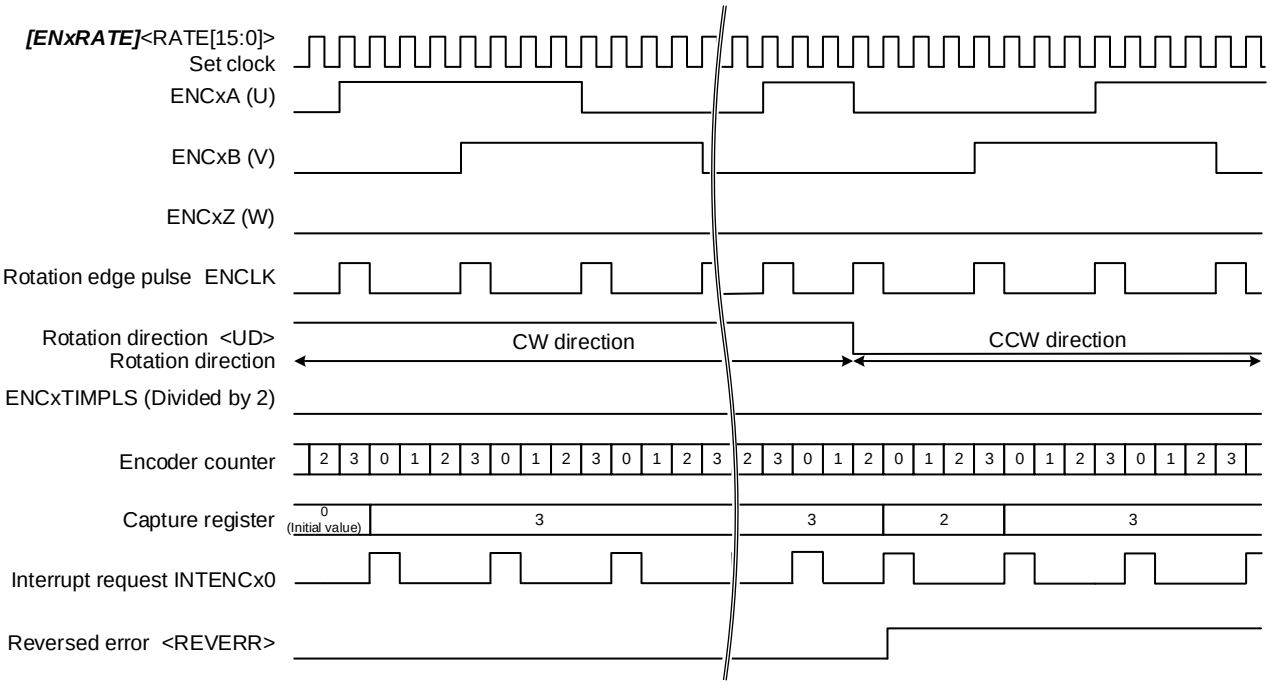

Figure 3.8 2-phase Decode (*[ENxTNCR]*<P3EN> = 0)

The outputs of Hall sensor (U, V, and W) are connected to ENCxA, ENCxB, and ENCxZ, respectively. When <P3EN> = 0, the frequency of 2-phase inputs (ENCxA and ENCxB) is multiplied by 4, and when <P3EN> = 1, the frequency of 3-phase inputs (ENCxA, ENCxB, and ENCxZ) is multiplied by 6. Then, the rotation edge pulses (ENCLK) are generated.

Using <UDMD> setting and ***[ENxRATE]***<RATE[15:0]> setting, the up-count of the counter or the down-count is controlled. The counter operates with any frequency. At up-count, when the counter value becomes ***[ENxRELOAD]***<RELOAD[31:0]> value, the counter is cleared to "0x00000000". At down-count, when the counter value becomes "0x00000000", the counter value is set to ***[ENxRELOAD]***<RELOAD[31:0]> value.

When <ENCLR> is set to "1", the counter is cleared to "0x00000000".

When <TOVMD> is set to "1", the counter stops at the value in ***[ENxRELOAD]***<RELOAD[31:0]>.

The counter value is captured by ENCLK. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

When <SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

The value in ***[ENxCNT]***<CNT[31:0]> (the captured value) is kept regardless of the value of <ENRUN>.

When the rotation direction is detected as CW direction, <UD> is set to "1", and detected as CCW direction, cleared to "0". <UD> is cleared to "0" when <ENRUN> = 0.
When the rotation direction changes, <REVERR> = 1 is set. The flag is cleared by reading itself.

[ENxTNCR]<DECMD[1:0]> can set the rotation direction to CW only or CCW only. When <DECMD[1:0]> is not "00", the rotation edge is detected by comparing the input state (***[ENxINPMON]***<DETMONA>, <DETMONB>, and <DETMONZ>) stored at the previous edge detection with the current input values.

When ***[ENxINTCR]***<CMPIE> = 1 and the counter value becomes ***[ENxINT]***<INT[31:0]>, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE> = 1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]>, INTENCx1 interrupt occurs.

3.2.3. Timer Mode

This circuit can be used as a general purpose 32-bit timer.

- 32-bit up-counter (fsys clock for counting)
- Counter clear control (Software clear, Comparison match clear, and External trigger)
- A match interrupt is generated by the comparison function.
- Capture function: External trigger capture (an interrupt generation available), and Software capture

(1) ENCxZ input is valid (***[ENxTNCR]***<ZEN> = 1)

[ENxINT]<INT[31:0]> = 0x00000006

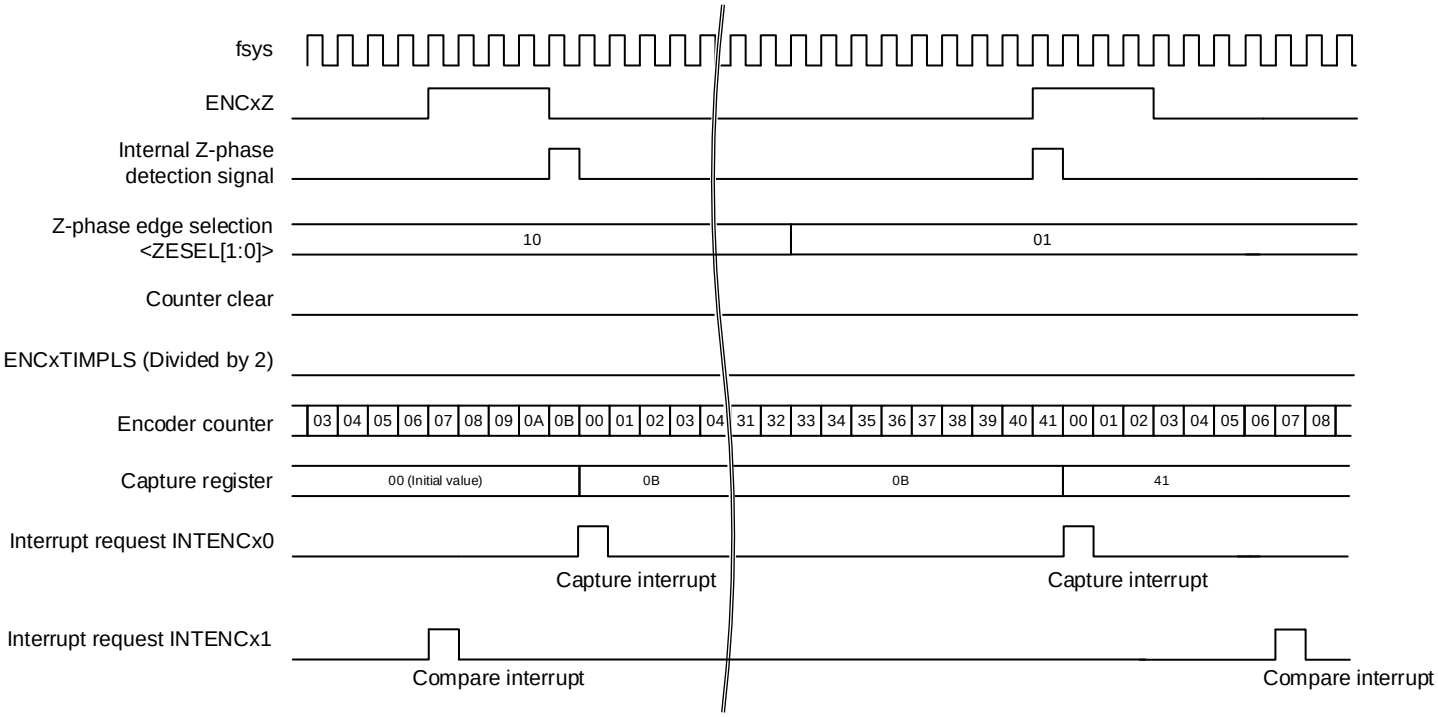

Figure 3.9 ENCxZ Input is Valid (*[ENxTNCR]*<ZEN> = 1)

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN> = 0)

[ENxINT]<INT[31:0]> = 0x00000006

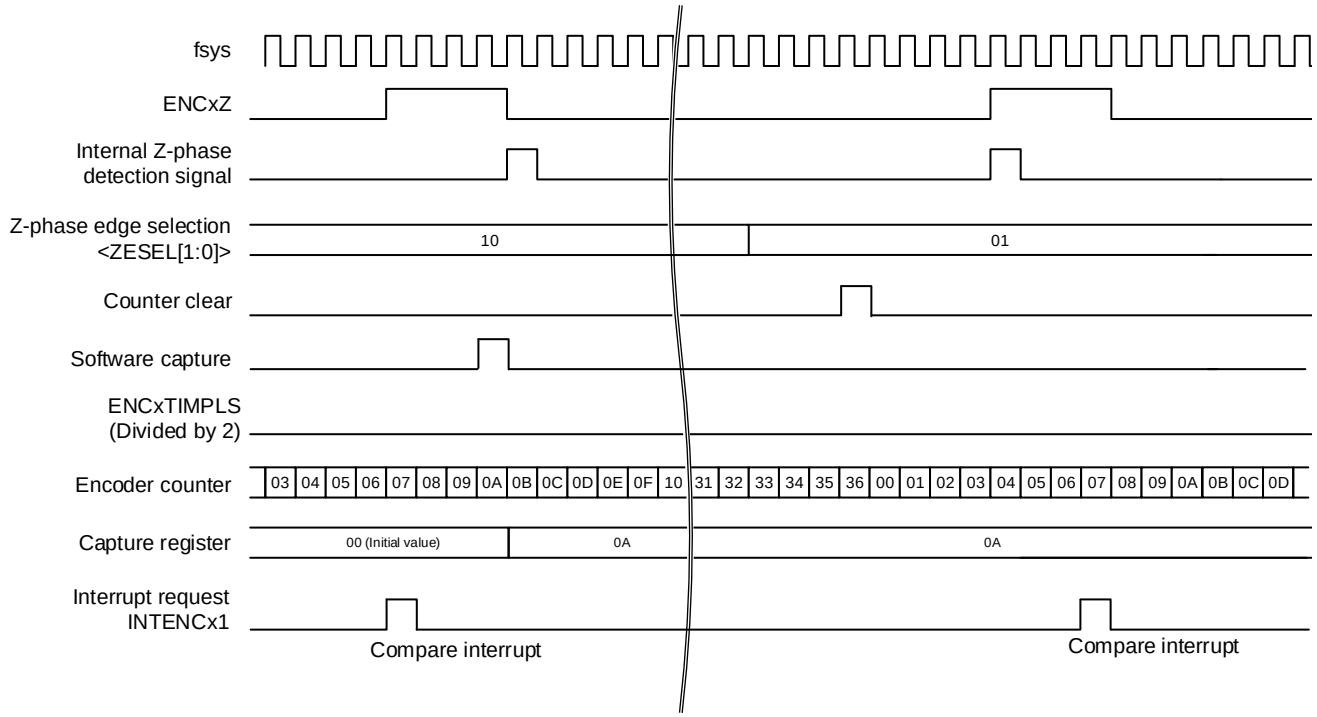

Figure 3.10 ENCxZ Input is Invalid (*[ENxTNCR]*<ZEN> = 0)

When <ZEN> = 1, ENCxZ input is used as an external trigger. When <ZEN> = 0, no external triggers are used. The counter always increments.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0x00000000".

When <ZEN> = 1 and ***[ENxTNCR]***<ZESEL[1:0]> = 01, the counter is cleared to "0x00000000" by ENCxZ rising edge. And when <ZESEL[1:0]> = 10, it is cleared by ENCxZ falling edge, and, when <ZESEL[1:0]> = 11, cleared by both edges.

The counter value is captured by the edge detection of ENCxZ. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

The value in ***[ENxCNT]***<CNT[31:0]> (the captured value) is kept regardless of the value of ***[ENxTNCR]*** <ENRUN>. The capture value is cleared only by the reset.

When ***[ENxINTCR]***<RLDIE> = 1 and the counter value becomes ***[ENxRELOAD]***<RELOAD[31:0]>, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<CMPIE> = 1 and the counter value becomes ***[ENxINT]***<INT[31:0]>, INTENCx1 interrupt

occurs.

When ***[ENxINTCR]***<MCMPIE> = 1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value, INTENCx1 interrupt occurs. When ***[ENxTNCR]***<MCMPMD> = 1 is set and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value or more, INTENCx1 interrupt occurs.

3.2.4. Phase Counter Mode

3.2.4.1. Phase Measurement

The counter is 32-bit one which is controlled by any frequency clock.

- Up- and down-count are available.
- Comparison function is available and a match interrupt can be generated.
- ENCxZ input can capture the counter value, clear the counter, and generate an interrupt.

(1) ENCxZ input is valid (***[ENxTNCR]***<ZEN> = 1).

[ENxINT]<INT[31:0]> = 0x00000006

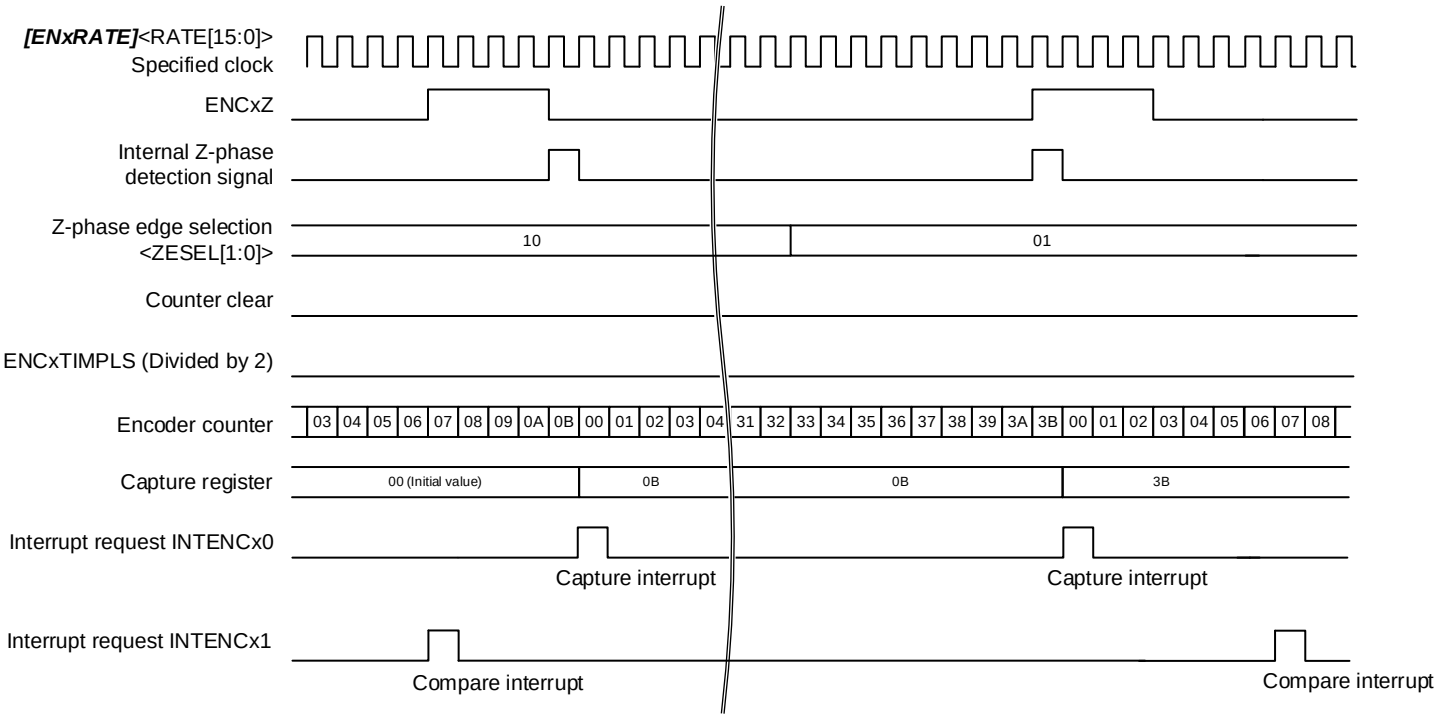

Figure 3.11 ENCxZ Input is Valid (*[ENxTNCR]*<ZEN> = 1)

(2) ENCxZ input is invalid (***[ENxTNCR]***<ZEN> = 0).

[ENxINT]<INT[31:0]> = 0x00000006

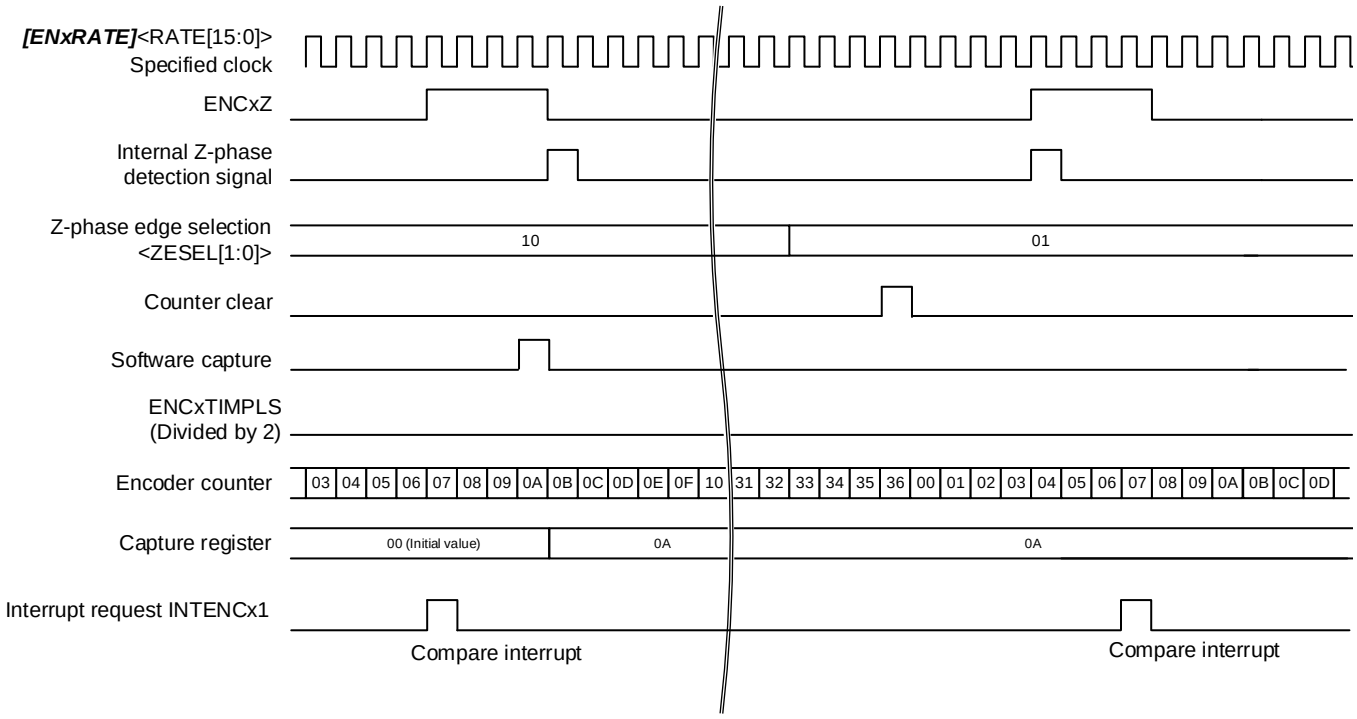

Figure 3.12 ENCxZ Input is Invalid (*[ENxTNCR]*<ZEN> = 0)

When <ZEN> = 1, ENCxZ input is used as an external trigger. When <ZEN> = 0, no external triggers are used. Using ***[ENxTNCR]***<UDMD> setting and ***[ENxRATE]***<RATE[15:0]> setting, the up-count and the down-count of the counter are controlled with any frequency clock.

At up-count, when the counter value becomes ***[ENxRELOAD]***<RELOAD[31:0]> value, the counter is cleared to "0x00000000".

At down-count, when the counter value becomes "0x00000000", the counter value is set to ***[ENxRELOAD]*** <RELOAD[31:0]> value.

When ***[ENxTNCR]***<TOVMD> = 1 is set, the counter stops at the value in ***[ENxRELOAD]***<RELOAD[31:0]>.

When ***[ENxTNCR]***<ENCLR> is set to "1", the counter is cleared to "0x00000000".

When <ZEN> = 1 and ***[ENxTNCR]***<ZESEL[1:0]> = 01, the counter is cleared to "0x00000000" by ENCxZ rising edge. And when <ZESEL[1:0]> = 10, it is cleared by ENCxZ falling edge, and, when <ZESEL[1:0]> = 11, cleared by both edges.

The counter value is captured by the edge detection of ENCxZ. The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

When ***[ENxTNCR]***<SFTCAP> is set to "1", the counter value is captured. The capture can be done at any timing.

The captured value can be read through ***[ENxCNT]***<CNT[31:0]>.

The value in ***[ENxCNT]***<CNT[31:0]> (the captured value) is kept regardless of the value of ***[ENxTNCR]*** <ENRUN>. The capture value is cleared only by the reset.

When ***[ENxINTCR]***<CMPIE> = 1 and the counter value becomes ***[ENxINT]***<INT[31:0]> value, INTENCx1 interrupt occurs.

When ***[ENxINTCR]***<MCMPIE> = 1 and the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value, INTENCx1 interrupt occurs.

3.2.4.2. Phase Difference Measurement

The phase difference can be measured in the phase counter mode with setting <P3EN> = <ZEN> = 1.
The up- and down-counter is controlled by the output of the general purpose timer (ENCxPSGI) and ENCxZ input.

- When the output of the general purpose timer and the value of ENCxZ input are the same, up-count is done. When they are different, down-count is done.
- The output edge of the general timer can capture the counter value, clear the counter, and generate an interrupt.

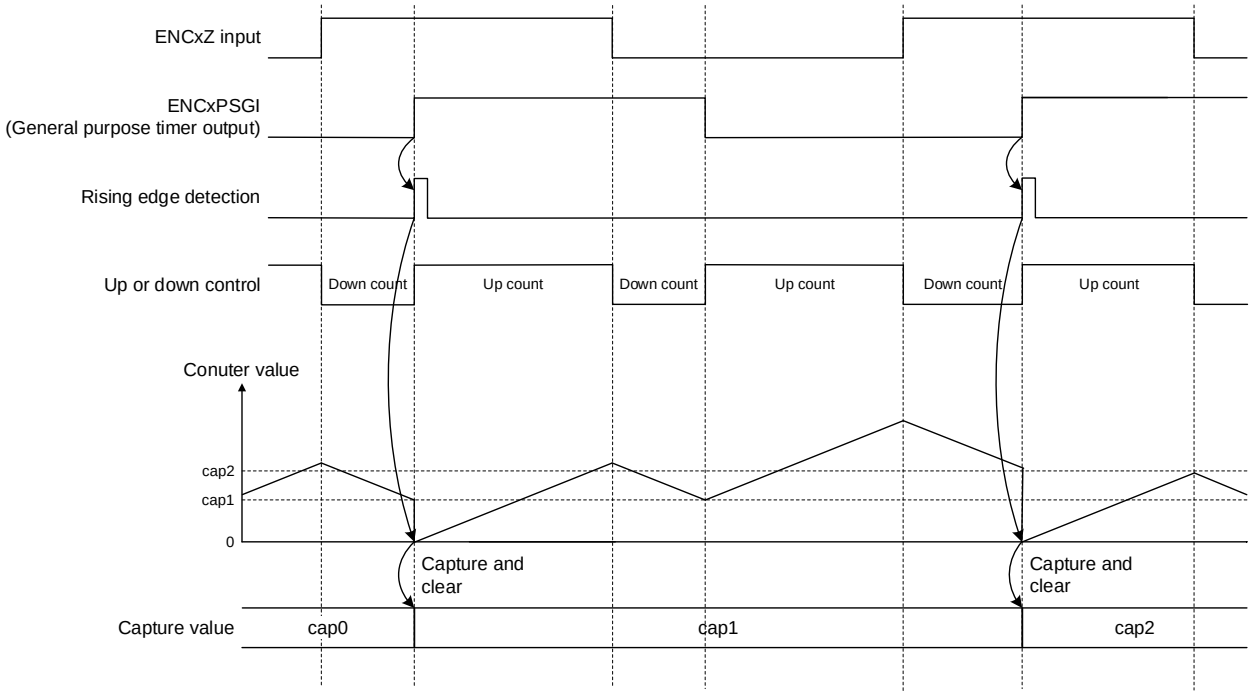

Figure 3.13 Operation of Phase Counter Mode (Phase Difference)

The output edge of the general purpose timer (ENCxPSGI) is detected, then the counter value is captured and the counter is cleared. The detection edge should be selected by ***[ENxTNCR]***<ZESEL[1:0]>. When ***[ENxTNCR]*** <ENCLR> is set to "1", the counter is cleared to "0x00000000".

The captured value represents the phase difference between ENCxZ input and the output of the general purpose timer (ENCxPSGI). The origin (the captured value is "0x00000000") of the phase difference between them is 1 / 4 cycles.

3.3. Function Outline of Each Circuit

3.3.1. Input Circuit

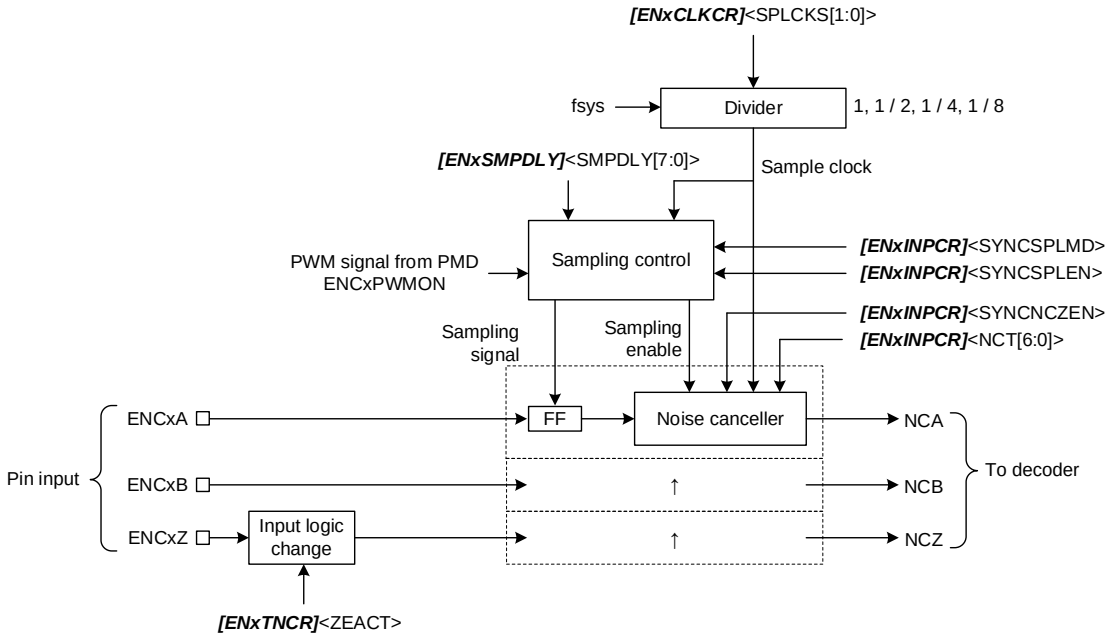

Figure 3.14 Input Circuit Configuration

The pin inputs (ENCxA, ENCxB, and ENCxZ) are sampled by a suitable sampling signal, and noises are reduced by the digital noise canceller in the input circuit.

The input logic change circuit of ENCxZ pin input is valid only in the encoder mode (***[ENxTNCR]*** <MODE[2:0]> = 000).

3.3.1.1. Sample Clock

The sample clock can be selected from among fsys, fsys/2, fsys/4, and fsys/8 by ***[ENxCLKCR]***<SPLCKS[1:0]>.

3.3.1.2. Sampling Mode

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN> = 0)

The input signals are sampled by the sampling clock which is selected by ***[ENxCLKCR]***<SPLCKS[1:0]>.

(2) PWM synchronous sampling (***[ENxINPCR]***<SYNCSPLEN> = 1)

The sampling is done at the timing synchronous with PWM signal (ENCxPWMON) from PMD.

- PWM-on period sampling (***[ENxINPCR]***<SYNCSPLMD> = 0)
  Only in the period when ENCxPWMON signal is On, the sampling is done by the clock selected by ***[ENxCLKCR]***<SPLCKS[1:0]>.
  An On-delay time can be set by ***[ENxSMPDLY]***<SMPDLY[7:0]> in PWM-on period sampling.

  Delay time: <SMPDLY[7:0]> × Sample clock cycle

Note: After A-ENC32-A is enabled (after changing [ENxTNCR]<ENRUN> from "0" to "1"), the first delay time may be different from the <SMPDLY[7:0]> setting value.

- PWM-off edge sampling ([ENxINPCR]<SYNCSPLMD>=1)
  The sampling signal is ENCxPWMON. The sampling is done at the Off edge of ENCxPWMON.

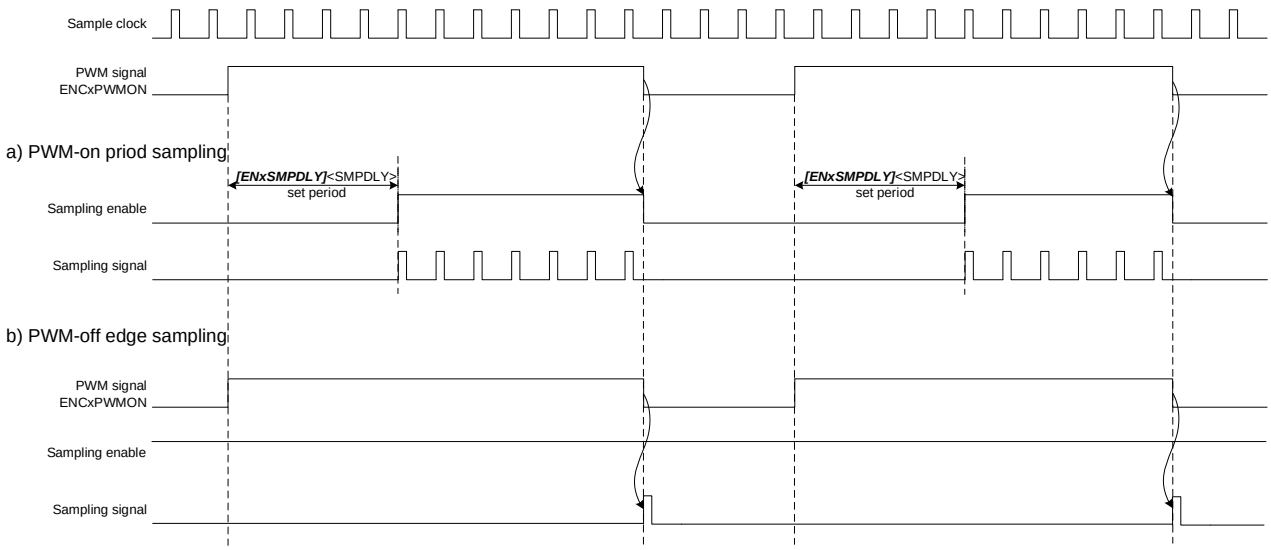

Figure 3.15 PWM Synchronous Sampling

3.3.1.3. Noise Cancellation

(1) Continuous sampling (***[ENxINPCR]***<SYNCSPLEN> = 0)

The noise cancellation time should be set to ***[ENxINPCR]***<NCT[6:0]>. The real noise cancellation time is calculated by the following formula.

Noise cancellation time: <NCT[6:0]> × Sample clock cycle

Note: When <NCT[6:0]> is set to "0x00", the noise cancellation is invalid.

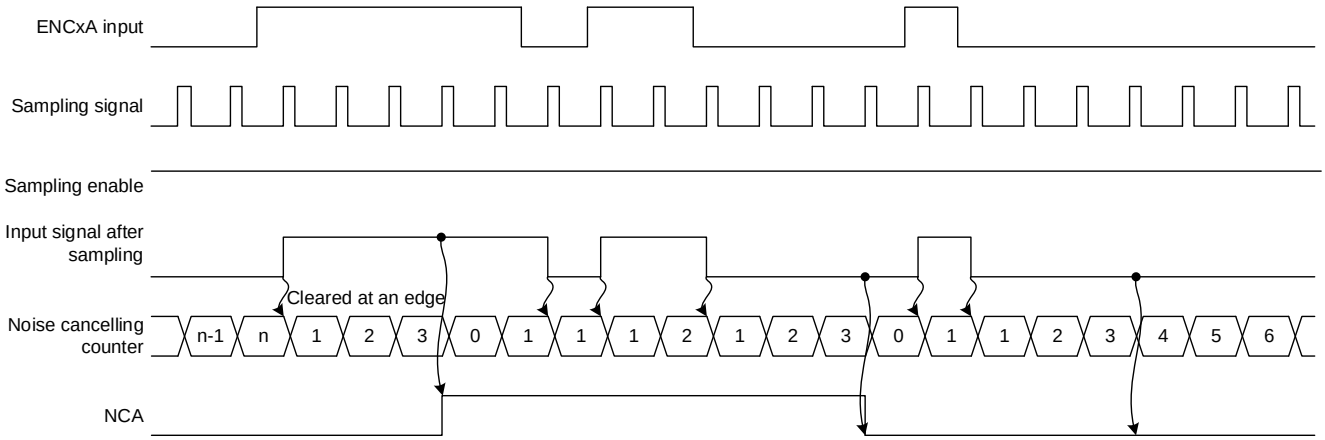

Figure 3.16 Noise Cancelling (Continuous Sampling: <NCT[6:0]> = 0x03)

(2) PWM-on period sampling (***[ENxINPCR]***<SYNCSPLEN>=1)

- The noise cancellation timer stops during "Low" period of the sampling enable signal (***[ENxINPCR]***<SYNCNCZEN> = 0).
- The noise cancellation timer is cleared during "Low" period of the sampling enable signal (***[ENxINPCR]***<SYNCNCZEN> = 1).

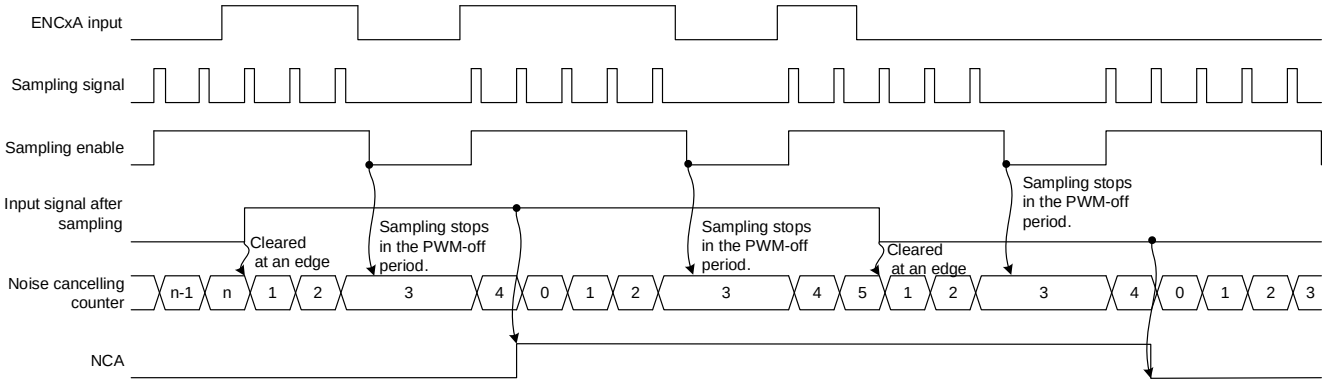

Figure 3.17 Noise Cancelling (PWM-on Period Sampling and PWM-off Period Stop: <NCT[6:0]> = 0x04)

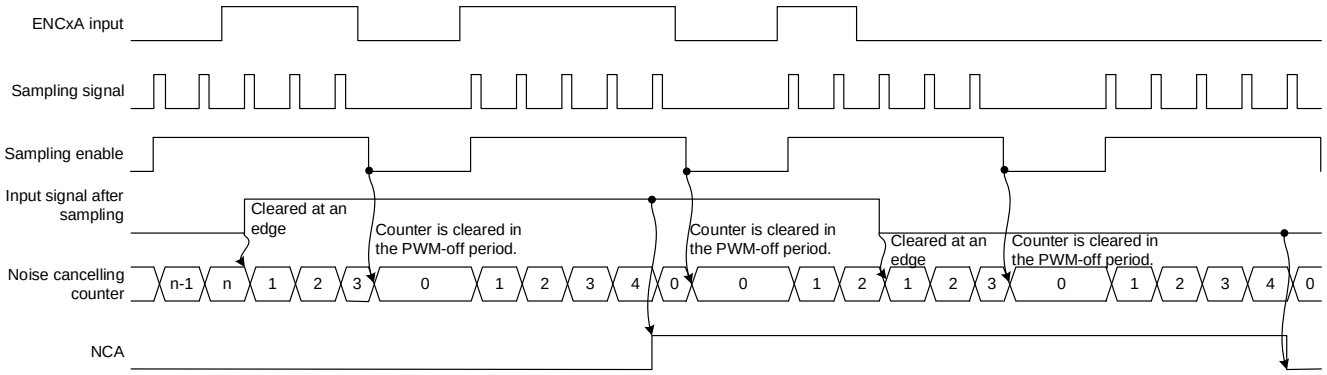

Figure 3.18 Noise Cancelling (PWM-on Period Sampling and PWM-off Period Clear: <NCT[6:0]> = 0x04)

3.3.2. Decoder

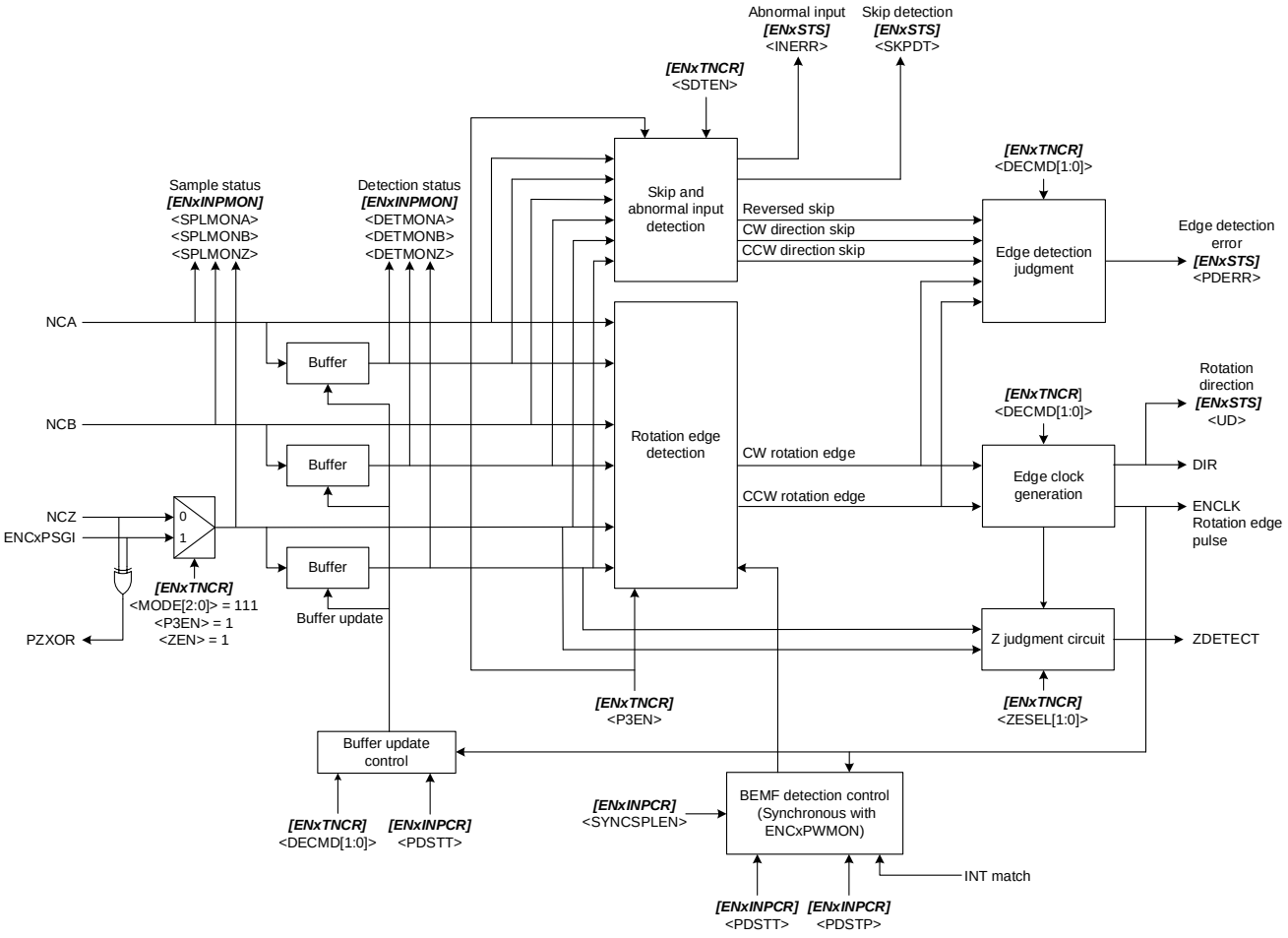

Figure 3.19 Decoder Circuit

The decoder detects the rotation edge and judges the rotation direction using the noise-canceled 2-phase or 3-phase input signals. It also detects ENCxZ in the encoder mode, and the edge of ENCxZ signal in the timer mode and the phase counter mode.

3.3.2.1. Rotation Edge Detection and Direction Signal Generation

(1) 2-phase decode (***[ENxTNCR]***<P3EN>=0)

The encoder mode and the sensor mode (2-phase input) are supported.

A change of input patterns (a rotation edge) among 4 patterns is detected in 2-phase decode.

CW direction input: The rotation edges of (1) → (2), (2) → (3), (3) → (4), and (4) → (1) are detected. Then ***[ENxSTS]***<UD> is set to "1".

CCW direction input: The rotation edges of (4) → (3), (3) → (2), (2) → (1), and (1) → (4) are detected. Then ***[ENxSTS]***<UD> is cleared to "0".

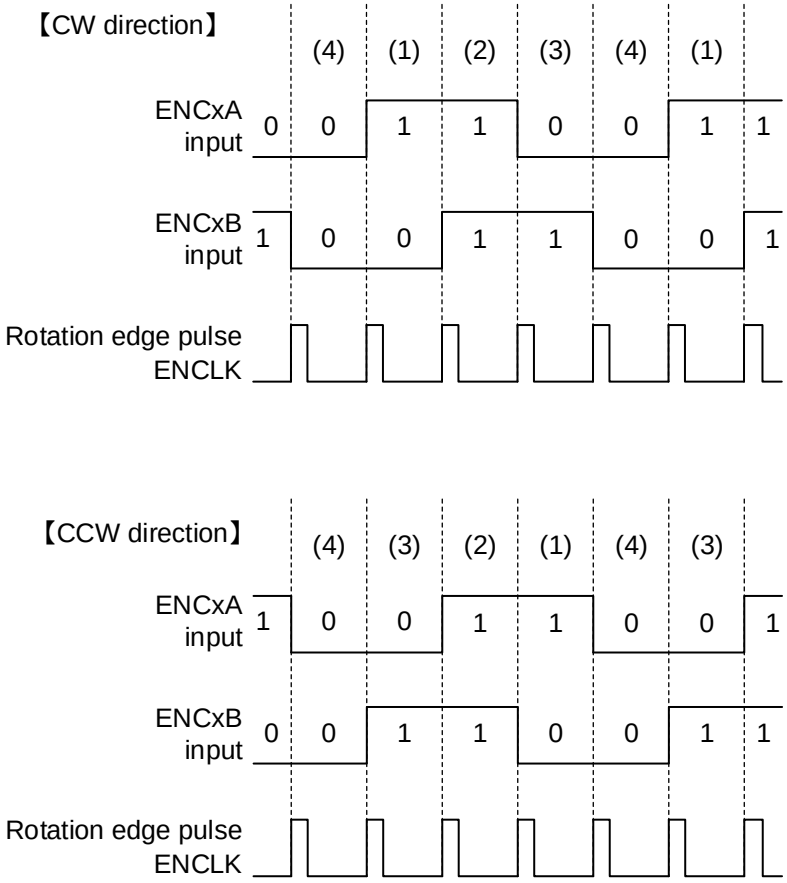

Figure 3.20 2-phase Decoder Waveform

(2) 3-phase decode (***[ENxTNCR]***<P3EN>=1)

The sensor mode (3-phase input) is supported.

A change of input patterns (a rotation edge) among 6 patterns is detected in 3-phase decode.

CW direction input: The rotation edges of (1) → (2), (2) → (3), (3) → (4), (4) → (5), (5) → (6), and (6) → (1) are detected. Then ***[ENxSTS]***<UD> is set to "1".

CCW direction input: The rotation edges of (6) → (5), (5) → (4), (4) → (3), (3) → (2), (2) → (1), and (1) → (6) are detected. Then ***[ENxSTS]***<UD> is cleared to "0".

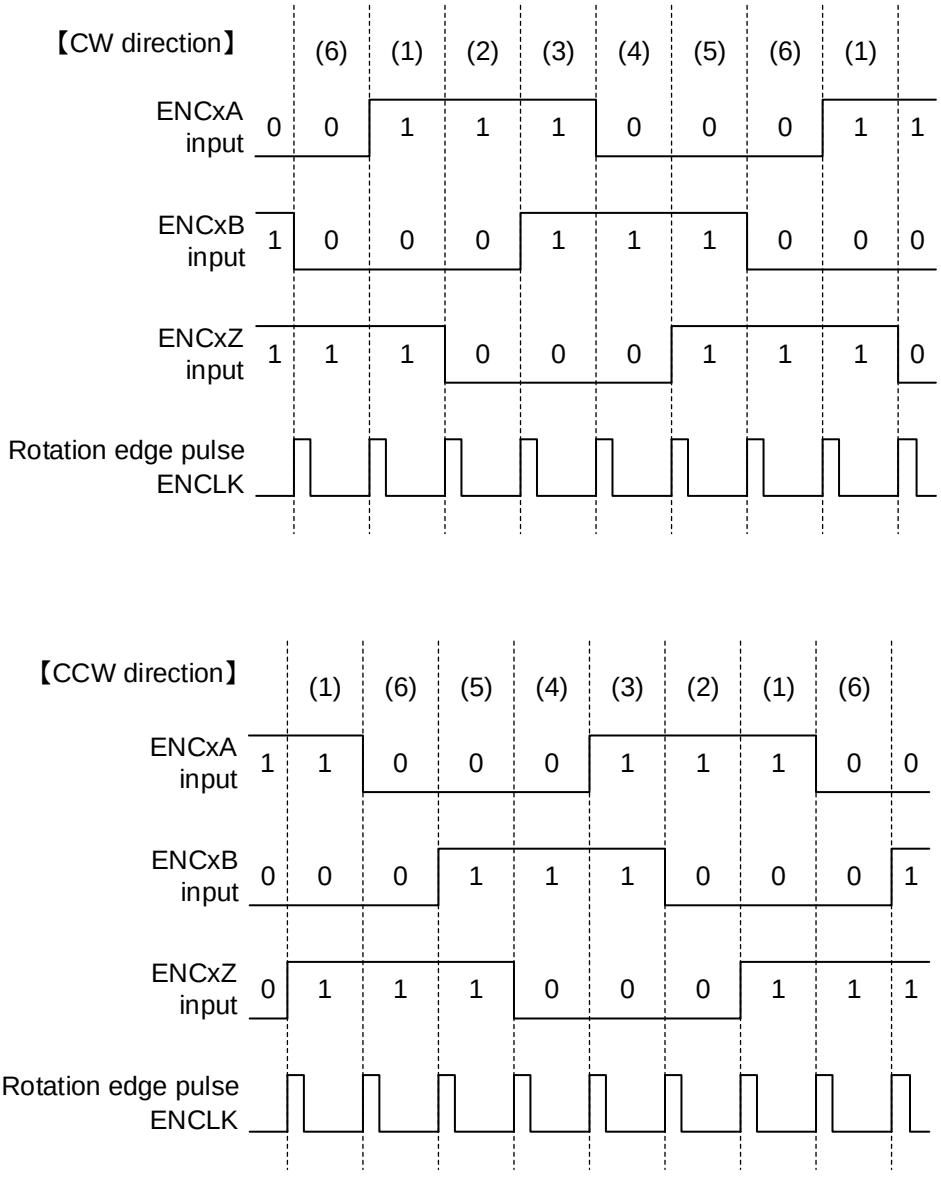

Figure 3.21 3-phase Decoder Waveform

3.3.2.2. Z Judgment Circuit

This circuit detects the edge of ENCxZ input signal.

- Encoder mode

  A rising edge is detected when ENCxA/ENCxB input is CW direction, and a falling edge is detected when the input is CCW direction.

  The input logic of the ENCxZ input can be selected with ***[ENxTNCR]***<ZEACT>.

- Timer mode and Phase counter mode

  The rising edge detection, the falling edge detection, and both edge detection can be selected by ***[ENxTNCR]***<ZESEL[1:0]>.

3.3.2.3. Skip Judgment and Abnormal Input Judgment

(1) Skip judgment

This function is valid when [ENxTNCR]<SDTEN> = 1.

- Skip detection in 2-phase decode (***[ENxTNCR]***<P3EN> = 0)

  Reversed skip detection: (1) → (3), (2) → (4), (3) → (1), and (4) → (2)

- Skip detection in 3-phase decode (***[ENxTNCR]***<P3EN>=1)

  CW direction skip detection: (1) → (3), (2) → (4), (3) → (5), (4) → (6), (5) → (1), and (6) → (2)
  CCW direction skip detection: (1) → (5), (2) → (6), (3) → (1), (4) → (2), (5) → (3), and (6) → (4)
  Reversed skip detection: (1) → (4), (4) → (1), (2) → (5), (5) → (2), (3) → (6), and (6) → (3)

- Combination that skip detection flag (***[ENxSTS]***<SKPDT>) is set to "1"

  CW direction skip detection: (1) → (3), (2) → (4), (3) → (5), (4) → (6), (5) → (1), and (6) → (2)
  CCW direction skip detection: (1) → (5), (2) → (6), (3) → (1), (4) → (2), (5) → (3), and (6) → (4)

(2) Abnormal input judgment

In the sensor mode (the event count, the timer count, or the phase count), when all 3 inputs change to "0" or "1" for 3-phase decode, the detected edges are judged as the abnormal input. Then ***[ENxSTS]***<INERR> is set to "1".

3.3.2.4. Edge Detection Error Judgment

When ***[ENxTNCR]***<DECMD[1:0]> sets a direction and an unset direction is detected, the detected direction is judged as an error. The error judgment can generate an interrupt. ***[ENxSTS]***<PDERR> is set to "1", when an error is detected.

- Skip detection disable (***[ENxTNCR]***<SDTEN> = 0)

  CW rotation edge detection (***[ENxTNCR]***<DECMD[1:0]> = 01): An error occurs at CCW rotation edge.
  CCW rotation edge detection (***[ENxTNCR]***<DECMD[1:0]> = 10): An error occurs at CW rotation edge.

- Skip detection enable (***[ENxTNCR]***<SDTEN>=1)

  CW rotation edge detection (***[ENxTNCR]***<DECMD[1:0]> = 01): An error occurs at CCW direction skip, Reversed skip, or CCW rotation edge.
  CCW rotation edge detection (***[ENxTNCR]***<DECMD[1:0]> = 10): An error occurs at CW direction skip, Reversed skip, or CW rotation edge.

3.3.2.5. Buffer Update Control

When ***[ENxTNCR]***<DECMD[1:0]> is set to "00", the buffer is always valid. The rotation edge judgment and the skip judgment are done by the change of the input signals.

When <DECMD[1:0]> is not "00", the buffer is updated only at the rotation edge detection. So, the edge judgment and the skip judgment are done by using the data at the previous rotation edge detection in the buffer (***[ENxINPMON]*** <DETMONA>, <DETMONB>, and <DETMONZ>) and the current input data (***[ENxINPMON]***<SPLMONA>, <SPLMONB>, and <SPLMONZ>).

3.3.2.6. BEMF Detection Control

In the sensor mode (the timer count and the phase count), this circuit is valid when PWM synchronous sampling is enabled (***[ENxINPCR]***<SYNCSPLEN> = 1). Then the rotation edge detection can be stopped (suspended) and started (resumed).

This control is used when the position detection (the position sensor-less control) is done using the induced voltage of BLDC motor (BEMF) which is driven with the pulse wave of a motor control circuit (PMD).

(1) Rotation edge detection start

- Command operation: ***[ENxINPCR]***<PDSTT> should be set to "1".
- Event operation: At match of INT comparison by a counter circuit

(2) Rotation edge detection stop

- Command operation: ***[ENxINPCR]***<PDSTP> should be set to "1".
- Event operation: At the rotation edge detection

3.3.3. Counter

The counter circuit consists of a clock generator, a counter, a comparison function, a capture function, and others. The used internal circuits depend on an operation mode.

3.3.3.1. Encoder Mode and Sensor Mode (Event Count)

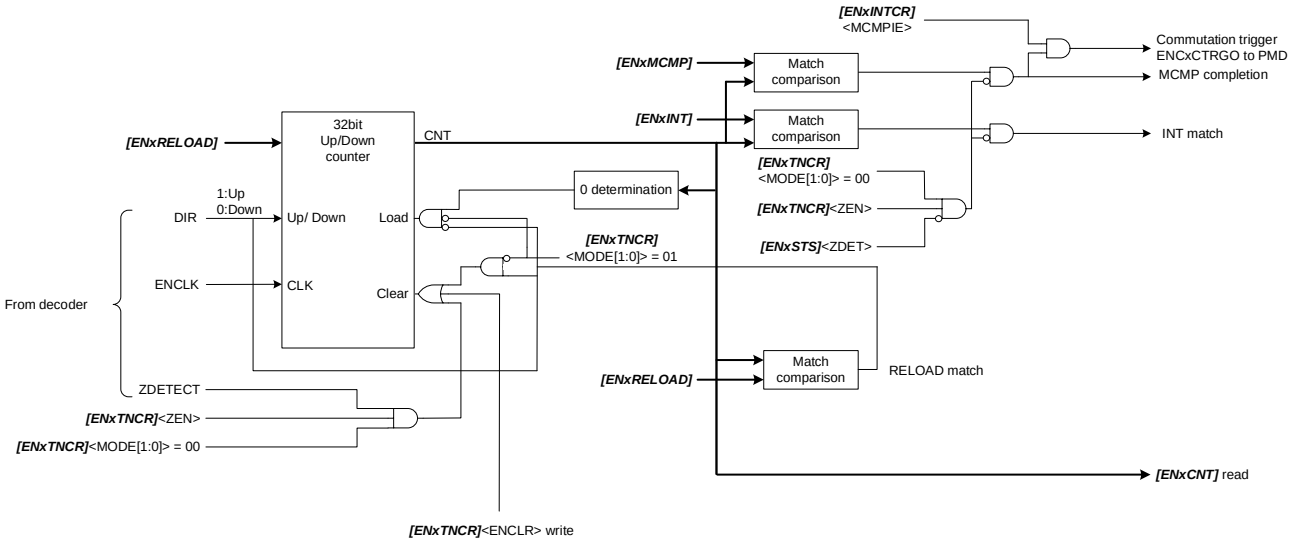

Figure 3.22 Counter Circuit (Encoder Mode and Sensor Mode (Event Count))

This circuit consists of 32-bit up- and down-counter which is driven by the rotation edge pulse (ENCLK) and the rotation direction signal (DIR) from the decoder, and 3 comparison functions (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***).

In the encoder mode, the counter is cleared at the match with ***[ENxRELOAD]***<RELOAD[31:0]> at CW rotation. And ***[ENxRELOAD]***<RELOAD[31:0]> value is loaded to the counter when the counter value becomes "0x00000000" at CCW rotation.

In the encoder mode, when Z detection enable (***[ENxTNCR]***<ZEN> = 1) is set, the matches with ***[ENxINT]***<INT[31:0]> and ***[ENxMCMP]***<MCMP[31:0]> are ignored till the first ENCxZ edge detection after the encoder input enable (***[ENxTNCR]***<ENRUN> = 1) is set.

The up- and down-counter value can be acquired by reading the counter register (***[ENxCNT]***<CNT[31:0]>).

When ***[ENxINTCR]***<MCMPIE> = 1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.3.2. Sensor Mode (Timer Count) and Timer Mode

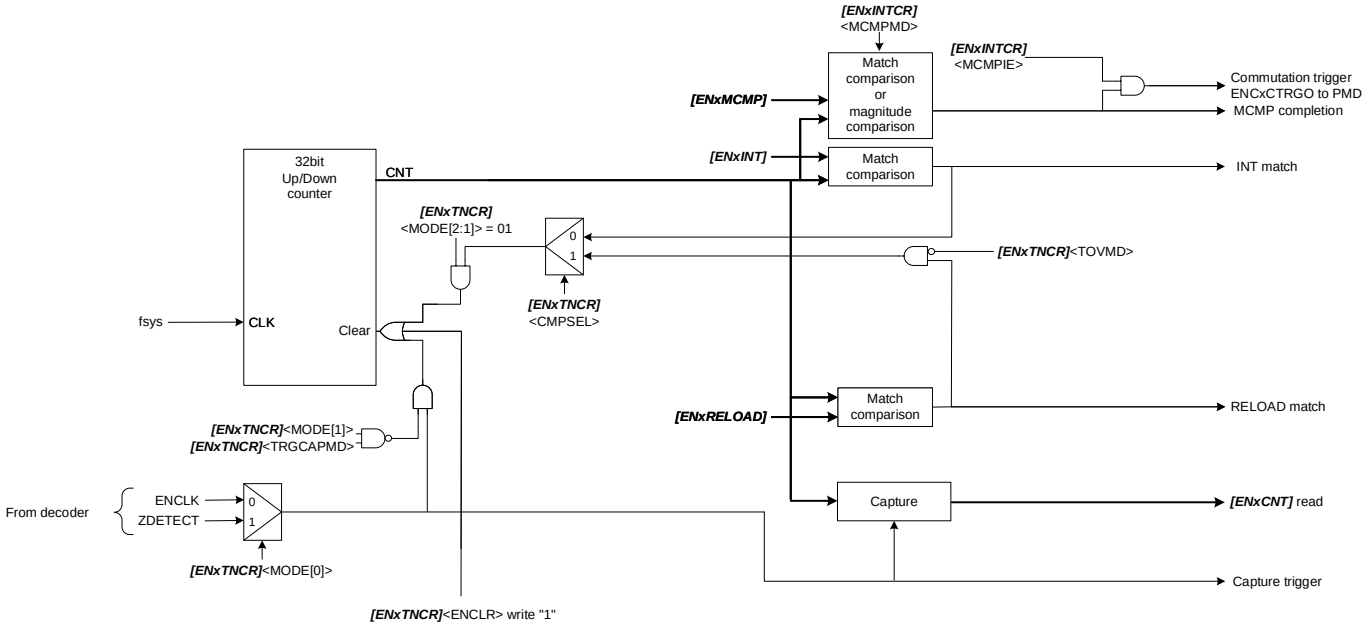

Figure 3.23 Counter Configuration (Sensor Mode (Timer Count) and Timer Mode)

This circuit consists of a 32-bit counter operating with the system clock (fsys), 3 comparison function circuits (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***), and a capture function circuit.

A match comparison and a magnitude comparison can be selected in MCMP comparison function. In the magnitude comparison (***[ENxTNCR]***<MCMPMD>=1), the comparison starts at the setting of ***[ENxMCMP]*** <MCMP[31:0]> and finishes when the condition is met and the MCMP match signal is generated.

In the timer mode, INT match or RELOAD match can clear the counter.

In the sensor mode (Timer count), the rotation edge detection (ENCLK) captures the counter value and clears the counter. In the timer mode, Z edge detection (ZDETECT) can capture the counter value and clear the counter. The captured value can be acquired by reading the counter register (***[ENxCNT]***<CNT[31:0]>).

When ***[ENxINTCR]***<MCMPIE> = 1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode

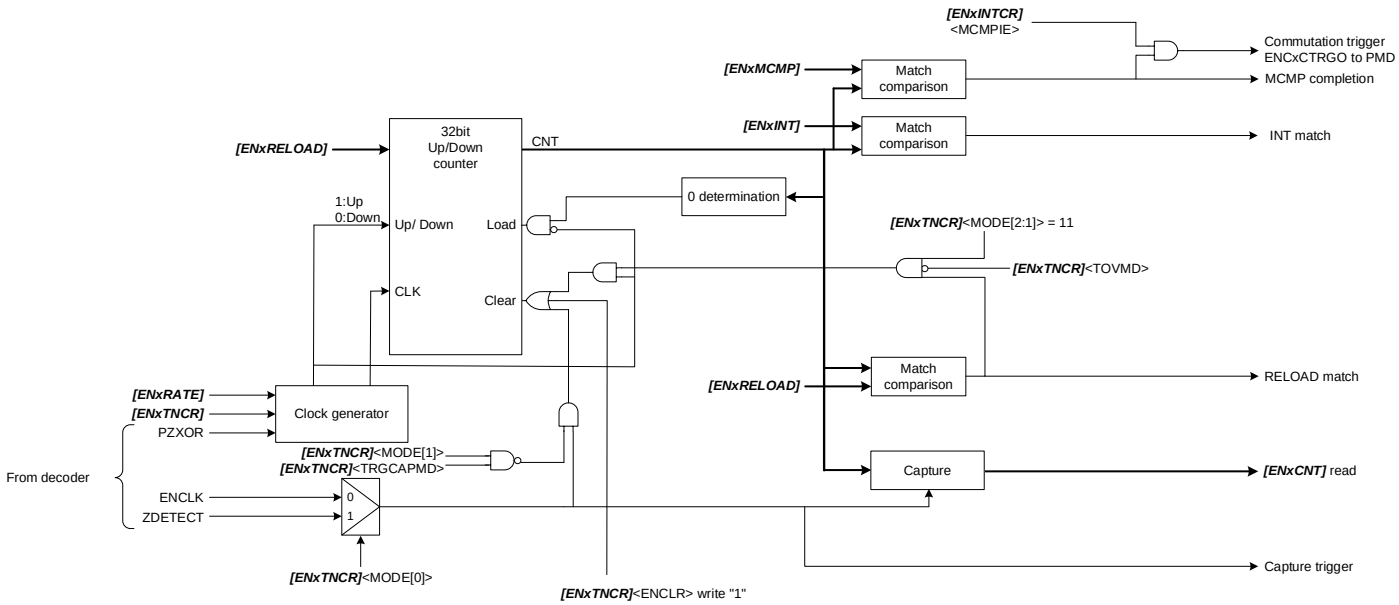

Figure 3.24 Counter Configuration (Sensor Mode (Phase Count) and Phase Counter Mode)

This circuit consists of a clock generator which generates the counter clock controlled by ***[ENxRATE]*** <RATE[15:0]> setting, a 16-bit up- and down-counter which operates with the clock signal and the direction signal from the clock generator, 3 match comparators (***[ENxRELOAD]***, ***[ENxINT]***, and ***[ENxMCMP]***), and a capture function circuit.

The counter clock settings are done in ***[ENxRATE]***<RATE[15:0]>.

The settings of the up- and down-counter are done in ***[ENxTNCR]***<UDMD>. In the phase counter mode (Phase difference measurement) (***[ENxTNCR]***<MODE[2:0]> = 111, <ZEN> = 1, and <P3EN> = 1), PZXOR signal controls the up- and down-counter.

When the up-count is set, RELOAD comparison match clears the counter, and when the down-count is set, "0x00000000" match loads the ***[ENxRELOAD]***<RELOAD[31:0]> value to the counter.

In the sensor mode (Phase count), the rotation edge detection (ENCLK) captures the counter value and clears the counter. In the phase counter mode, Z edge detection (ZDETECT) can capture the counter value and clear the counter. The captured value can be acquired by reading the counter register (***[ENxCNT]***<CNT[31:0]>).

When ***[ENxINTCR]***<MCMPIE> = 1 is set, MCMP comparison match signal can be used as the commutation trigger for PMD circuit.

3.3.4. Interrupt Control

There are 6 interrupt factors and 2 interrupt outputs. The output of the interrupt of each factor is enabled by Interrupt control register (***[ENxINTCR]***) individually. The factor generating the current interrupt can be checked in Interrupt flag register (***[ENxINTF]***).

A bit in Interrupt flag register (***[ENxINTF]***) is set by occurrence of the corresponding interrupt factor, and cleared by reading its register.

Table 3.2 List of the Interrupt Factors

Interrupt factor	Description	Mode	Interrupt enable *[ENxINTCR]*	Factor flag *[ENxINTF]*	Interrupt output
Division pulse	The frequency of the rotation edge pulse is divided by 1 to 128 according to ***[ENxTNCR]***<ENDEV[2:0]> setting. And the result pulse generation is notified.	Encoder mode Sensor mode (Event count)	<TPLSIE>	<TPLSF>	INTENCx0
Capture	This notifies that a capture is done by an external trigger (ENCxZ input).	Timer mode Phase counter mode	<CAPIE>	<CAPF>	INTENCx0
	This notifies that a capture is done by a rotation edge pulse (ENCLK).	Sensor mode (Timer count) Sensor mode (Phase count)			
Detection error	This notifies of occurrence of an edge detection error (***[ENxSTS]***<PDERR>) or a skip detection (***[ENxSTS]***<SKPDT>).	Encoder mode Sensor mode (Event count, Timer count and Phase count)	<ERRIE>	<ERRF>	INTENCx0
INT match	This notifies that the counter value matches ***[ENxINT]***<INT[31:0]> value.	All modes	<CMPIE>	<INTCPF>	INTENCx1
RELOAD match	This notifies that the counter value matches ***[ENxRELOAD]***<RELOAD[31:0]> value.	Sensor mode (Timer count and Phase count) Timer mode Phase counter mode (Phase measurement)	<RLDIE>	<RLDCPF>	INTENCx1
MCMP match	When ***[ENxTNCR]***<MCMPMD> = 0, this notifies that the counter value matches ***[ENxMCMP]***<MCMP[31:0]> value. When <MCMPMD> = 1, this notifies the counter value becomes ***[ENxMCMP]***<MCMP[31:0]> value or more.	Sensor mode (Timer count) Timer mode	<MCMPIE>	<MCMPF>	INTENCx1
	This notifies that the counter value matches ***[ENxMCMP]***<MCMP[31:0]> value.	Encoder mode Sensor mode (Event count and Phase count) Phase counter mode			

Table 3.3 List of Interrupt Factors in Each Mode

Mode	Interrupt factor
Encoder mode	Division pulse, Detection error, INT match, and MCMP match condition.
Sensor mode (Event count)	Division pulse, Detection error, INT match, and MCMP match condition
Sensor mode (Timer count)	Capture, Detection error, INT match, RELOAD match, and MCMP match condition
Sensor mode (Phase count)	Capture, Detection error, INT match, RELOAD match, and MCMP match condition
Timer mode	Capture, INT match, RELOAD match, and MCMP match condition
Phase counter mode	Capture, INT match, RELOAD match, and MCMP match condition

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following tables.

Peripheral function		Channel/Unit	Base address		
			TYPE1	TYPE2	TYPE3
Advanced Encoder Input Circuit (32-bit)	A-ENC32-A	ch0	0x400F7000	0x400EA000	0x4008A000
		ch1	-	0x400EA400	0x4008A400
		ch2	-	0x400EA800	0x4008A800
		ch3	-	0x400EAC00	0x4008AC00

Note: The channel/unit and base address type are different by products. Please refer to the reference manual "Product Information" for the details.

Register name		Address (Base+)
A-ENC32-A Control Register	***[ENxTNCR]***	0x0000
RELOAD Comparison Register	***[ENxRELOAD]***	0x0004
INT Comparison Register	***[ENxINT]***	0x0008
Counter Register	***[ENxCNT]***	0x000C
MCMP Comparison Register	***[ENxMCMP]***	0x0010
Phase Count Rate Register	***[ENxRATE]***	0x0014
Status Register	***[ENxSTS]***	0x0018
Input Procedure Control Register	***[ENxINPCR]***	0x001C
Sample Delay Register	***[ENxSMPDLY]***	0x0020
Input Monitor Register	***[ENxINPMON]***	0x0024
Sample Clock Control Register	***[ENxCLKCR]***	0x0028
Interrupt Control Register	***[ENxINTCR]***	0x002C
Interrupt Flag Register	***[ENxINTF]***	0x0030

Note: The registers which can be updated in operation are ***[ENxTNCR]***<SFTCAP>, <ENRUN>, and <ENCLR>, and ***[ENxINPCR]***<PDSTP> and <PDSTT>.
The other registers should not be updated in operation.

4.2. Details of Registers

For a special description in an operation mode is shown separately after **[xx mode]**.

4.2.1. *[ENxTNCR]* (A-ENC32-A Control Register)

Bit	Bit symbol	After reset	Type	Description
31:29	-	0	R	Read as "0".
28	CMPSEL	0	R/W	**[Timer mode]** Counter clear condition 0: ***[ENxINT]***<INT[31:0]> match 1: ***[ENxRELOAD]***<RELOAD[31:0]> match When <CMPSEL> = <TOVMD> = 1, the counter is not cleared. **[Encoder mode, Sensor mode (Phase count), and Phase counter mode]** ***[ENxRELOAD]***<RELOAD[31:0]> match at CW rotation, regardless of the setting of this bit **[Sensor mode (Event count and Timer count)]** The counter is not cleared by any comparison matches.
27:26	UDMD[1:0]	00	R/W	**[Sensor mode (Phase count), Phase counter mode (Phase measurement)]** Up-count or Down-count control 00: Up-count 01: Down-count 10, 11: Up- and down-count are controlled by ***[ENxRATE]*** <RATE[15:0]>. When this field is set to "10" or "11", the setting value in ***[ENxRATE]***<RATE[15:0]> becomes 2-complementary. The value in ***[ENxRATE]***<RATE[15:0]> < 0 makes down-count, and value in ***[ENxRATE]***<RATE[15:0]> ≥ 0 makes up-count. **[Encoder mode, Sensor mode (Event count) and Phase counter mode (Phase difference measurement)]** Auto judgment is done (refer to "3.3.2.1 Rotation Edge Detection and Direction Signal Generation"). **[Sensor mode (Timer count) and Timer mode]** Up-count is done.

Bit	Bit symbol	After reset	Type	Description
25	TOVMD	0	R/W	Operation setting at RELOAD match **[Sensor mode (Timer count)]** 0: Count continues. 1: Count stops. If the counter should be operated from the stop state, the match state should be released by the software clear. **[Timer mode, Sensor mode (Phase count), and Phase counter mode (Phase measurement)]** 0: Counter is cleared and continues the count. 1: Counter stops. If the counter should be operated from the stop state, the match state should be released by the software clear. **[Encoder mode, Sensor mode (Event count) and Phase counter mode (Phase difference measurement)]** This bit cannot be used. In Encoder mode, regardless of <TOVMD> setting, CW direction: Counter is cleared and continues the count. CCW direction: Counter continues the count. In Sensor mode (Event count) and Phase counter mode (Phase difference measurement), RELOAD match cannot be used.
24	MCMPMD	0	R/W	**[Sensor mode (Timer count) and Timer mode]** Comparison mode of ***[ENxMCMP]*** register 0: Match comparison (***[ENxMCMP]***<MCMP[31:0]> = Counter value) 1: Magnitude comparison (***[ENxMCMP]***<MCMP[31:0]> ≤ Counter value) The magnitude comparison is available only for the up-counter. **[Encoder mode, Sensor mode (Event count and Phase count), and Phase counter mode]** The MCMP comparison is a match comparison regardless of the setting.
23:22	DECMD[1:0]	00	R/W	**[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** Selection of Decoder detection direction 00: CW or CCW rotation edge detection The changes of the input signals (ENCxA, ENCxB, and ENCxZ) are detected. 01: CW Rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detected result is kept.) 10: CCW rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detected result is kept.) 11: CW or CCW rotation edge detection Changes of the input signals from the previous rotation edge detection are detected. (The detection result is kept.) **[Timer mode and Phase counter mode]** <DECMD[1:0]> should be set to "00".

Bit	Bit symbol	After reset	Type	Description
21	SDTEN	0	R/W	**[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** Skip detection 0: Detection disable 1: Detection enable For the details, refer to "3.3.2.3. Skip Judgment and Abnormal Input Judgment". <SDTEN> should be cleared to "0" in other mode.
20	-	0	R	Read as "0".
19:17	MODE[2:0]	000	R/W	Operation mode setting 000: Encoder mode 001: Sensor mode (Event count) 010: Sensor mode (Timer count) 011: Timer mode 100: Reserved 101: Reserved 110: Sensor mode (Phase count) 111: Phase counter mode In Phase counter mode, when <ZEN> = <P3EN> = 1, the operation mode becomes "Phase difference measurement". There are 13 operation modes. The operation mode is determined by <MODE[2:0]>, <P3EN>, and <ZEN> (Refer to "Table 3.1 Operation Modes").
16	P3EN	0	R/W	**[Sensor mode (Event count, Timer count and Phase count)]** Decode mode setting (2-phase/3-phase input selection) 0: 2-phase decode 1: 3-phase decode **[Phase counter mode (Phase difference measurement)]** Set <ZEN> and <P3EN> to "1". **[Encoder mode, Timer mode and Phase counter mode (Phase measurement)]** <P3EN> should be cleared to "0". (Refer to "Table 3.1 Operation Modes Operation Modes").
15:13	-	0	R	Read as "0".
12	TRGCAPMD	0	R/W	**[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** Trigger capture operation selection Operation selection for the capture by the rotation edge pulse and ENCxZ input 0: Capture and counter clear 1: Only capture This bit selects the trigger capture operation at the rotation edge detection in the sensor mode (Timer count and Phase count), and at ENCxZ input enable in Timer mode and Phase counter mode. The counter is not cleared by the software capture. **[Encoder mode and Sensor mode (Event count)]** Capture is not performed.

Bit	Bit symbol	After reset	Type	Description
11	SFTCAP	0	W	**[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** Software capture execution 0: No meaning 1: The counter value is captured. When this bit is set to "1", the counter value is captured. ***[ENxCNT]***<CNT[31:0]> should be read to acquire the captured value. Read as "0". **[Encoder mode and Sensor mode (Event count)]** <SFTCAP> should be cleared to "0".
10	ENCLR	0	W	Counter clear 0: No meaning 1: Clear When this bit is set to "1", the counter is cleared to "0x00000000". The counter operates after the clear. Read as "0". <SFTCAP> and <ENCLR> should not be set to "1" at the same time.
9:8	ZESEL[1:0]	00	R/W	**[Timer mode and Phase counter mode]** This field selects the detection edge in ENCxZ input enable (<ZEN>=1). (ENCxZ input/ENCxPSGI input) 00: Reserved 01: Rising edge detection 10: Falling edge detection 11: Both edge detection The detection target is ENCxPSGI input in the phase difference measurement. **[Encoder mode and Sensor mode (Event count, Timer count and Phase count)]** <ZESEL[1:0]> should be set to "00".
7	ZEN	0	R/W	**[Encoder mode, Timer mode, and Phase counter mode (Phase measurement)]** ENCxZ input enable 0: ENCxZ input disable 1: ENCxZ input enable **[Phase counter mode (Phase difference measurement)]** Set <P3EN> and <ZEN> to "1". **[Sensor mode (Event count and Timer count and Phase count)]** <ZEN> should be cleared to "0". (Refer to "Table 3.1 Operation Modes").
6	ENRUN	0	R/W	Encoder input circuit enable 0: Disable 1: Enable

Bit	Bit symbol	After reset	Type	Description
5	ZEACT	0	R/W	**[Encoder mode]** ENCxZ active level selection 0: H active input (Positive logic) 1: L active input (Negative logic) This bit is valid when ENCxZ input is enabled (<ZEN>=1) in Encoder mode. **[Sensor mode (Event count, Timer count, and Phase count), Timer mode, and Phase counter mode]** High active input (Positive logic) is selected regardless of <ZEACT> value.
4:3	-	0	R	Read as "0".
2:0	ENDEV[2:0]	000	R/W	**[Encoder mode and Sensor mode (Event count)]** The division ratio of the division signal of the rotation edge pulse (ENCxTIMPLS) The frequency of the rotation edge pulse is divided according to the setting and the output signal is used as an interrupt factor. 000: 1-division 100: 16-division 001: 2-division 101: 32-division 010: 4-division 110: 64-division 011: 8-division 111: 128-division **[Sensor mode (Timer count and Phase count), Timer mode, and Phase counter mode]** There is no division output.

Note: When setting <ENRUN> = 1, do not change other bits at the same time. Operation settings other than <ENRUN> must be set before setting <ENRUN> = 1.

4.2.2. *[ENxRELOAD]* (RELOAD Comparison Register)

Bit	Bit symbol	After reset	Type	Description
31:0	RELOAD[31:0]	0x00000000	R/W	**[Encoder mode]** Sets the maximum value of the counter. ***[ENxTNCR]***<ZEN> = 1: Set "Number of input pulses per rotation" × 4. ***[ENxTNCR]***<ZEN> = 0: Set "Number of input pulses per rotation" × 4 -1 **[Sensor mode (Phase count) and Phase counter mode (Phase measurement)]** The maximum value of the counter (the count range per rotation) is set. When ***[ENxINTCR]***<RLDIE> = 1, a RELOAD match generates an INTENCx1 interrupt. **[Sensor mode (Timer count) and Timer mode]** This register is used as a comparison register with the counter value. When ***[ENxINTCR]***<RLDIE> = 1, a RELOAD match generates an INTENCx1 interrupt. **[Sensor mode (Event count) and Phase counter mode (Phase difference measurement)]** This register is not used.

4.2.3. *[ENxINT]* (INT Comparison Register)

Bit	Bit symbol	After reset	Type	Description
31:0	INT[31:0]	0x00000000	R/W	**[Encoder mode]** When the counter value matches this value, ***[ENxINTF]***<INTCPF> is set to "1". When ***[ENxINTCR]***<CMPIE> = 1, INTENCx1 interrupt occurs. When ***[ENxTNCR]***<ZEN> = 1, however, no interrupt occurs before ***[ENxSTS]***<ZDET> becomes "1". **[Sensor mode (Event count, Timer count), Timer mode]** When the counter value matches this value, <INTCPF> is set to "1". When <CMPIE> = 1, INTENCx1 interrupt occurs. **[Sensor mode (Phase count) and Phase counter mode]** When the counter value matches this value, <INTCPF> is set to "1" at the next count. When <CMPIE> = 1, INTENCx1 interrupt occurs When ***[ENxTNCR]***<TOVMD> = 1, which stops the counter at RELOAD match, INTENCx1 interrupt will not occur if <INT[31:0> setting value is the same as the ***[ENxRELOAD]***<RELOAD[31:0]> value.

Note: In sensor mode (phase count, timer count), it is used for BEMF control (Refer to "3.3.2.6. BEMF Detection Control").

4.2.4. *[ENxCNT]* (Counter Register)

Bit	Bit symbol	After reset	Type	Description
31:0	CNT[31:0]	0x00000000	R	**[Encoder mode and Sensor mode (Event count)]** The counter value of the rotation edge pulses can be read. **[Sensor mode (Timer count and Phase count)]** The captured value of the internal counter by the rotation edge pulse (ENCLK) can be read. Or the captured value of the internal counter by writing ***[ENxTNCR]***<SFTCAP> to "1" in software can be read. **[Timer mode and Phase counter mode (Phase measurement)]** <SFTCAP> should be set to "1" to read the software-captured value of the internal counter. When ***[ENxTNCR]***<ZEN> = 1, the capture is also done by the edge of ENCxZ (ZDETECT timing) set by ***[ENxTNCR]***<ZESEL[1:0]>. **[Phase counter mode (Phase difference measurement)]** The software-captured value of the internal counter by writing <SFTCAP> to "1" can be read. The capture is also done by the edge of ENCxPSGI (ZDETECT timing) set by <ZESEL[1:0]>.

4.2.5. *[ENxMCMP]* (MCMP Comparison Register)

Bit	Bit symbol	After reset	Type	Description
31:0	MCMP[31:0]	0x00000000	R/W	**[Sensor mode (Timer count) and Timer mode]** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1". When ***[ENxINTCR]*** <MCMPIE> = 1, INTENCx1 interrupt occurs. Magnitude comparison mode (***[ENxTNCR]***<MCMPMD> = 1) When <MCMP[31:0]> ≥ counter value is met, one pulse is generated. Only one pulse is generated per writing to the register. Match comparison mode (***[ENxTNCR]***<MCMPMD> = 0) When <MCMP[31:0]> matches counter value, the match signal is generated. **[Encoder mode and Sensor mode (Event count)]** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]*** <MCMPIE> = 1, INTENCx1 interrupt is generated. **[Sensor mode (Phase count) and Phase counter mode]** When the comparison condition with the counter value is met, ***[ENxINTF]***<MCMPF> is set to "1".When ***[ENxINTCR]*** <MCMPIE> = 1, INTENCx1 interrupt occurs. When it is set that RELOAD match counter stops at ***[ENxTNCR]***<TOVMD> = 1, do not set <MCMP> = ***[ENxRELOAD]***<RELOAD[31:0]>.

Note: When the comparison mode of ***[ENxMCMP]*** register is set to the magnitude comparison in Sensor mode (Timer count) or Timer mode, if ***[ENxMCMP]***<MCMP[31:0]> value is updated at the same time immediately MCMP comparison is met, MCMP comparison met interrupt does not occur by the updated ***[ENxMCMP]*** value. MCMP comparison met flag ***[ENxINTF]***<MCMPIF> is not set, either.

4.2.6. *[ENxRATE]* (Phase Count Rate Register)

Bit	Bit symbol	After reset	Type	Description
31:16	-	0	R	Read as "0".
15:0	RATE[15:0]	0x0000	R/W	**[Sensor mode (Phase count) and Phase counter mode]** The count frequency of the counter is set. Generated clock frequency: fsys × <RATE[15:0]> /2^{16} By ***[ENxTNCR]***<UDMD> setting, the sign of <RATE[15:0]> setting value can be selected. When the value is negative, the counter decrements. <UDMD> = 0x: Without a sign. 0 and more/Less than 1.0 ("0x0000" to "0xFFFF") <UDMD> = 1x: With a sign. -0.5 and more/Less than 0.5 ("0x8000" to "0x7FFF", two's complement) When <RATE[15:0]> = 0x0000, ***[ENxCNT]***<CNT[31:0]> does not count. **[Encoder mode, Sensor mode (Event count and Timer count), and Timer mode]** This register is not used.

4.2.7. *[ENxSTS]* (Status Register)

Bit	Bit symbol	After reset	Type	Description
31:15	-	0	R	Read as "0".
14	REVERR	0	R	**[Sensor mode (Timer count and Phase count)]** The reversed <UD> flag at both direction detection (Note1) (Note2) 0: - 1: Reversed <UD> is generated. When ***[ENxTNCR]***<ENRUN> is "0", this bit is always cleared to "0". After <ENRUN> is set to "1", <REVERR> is not set by the first rotating edge pulse (ENCLK). In Encoder mode, Sensor mode (Event count), Timer mode and Phase counter mode, this bit means nothing.
13	UD	0	R	**[Encoder mode, Sensor mode (Event count, Timer count, and Phase count)]** Rotation direction judgment 0: CCW direction (Counter-clockwise) 1: CW direction (Clockwise) When a motor rotates in CW direction, this bit is set to "1", and, in CCW direction, cleared to "0". When ***[ENxTNCR]***<ENRUN> = 0, <UD> is always cleared to "0".
12	ZDET	0	R	**[Encoder mode]** ENCxZ input pass detection 0: ENCxZ input has not been detected after the encoder input is enabled. 1: ENCxZ input has been detected. This bit is cleared by ***[ENxTNCR]***<ENRUN> = 0.
11:3	-	0	R	Read as "0".
2	SKPDT	0	R	**[Sensor mode (Event count, Timer count, and Phase count)]** Skip detection flag at Skip detection enable (Note1) 0: No detection 1: Skip detection
1	PDERR	0	R	**[Encoder mode, Sensor mode (Event count, Timer count, and Phase count)]** Edge detection error flag (Note1) 0: No detection. 1: Error is detected.
0	INERR	0	R	**[Sensor mode (Event count, Timer count, and Phase count)]** Abnormal input detection (Note1) 0: Abnormal input has not been detected. 1: Abnormal input has been detected. In 3-phase decode operation, 3 phase inputs are detected as all Low or all High, this bit is set to "1".

Note1: When the register is read, the flag is cleared.

Note2: After an operation mode (***[ENxTNCR]***<MODE[2:0]>) is updated, this register should be read to clear the flags to "0" at first.

4.2.8. *[ENxINPCR]* (Input Procedure Control Register)

Bit	Bit symbol	After reset	Type	Description
31:15	-	0	R	Read as "0".
14:8	NCT[6:0]	0x00	R/W	Noise cancellation time (Note1) Setting range: 0 to 127 (0x00 to 0x7F) Cancellation time: Setting value × Sample clock cycle (depend on ***[ENxCLKCR]***<SPLCKS[1:0]> setting) When "0" is set, the noise cancellation does not operate (the circuit is bypassed). The sampling clock is PWM signal (ENCxPWMON) in PWM-off edge sample mode.
7	PDSTP	0	W	**[Sensor mode (Timer count and Phase count)]** The rotation edge detection stop command (BEMF detection control) at PWM synchronous sampling. 0: No meaning 1: Rotation edge detection stop When this bit is set to "1", the rotation edge detection stops. Read as "0". <PDSTP> and <PDSTT> should not be set to "1" at the same time.
6	PDSTT	0	W	**[Sensor mode (Timer count and Phase count)]** The rotation edge detection start command (BEMF detection control) at PWM synchronous sampling. 0: No meaning 1: Rotation edge detection start When this bit is set to "1", the rotation edge detection starts. Read as "0". <PDSTP> and <PDSTT> should not be set to "1" at the same time.
5:3	-	0	R	Read as "0".
2	SYNCNCZEN	0	R/W	Noise cancellation counter control at PWM-on period sampling 0: PWM-off period counter stop 1: PWM-off period counter stop and clear This bit is valid at PWM-on period sampling selection (<SYNCSPLMD> = 0) and PWM synchronous sampling enable (<SYNCSPLEN> = 1).
1	SYNCSPLMD	0	R/W	PWM synchronous sampling selection 0: PWM-on period sampling 1: PWM-off edge sampling This bit is valid at PWM synchronous sampling enable (<SYNCSPLEN> = 1).
0	SYNCSPLEN	0	R/W	PWM synchronous sampling enable 0: Continuous sampling 1: PWM synchronous sampling (Note1) The sampling synchronous with PWM signal in PMD circuit (ENCxPWMON) is done. (Note2) When <SYNCSPLEN> is "1" in Sensor mode (Timer count and Phase count), BEMF detection control is valid in the decode operation.

Note1: When PWM synchronous sampling (<SYNCSPLEN>=1), <NCT[6:0]> should be set to "1" or more.

Note2: For the details of PMD circuit, refer to Reference manual "Programmable Motor Control Circuit Plus" or "Advanced Programmable Motor Control Circuit".

4.2.9. *[ENxSMPDLY]* (Sample Delay Register)

Bit	Bit symbol	After reset	Type	Description
31:8	-	0	R	Read as "0".
7:0	SMPDLY[7:0]	0x00	R/W	Sampling start delay time Setting range: "0" to "255" ("0x00" to "0xFF") Delay time: Setting value × Sampling cycle (by ***[ENxCLKCR]***<SPLCKS[1:0]> setting) This field sets the delay time from PWM-on to the first sampling start in the PWM-on period sampling (***[ENxINPCR]*** <SYNCSPLEN> = 1 and ***[ENxINPCR]***<SYNCSPLMD> = 0).

Note: After A-ENC32-A is enabled (after changing ***[ENxTNCR]***<ENRUN> from "0" to "1"), the first delay time may be different from the <SMPDLY[7:0]> setting value.

4.2.10. *[ENxINPMON]* (Input Monitor Register)

Bit	Bit symbol	After reset	Type	Description
31:7	-	0	R	Read as "0".
6	DETMONZ	0	R	Monitor of NCZ rotation edge detection status (Note1) (Note2) NCZ value at the rotation edge detection is stored.
5	DETMONB	0	R	Monitor of NCB rotation edge detection status (Note1) (Note2) NCB value at the rotation edge detection is stored.
4	DETMONA	0	R	Monitor of NCA rotation edge detection status (Note1) (Note2) NCA value at the rotation edge detection is stored.
3	-	0	R	Read as "0".
2	SPLMONZ	0	R	ENCxZ status after the noise cancellation Status of the signal of the noise-cancelled ENCxZ input (NCZ)
1	SPLMONB	0	R	ENCxB status after the noise cancellation Status of the signal of the noise-cancelled ENCxB input (NCB)
0	SPLMONA	0	R	ENCxA status after the noise cancellation Status of the signal of the noise-cancelled ENCxA input (NCA)

Note1: This bit is valid when ***[ENxTNCR]***<DECMD[1:0]> is not "00". When <DECMD[1:0]> = 00, this bit shows <SPLMONn> value (n = A, B, or Z) in the previous cycle.

Note2: Even when ***[ENxTNCR]***<ENRUN> is updated to "1" or ***[ENxINPCR]***<PDSTT> is set to "1", this bit shows <SPLMONn> value (n = A, B, or Z) in the previous cycle until the first rotation edge is detected.

4.2.11. *[ENxCLKCR]* (Sample Clock Control Register)

Bit	Bit symbol	After reset	Type	Description
31:2	-	0	R	Read as "0".
1:0	SPLCKS[1:0]	00	R/W	Sampling frequency 00: fsys 01: fsys / 2 10: fsys / 4 11: fsys / 8 The sampling frequency is selected for ENCxA, ENCxB, and ENCxZ inputs. This field is not valid when PWM-off edge sampling (***[ENxINPCR]*** <SYNCSPLEN> = 1 and ***[ENxINPCR]***<SYNCSPLMD> = 1) in PWM synchronous sampling.

4.2.12. *[ENxINTCR]* (Interrupt Control Register)

Bit	Bit symbol	After reset	Type	Description
31:6	-	0	R	Read as "0".
5	MCMPIE	0	R/W	MCMP match interrupt enable 0: Disable 1: Enable When <MCMPIE> is set to "1", INTENCx1 interrupt occurs by MCMP match.
4	RLDIE	0	R/W	RELOAD match interrupt enable 0: Disable 1: Enable When <RLDIE> is set to "1", INTENCx1 interrupt occurs by RELOAD matches. In Encoder mode and Sensor mode (Event count), the interrupt does not occur.
3	CMPIE	0	R/W	INT match interrupt enable 0: Disable 1: Enable When <CMPIE> is set to "1", INTENCx1 interrupt occurs by INT matches.
2	ERRIE	0	R/W	Detection error interrupt enable 0: Disable 1: Enable When <ERRIE> is set to "1", INTENCx0 interrupt occurs by the edge detection error (***[ENxSTS]*** <PDERR>) or the skip detection (***[ENxSTS]***<SKPDT>). In Timer mode and Phase counter mode, the interrupt does not occur.
1	CAPIE	0	R/W	Capture trigger interrupt enable 0: Disable 1: Enable When <CAPIE> is set to "1", INTENCx0 interrupt occurs by the external trigger (ENCxZ input) or capturing the counter value at the rotation edge pulse (ENCLK). In Encoder mode and Sensor mode (Event count), the interrupt does not occur.
0	TPLSIE	0	R/W	Rotation edge division interrupt enable 0: Disable 1: Enable When <TPLSIE> is set to "1", INTENCx0 interrupt occurs by a rotation edge division pulse. In the other modes than Encoder mode and Sensor mode (Event count), the interrupt does not occur.

4.2.13. *[ENxINTF]* (Interrupt Flag Register)

Bit	Bit symbol	After reset	Type	Description
31:6	-	0	R	Read as "0".
5	MCMPF	0	R	MCMP comparison met flag 0: Not generated 1: Generated
4	RLDCPF	0	R	RELOAD match flag 0: Not generated 1: Generated In Encoder mode and Sensor mode (Event count), this bit is not set.
3	INTCPF	0	R	INT match flag 0: Not generated 1: Generated
2	ERRF	0	R	Detection error flag 0: Not generated 1: Generated In Timer mode and Phase counter mode, this bit is not set.
1	CAPF	0	R	Capture flag 0: Not generated. 1: Generated This bit is not set by the software capture. In Encoder mode and Sensor mode (Event count), this bit is not set.
0	TPLSF	0	R	Rotation edge division pulse flag 0: Not generated 1: Generated This bit is valid in Encoder mode and Sensor mode (Event count).

Note: Each flag is set by the occurrence of the enabled factor, and cleared by reading ***[ENxINTF]*** register. When ***[ENxTNCR]***<ENRUN> = 0, the flags are cleared to "0".

5. Precaution for Usage

- Before the clock supply is shut down, it should be checked that A-ENC32-A has stopped. And, before the operation mode is changed to the stop mode, it should be checked that A-ENC32-A has stopped.

6. Revision History

Table 6.1 Revision history

Revision	Date	Description
1.0	2018-06-18	First release
1.1	2018-10-11	- Conventions Modified explanation of trademark - 2. Configuration Figure 2.1: "Encoder input circuit"→"ENC" - 3.2.1. Encoder Mode "incremental encoder input" → "incremental encoder" - 3.3.3.3. Sensor Mode (Phase Count) and Phase Counter Mode Corrected Figure 3.24 "***[ENxRATE]***<RATE>" → "***[ENxRATE]***" - 3.3.4. Interrupt Control Corrected Table 3.2. "PDERR" → "***[ENxSTS]***<PDERR> " "SKPDT" → "***[ENxSTS]***<SKPDT>" - 4.2.1. ***[ENxTNCR]*** (ENC Control Register) Changed the expression of "Note". - RESTRICTIONS ON PRODUCT USE Replaced to Newer one.
1.2	2021-11-22	- Add bit range to registers. - "ENC" is changed to "A-ENC32-A". - Preface Modified trademark description Modified Terms and Abbreviations - 3.1. Clock Supply Add fsys supply stop register C to explanation. - 3.2.1. Encoder Mode (2) Changed the expression. - 3.2.2.1. Event Count (2) Changed the expression. - 3.3.1.2. Sampling Mode (2) Add name of PWM signal. - 3.3.2.2. Z Judgement Circuit Correct register name from "***[ENxTNCR]***<ZACT>" to "***[ENxTNCR]*** <ZEACT>". - 3.3.2.3 Skip Judgment and Abnormal Input Judgment Add "Combination that skip detection flag (***[ENxSTS]***<SKPDT>) is set to "1" ". - 3.3.2.4. Edge Detection Error Judgment Add "***[ENxSTS]***<PDERR> is set to "1", when an error is detected.". - 4.2.3. ***[ENxINT]*** (INT Comparison Register) Changed the expression for INT[31:0]. Add Note. - 4.2.7. ***[ENxSTS]*** (Status Register) Change the explanation for <REVERR>. - 4.2.9. ***[ENxSMPDLY]*** (Sample Delay Register) Correct the explanation for <SMPDLY[7:0]>.
1.3	2022-05-17	- Figure 2.1 Added fsys. Added connection from ***[ENxTNCR]*** to input circuit. Changed from "MCMP is met" to "MCMP match". - Table 2.1 Correction of errors - Figure 3.22 ZDETECT changed to "from decode". - Changed from "CTRGO" in Figure 3.22, Figure 3.23, and Figure 3.24 to "ENCxCTRGO". - Figure 3.23 Changed from "Match comparison" to "Match comparison or Magnitude comparison". Changed from "***[ENxTNCR]***<MODE[2:1]>=11" to "***[ENxTNCR]***<MODE[2:1]>=01" .
1.4	2023-01-17	- 1. Outline Changed from "The maximum count number per cycle is 232." to "The maximum count number per cycle is 2^{32}."
1.5	2024-10-31	- Appearance updated

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**