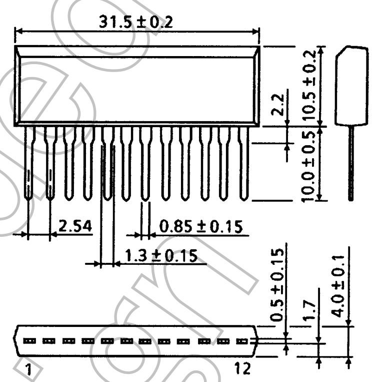
TOSHIBA Power MOS FET Module Silicon N&P Channel MOS Type (Six L^2-π-MOSV inOne)

MP6404

Industrial Applications

High Power High Speed Switching Applications
3-Phase Motor Drive and Stepping Motor Drive Applications

Unit: mm



2, 4, 6, 8, 9, 11	GATE
3, 7, 10	DRAIN
1, 5, 12	SOURCE

JEDEC	—
JEITA	—
TOSHIBA	2-32C1K

Weight: 3.9 g (typ.)

- 4-V gate drivability
- Small package by full molding (SIP 12 pins)
- High drain power dissipation (6-device operation)
  : P_T = 36 W (Tc = 25°C)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 120 mΩ (typ.) (Nch)
  160 mΩ (typ.) (Pch)
- High forward transfer admittance: $|Y_{fs}|$ = 5.0 S (typ.) (Nch)
  4.0 S (typ.) (Pch)
- Low leakage current: I_{GSS} = ±10 μA (max) (V_{GS} = ±16 V)
  I_{DSS} = 100 μA (max) (V_{DS} = 60 V)
- Enhancement-mode: V_{th} = 0.8 V to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating		Unit
			Nch	Pch	
Drain-source voltage		V_{DSS}	60	−60	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	60	−60	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	DC	I_D	5	−5	A
	Pulse	I_{DP}	20	−20	A
Drain power dissipation (1-device operation, Ta = 25°C)		P_D	2.2		W
Drain power dissipation (6-device operation)	Ta = 25°C	P_{DT}	4.4		W
	Tc = 25°C		36		
Single pulse avalanche energy (Note 1)		E_{AS}	129	273	mJ
Avalanche current		I_{AR}	5	−5	A
Repetitive avalanche energy (Note 2)	1 device operation	E_{AR}	0.22		mJ
	6 device operation	E_{ART}	0.44		
Channel temperature		T_{ch}	150		°C
Storage temperature range		T_{stg}	−55 to 150		°C

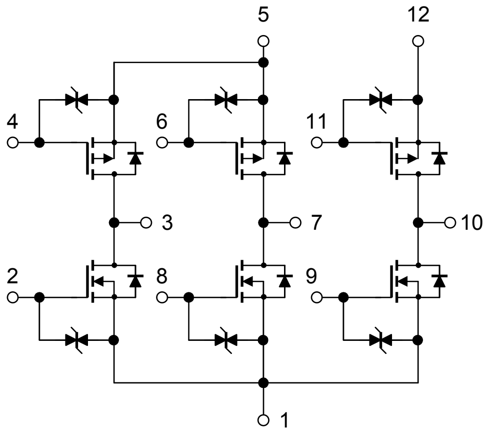
Note 1: Condition for avalanche energy (single pulse)
Nch: V_{DD} = 25 V, starting T_{ch} = 25°C, L = 7 mH, R_G = 25 Ω, I_{AR} = 5 A
Pch: V_{DD} = −25 V, starting T_{ch} = 25°C, L = 14.84 mH, R_G = 25 Ω, I_{AR} = −5 A

Note 2: Repetitive rating; pulse width limited by maximum channel temperature

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

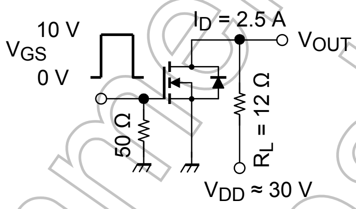
Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance of channel to ambient (6-device operation, Ta = 25°C)	$\Sigma R_{th\ (ch\text{-}a)}$	28.4	°C/W
Thermal resistance of channel to case (6-device operation, Tc = 25°C)	$\Sigma R_{th\ (ch\text{-}c)}$	3.47	°C/W
Maximum lead temperature for soldering purposes (3.2 mm from case for t = 10 s)	T_L	260	°C

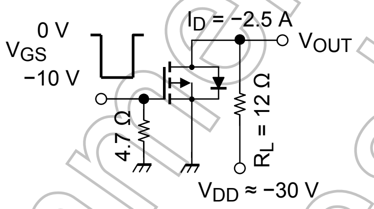
Electrical Characteristics (Ta = 25°C) (Nch MOS FET)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	100	μA
Drain source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 2.5 A	—	0.21	0.32	Ω
			V_{GS} = 10 V, I_D = 2.5 A	—	0.12	0.16	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2.5 A	3.0	5.0	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	370	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	pF
Output capacitance		C_{oss}		—	180	—	pF
Switching time	Rise time	t_r		—	18	—	ns
	Turn-on time	t_{on}		—	25	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}	V_{IN}: t_r, t_f < 5 ns, duty ≤ 1%, t_w = 10 μs	—	170	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 48 V, V_{GS} = 10 V, I_D = 5 A	—	12	—	nC
Gate-source charge		Q_{gs}		—	8	—	nC
Gate-drain ("miller") charge		Q_{gd}		—	4	—	nC

Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	5	A
Pulse drain reverse current	I_{DRP}	—	—	—	20	A
Diode forward voltage	V_{DSF}	I_{DR} = 5 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 5 A, V_{GS} = 0 V	—	70	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	0.1	—	μC

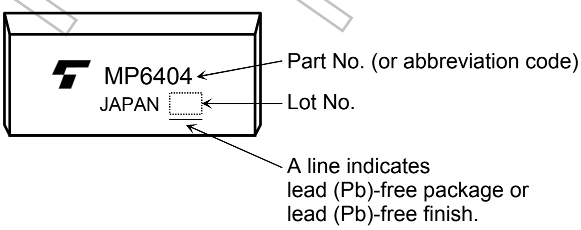
Electrical Characteristics (Ta = 25°C) (Pch MOS FET)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = −60 V, V_{GS} = 0 V	—	—	−100	μA
Drain source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −2.5 A	—	0.24	0.28	Ω
			V_{GS} = −10 V, I_D = −2.5 A	—	0.16	0.19	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D =−2.5 A	2.0	4.0	—	S
Input capacitance		C_{iss}	V_{DB} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	630	—	pF
Reverse transfer capacitance		C_{rss}		—	95	—	pF
Output capacitance		C_{oss}		—	290	—	pF
Switching time	Rise time	t_r		—	25	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}	V_{IN}: t_r, t_f < 5 ns, duty ≤ 1%, t_w = 10 μs	—	200	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ −48 V, V_{GS} = −10 V, I_D = −5 A	—	22	—	nC
Gate-source charge		Q_{gs}		—	16	—	nC
Gate-drain ("miller") charge		Q_{gd}		—	6	—	nC

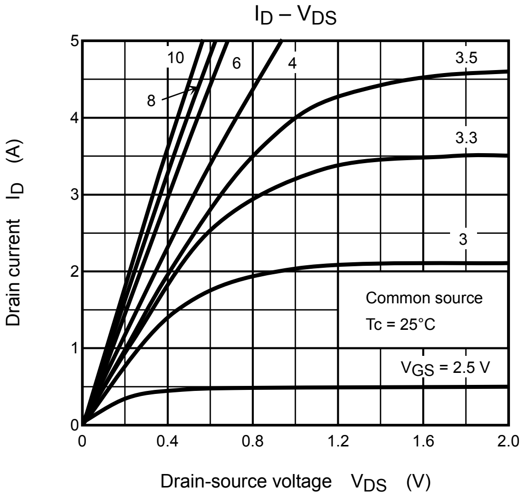
Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

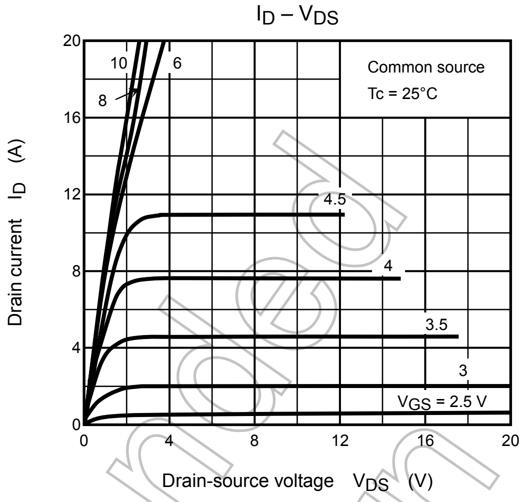
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	−5	A
Pulse drain reverse current	I_{DRP}	—	—	—	−20	A
Diode forward voltage	V_{DSF}	I_{DR} = −5 A, V_{GS} = 0 V	—	—	1.7	V
Reverse recovery time	t_{rr}	I_{DR} = −5 A, V_{GS} = 0 V	—	80	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	0.1	—	μC

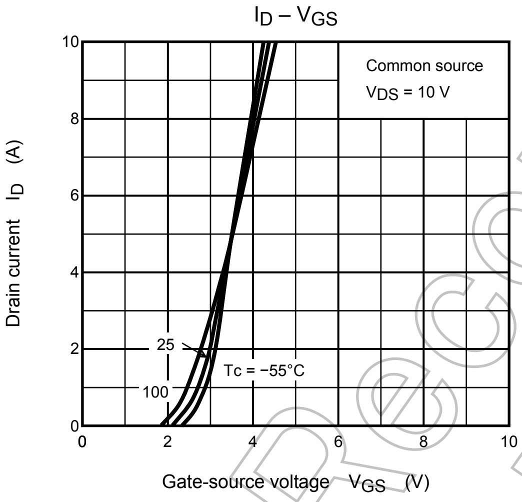
Marking

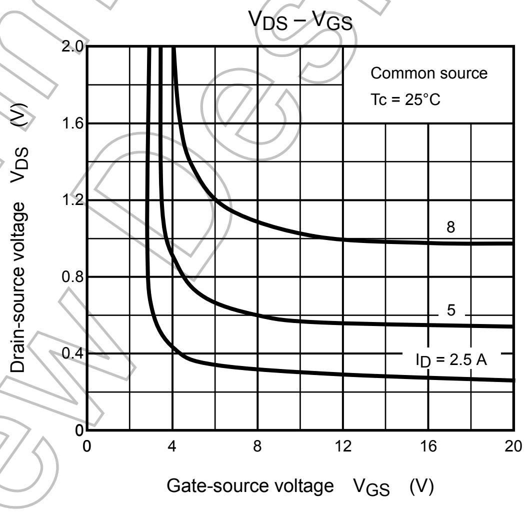


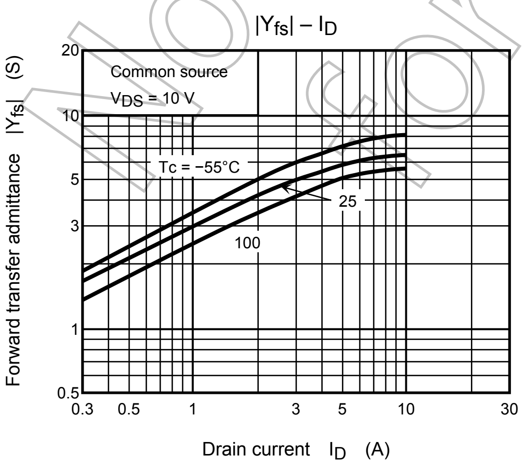
Nch MOS FET

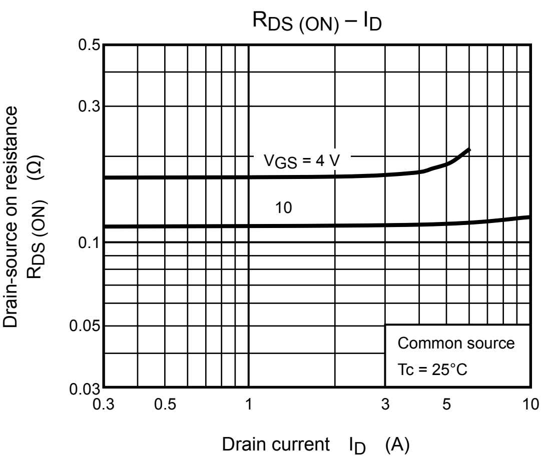

I_D – V_DS
10
8
6
4
3.5
3.3
3
Common source
Tc = 25°C
V_GS = 2.5 V
Drain current I_D (A)
Drain-source voltage V_DS (V)
0
1
2
3
4
5
0.4
0.8
1.2
1.6
2.0


I_D – V_DS
10
8
6
Common source
Tc = 25°C
4.5
4
3.5
3
V_GS = 2.5 V
Drain current I_D (A)
Drain-source voltage V_DS (V)
0
4
8
12
16
20


I_D – V_GS
Common source
V_DS = 10 V
25
Tc = −55°C
100
Drain current I_D (A)
Gate-source voltage V_GS (V)
0
2
4
6
8
10

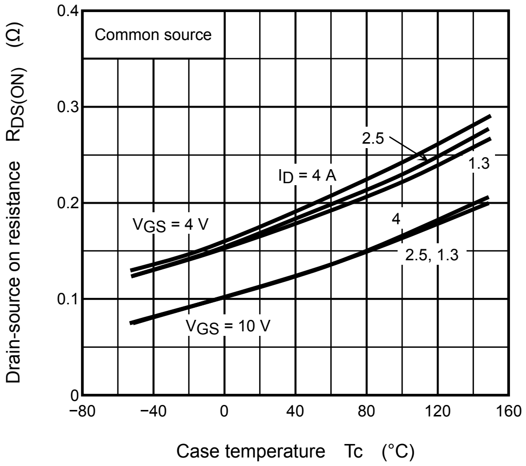

V_DS – V_GS
Common source
Tc = 25°C
8
5
I_D = 2.5 A
Drain-source voltage V_DS (V)
Gate-source voltage V_GS (V)
0
0.4
0.8
1.2
1.6
2.0
4
8
12
16
20


|Y_fs| – I_D
Common source
V_DS = 10 V
Tc = −55°C
25
100
Forward transfer admittance |Y_fs| (S)
Drain current I_D (A)
0.5
1
3
5
10
20
0.3
0.5
1
3
5
10
30

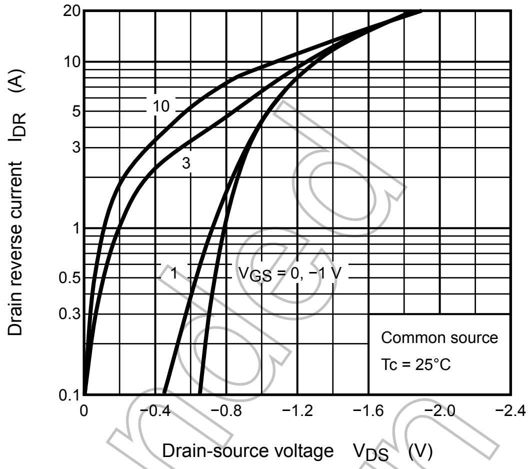

R_DS (ON) – I_D
V_GS = 4 V
10
Common source
Tc = 25°C
Drain-source on resistance R_DS (ON) (Ω)
Drain current I_D (A)
0.03
0.05
0.1
0.3
0.5
0.3
0.5
1
3
5
10

Nch MOS FET

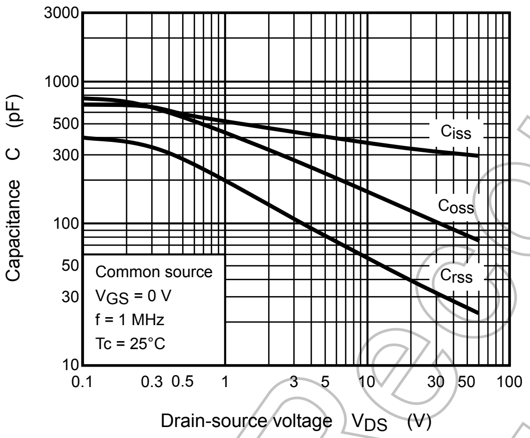
$R_{DS\ (ON)}$ – Tc



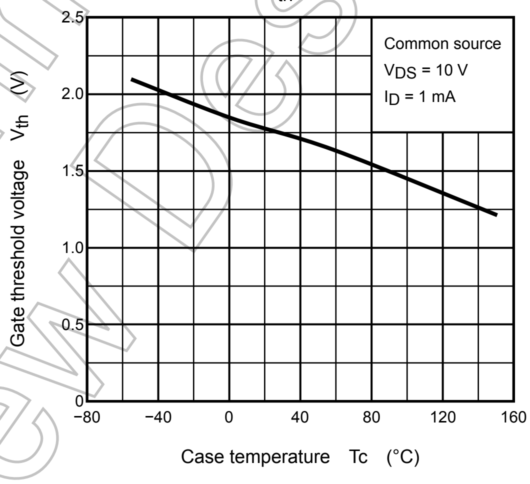
I_{DR} – V_{DS}



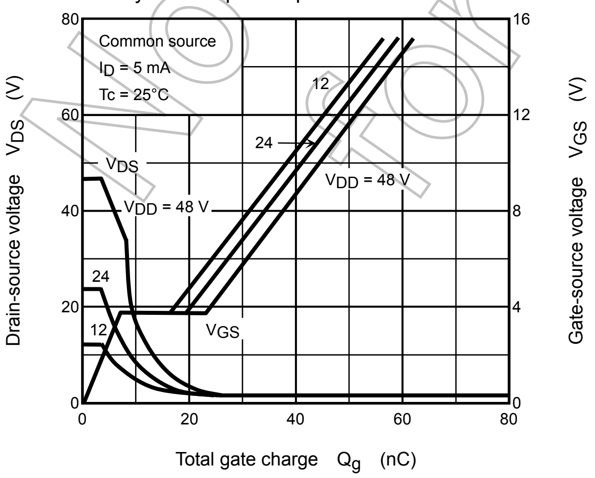
Capacitance – V_{DS}



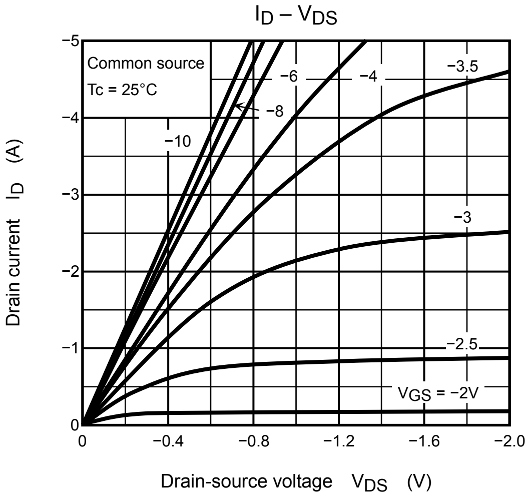
V_{th} – Tc

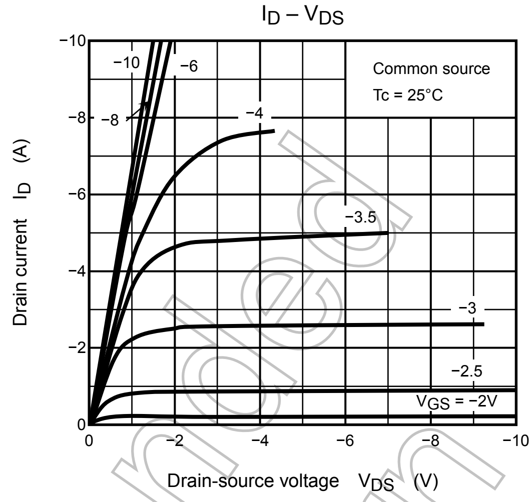


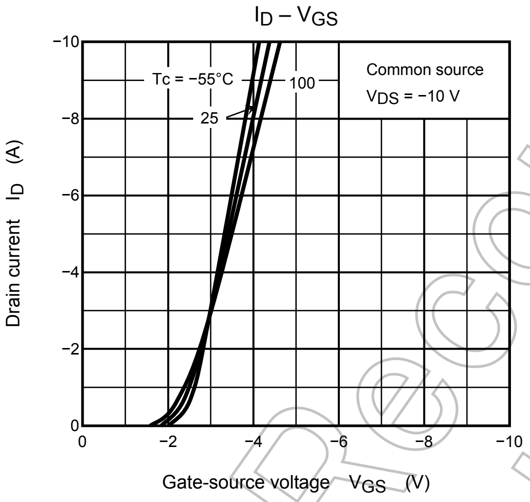
Dynamic Input/Output Characteristics

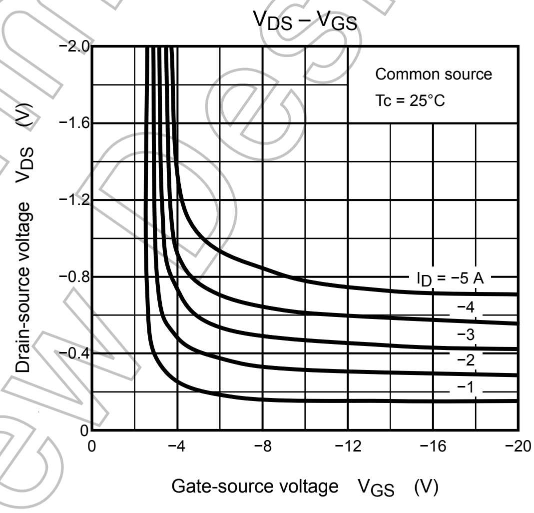


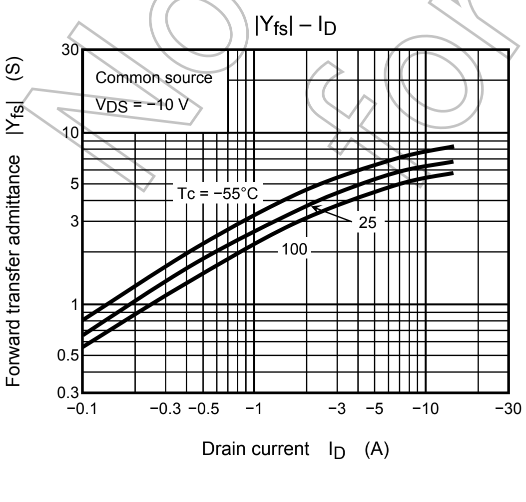
Pch MOS FET

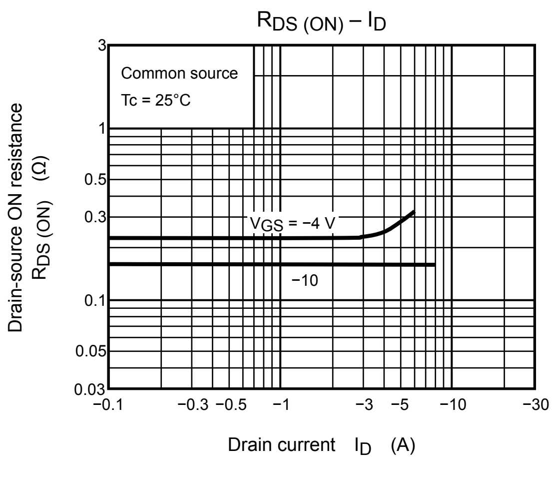

ID – VDS
Common source
Tc = 25°C
−10
−8
−6
−4
−3.5
−3
−2.5
VGS = −2V
Drain current ID (A)
Drain-source voltage VDS (V)
0
−0.4
−0.8
−1.2
−1.6
−2.0
−1
−2
−3
−4
−5


ID – VDS
Common source
Tc = 25°C
−10
−8
−6
−4
−3.5
−3
−2.5
VGS = −2V
Drain current ID (A)
Drain-source voltage VDS (V)
0
−2
−4
−6
−8
−10


ID – VGS
Common source
VDS = −10 V
Tc = −55°C
100
25
Drain current ID (A)
Gate-source voltage VGS (V)
0
−2
−4
−6
−8
−10

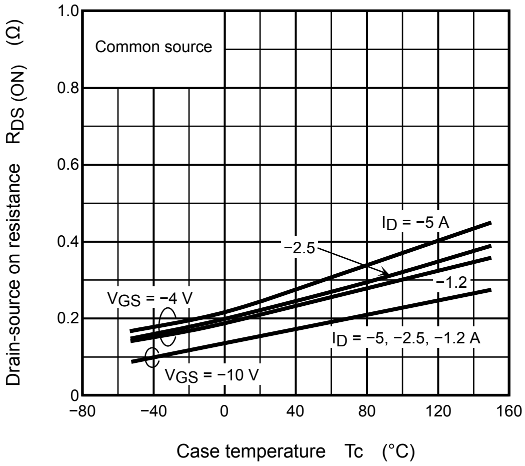

VDS – VGS
Common source
Tc = 25°C
ID = −5 A
−4
−3
−2
−1
Drain-source voltage VDS (V)
Gate-source voltage VGS (V)
0
−0.4
−0.8
−1.2
−1.6
−2.0
−4
−8
−12
−16
−20


|Yfs| – ID
Common source
VDS = −10 V
Tc = −55°C
25
100
Forward transfer admittance |Yfs| (S)
Drain current ID (A)
0.3
0.5
1
3
5
10
30
−0.1
−0.3
−0.5
−1
−3
−5
−10
−30

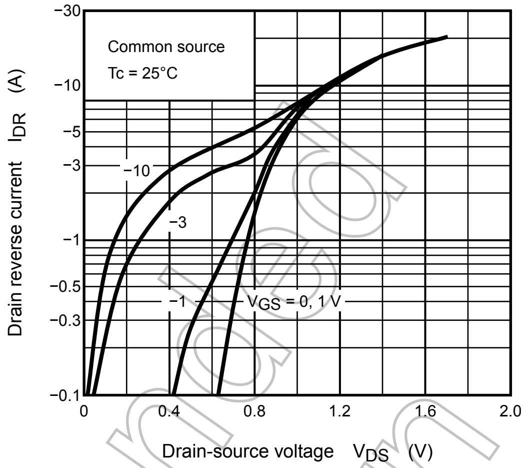

RDS (ON) – ID
Common source
Tc = 25°C
VGS = −4 V
−10
Drain-source ON resistance RDS (ON) (Ω)
Drain current ID (A)
0.03
0.05
0.1
0.3
0.5
1
3
−0.1
−0.3
−0.5
−1
−3
−5
−10
−30

Pch MOS FET

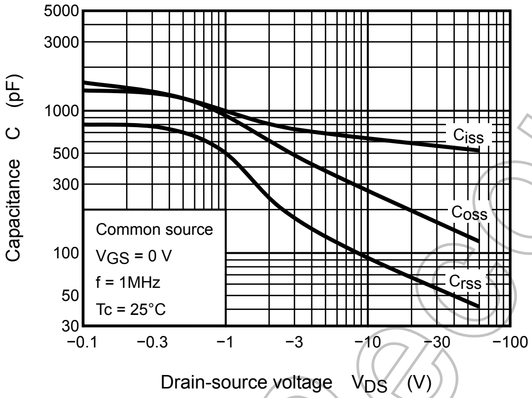
$R_{DS (ON)}$ – Tc



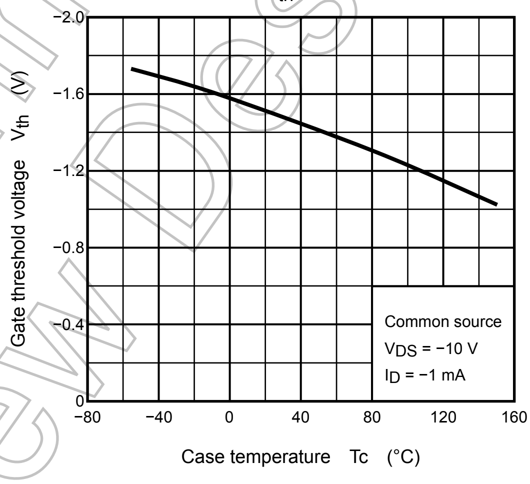
I_{DR} – V_{DS}



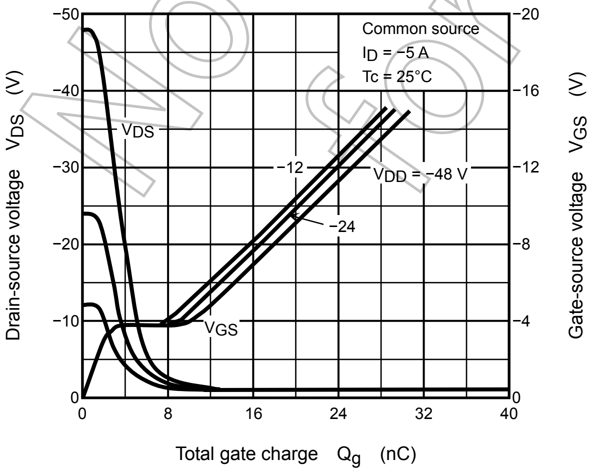
Capacitance – V_{DS}

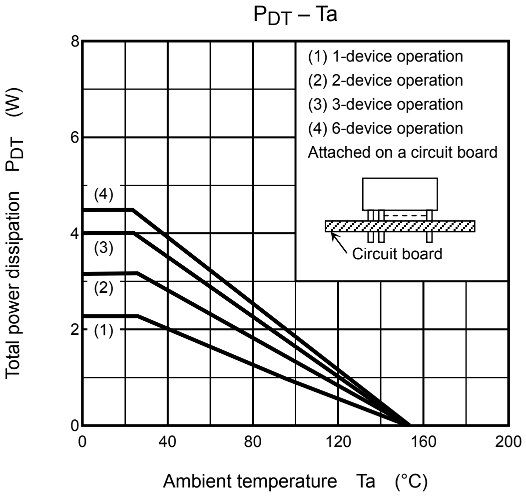


V_{th} – Tc

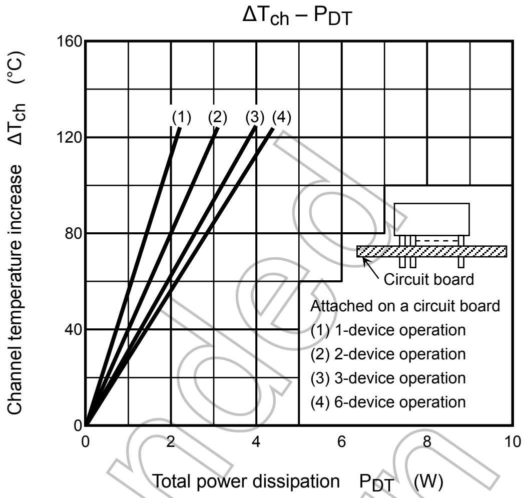


Dynamic Input/Output Characteristics

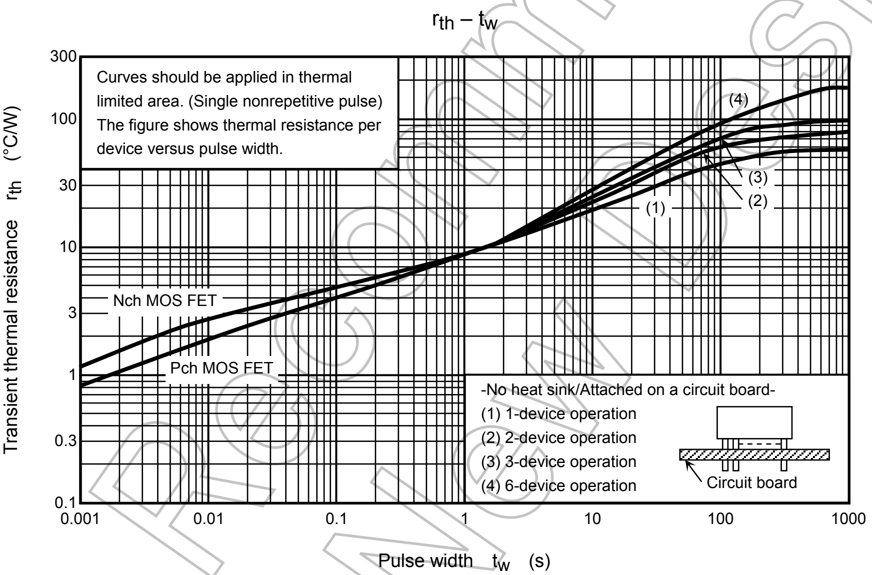




PDT – Ta
(1) 1-device operation
(2) 2-device operation
(3) 3-device operation
(4) 6-device operation
Attached on a circuit board
Circuit board
Total power dissipation PDT (W)
Ambient temperature Ta (°C)
0
2
4
6
8
40
80
120
160
200

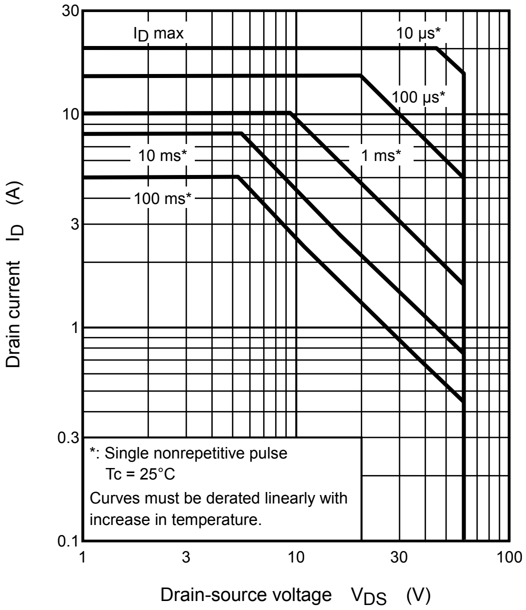


ΔTch – PDT
Circuit board
Attached on a circuit board
(1) 1-device operation
(2) 2-device operation
(3) 3-device operation
(4) 6-device operation
Channel temperature increase ΔTch (°C)
Total power dissipation PDT (W)
0
40
80
120
160
2
4
6
8
10

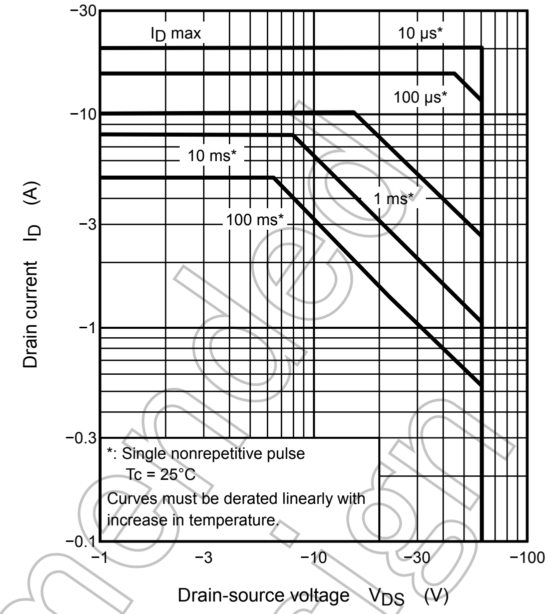


rth – tw
Curves should be applied in thermal limited area. (Single nonrepetitive pulse) The figure shows thermal resistance per device versus pulse width.
Nch MOS FET
Pch MOS FET
-No heat sink/Attached on a circuit board-
(1) 1-device operation
(2) 2-device operation
(3) 3-device operation
(4) 6-device operation
Circuit board
Transient thermal resistance rth (°C/W)
Pulse width tw (s)
0.1
0.3
1
3
10
30
100
300
0.001
0.01
0.1
1
10
100
1000

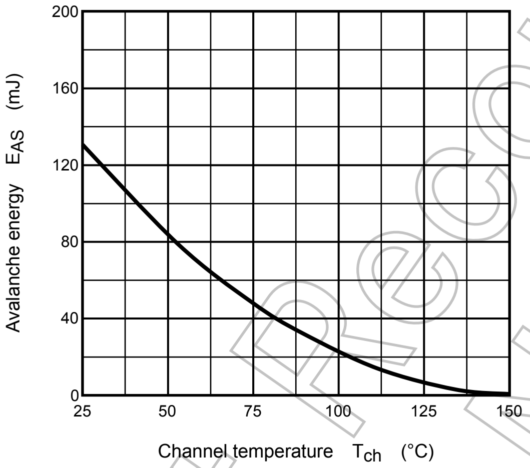
Safe Operating Area
(Applicable to Nch MOS FET)



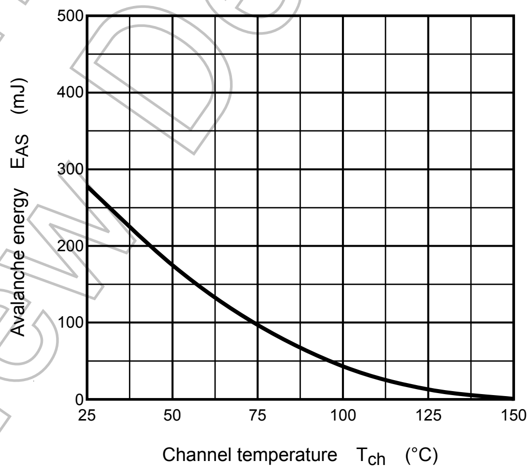
Safe Operating Area
(Applicable to Pch MOS FET)

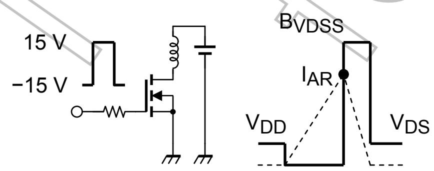


$E_{AS} – T_{ch}$
(Applicable to Nch MOS FET)



$E_{AS} – T_{ch}$
(Applicable to Pch MOS FET)

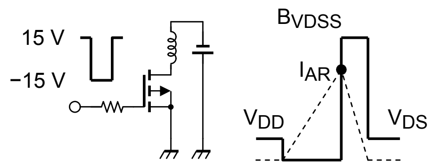




Test Circdcuit Test Waveform

Peak I_{AR} = 5 A, R_G = 25 Ω
V_{DD} = 25 V, L = 7 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$



Test Circuit Test Waveform

Peak I_{AR} = −5 A, R_G = 25 Ω
V_{DD} = −25 V, L = 14.84 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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20070701-EN

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