TOSHIBA Power MOS FET Module Silicon N&P Channel MOS Type (Four L²-π-MOSV in One)

MP4212

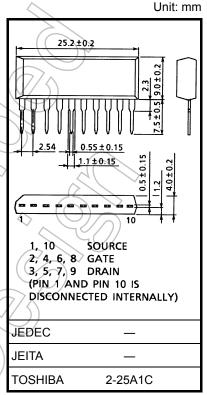
High Power High Speed Switching Applications H-Switch Driver

- 4-V gate drivability
- Small package by full molding (SIP 10 pin)
- High drain power dissipation (4-device operation)
 PT = 4 W (Ta = 25°C)
- Low drain-source ON resistance: RDS (ON) = 120 m Ω (typ.) (N-ch) 160 m Ω (typ.) (P-ch)
- High forward transfer admittance: $|Y_{fs}| = 5.0 \text{ S (typ.) (Nch)}$ 4.0 S (typ.) (Pch)
- Low leakage current: $I_{GSS} = \pm 10 \mu A \text{ (max) (V}_{GS} = \pm 16 \text{ V)}$ $I_{DSS} = 100 \mu A \text{ (max) (V}_{DS} = 60 \text{ V)}$
- Enhancement-mode: $V_{th} = 0.8 \text{ to } 2.0 \text{ V (VDS} = 10 \text{ V, ID} = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating Nch Pch		Unit		
Drain-source voltage		V _{DSS}	60	-60	V	
Drain-gate voltage (R _{GS}	= 20 kΩ)	V_{DGR}	60	-60	/ (v	
Gate-source voltage		V _{GSS}	±20	±20	X	
Drain current	DC	ĮD.	<u>)</u> 5	-5	^ A	
Diam current	Pulse	(IDP \	20	-20		
Drain power dissipation (1-device operation, Ta =	PD	2.0		W		
Drain power dissipation (4-device operation, Ta =	Рот	4.0		∜ _W		
Single pulse avalanche e	E _{AS}	129	273	mJ		
Avalanche current	IAR	5		Α		
Repetitive avalanche	1-device operation	E _{AR}	0.2		1	
energy (Note 2)	4-device operation	EART			mJ	
Channel temperature	Tch	150		°C		
Storage temperature ran	T _{stg}	−55 to 150		°C		

Industrial Applications



Weight: 2.1 g (typ.)

Note 1: Condition fo avalanche energy (single pulse) measurement

Nch: V_{DD} = 25 V, starting T_{ch} = 25°C, L = 7 mH, R_{G} = 25 Ω , I_{AR} = 5 A

Pch: V_{DD} = -25 V, starting T_{ch} = 25°C, L = 14.84 mH, R_{G} = 25 Ω , I_{AR} = -5 A

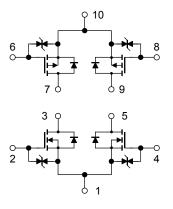
Note 2: Repetitive rating; pulse width limited by maximum channel temperature

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit (
Thermal resistance from channel to ambient	ΣR _{th (ch-a)}	31.2	°C/W
(4-device operation, Ta = 25°C)	(5 5)		
Maximum lead temperature for soldering purposes	TL	260	(C)
(3.2 mm from case for t = 10 s)	_	4	

Electrical Characteristics (Ta = 25°C) (Nch MOS FET)

Charac	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage curre	ent	(I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	_	_	±10	μΑ
Drain cut-off curre	nt	IDSS	V _{DS} = 60 V, V _{GS} = 0 V	_	_	100	μΑ
Drain-source brea	kdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	60	_	_	V
Gate threshold vol	tage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	0.8	_	2.0	V
Drain-source ON r	resistance	R _{DS} (ON)	$V_{GS} = 4 \text{ V}, I_D = 2.5 \text{ A}$	_	0.21	0.32	Ω
		7	$V_{GS} = 10 \text{ V}, I_D = 2.5 \text{ A}$		0.12	0.16	
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = 10 \text{ V}, I_D = 2.5 \text{ A}$	3.0	5.0	_	S
Input capacitance		C _{iss}		_	370	_	pF
Reverse transfer of	apacitance	C _{rss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	60	_	pF
Output capacitanc	e	Coss		_	180	_	pF
Switching time Turn-on time Fall time Turn-off time	Rise time	(t _r)	V _{GS}	_	18	_	
	Turn-on time	t _{on}		_	25	_	ns
	Fall time	t _f		_	55	_	113
	Turn-off time	t _{off}	V_{IN} : t_r , $t_f < 5$ ns, duty $\le 1\%$, $t_W = 10 \ \mu s$	_	170	_	
Total gate charge (Gate-source plus gate-drain)		Qg		_	12	_	nC
Gate-source charge		Q _{gs}	$V_{DD} \approx 48 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	_	8		nC
			-				
Gate-drain ("miller") charge Q _{gd} — 4 —						nC	



Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current	I _{DR}	_	_	_	5	Α
Pulse drain reverse current	I _{DRP}	_	_	_	20	Α
Diode forward voltage	V _{DSF}	I _{DR} = 5 A, V _{GS} = 0 V	/_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 5 A, V _{GS} = 0 V		70	_	ns
Reverse recovery charge	Q _{rr}	dl _{DR} /dt = 50 A/μs	1))0.1	_	μC

Electrical Characteristics (Ta = 25°C) (Pch MOS FET)

Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage curr	ent	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V	_		±10	μΑ
Drain cut-off curre	ent	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V		4	-100	μΑ
Drain-source brea	ıkdown voltage	V (BR) DSS	I _D = -10 mA, V _{GS} = 0 V	-60	()-/	> -	V
Gate threshold vo	Itage	V_{th}	V _{DS} = -10 V, I _D = -1 mA	-0.8	2/5	-2.0	V
Drain-source ON	resistance	R _{DS (ON)}	$V_{GS} = -4 \text{ V} \cdot _{D} = -2.5 \text{ A}$ $V_{GS} = -10 \text{ V} \cdot _{D} = -2.5 \text{ A}$		0.24	0.28	Ω
Forward transfer a	admittance	Y _{fs}	$V_{DS} = -10 \text{ V}, I_{D} = -2.5 \text{ A}$	2.0	4.0	_	S
Input capacitance		C _{iss}		\ _	630	_	pF
Reverse transfer	capacitance	C _{rss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	/ _	95	_	pF
Output capacitance		Coss			290	_	pF
Switching time	Rise time	tr	0 V I _D = -2.5 A	_	25	_	
	Turn-on time	ton	V _{GS} -10 V	_	45	_	no
	Fall time	tr		_	55	_	ns
	Turn-off time	t _{off}	V _{IN} : t _r , t _f < 5 ns, duty ≤ 1%, t _W = 10 μs	I	200	_	
Total gate charge (gate-source plus	\ \ \	Qg	V _{DD} ≈ -48 V, V _{GS} = -10 V, I _D = -5 A	_	22	_	nC
Gate-source charge		Q_{gs}	VDD ~ -40 V, VGS10 V, ID = -5 A	_	16	_	nC
Gate-drain ("mille	r") charge	Qgd		_	6	_	nC

Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current	I _{DR}	_	_	_	-5	Α
Pulse drain reverse current	I _{DRP}	_	_	_	-20	Α
Diode forward voltage	V _{DSF}	I _{DR} = -5 A, V _{GS} = 0 V	_	_	1.7	V
Reverse recovery time	t _{rr}	I _{DR} = -5 A, V _{GS} = 0 V	_	80	_	ns
Reverse recovery charge	Q _{rr}	dl _{DR} /dt = 50 A/μs	_	0.1	_	μC

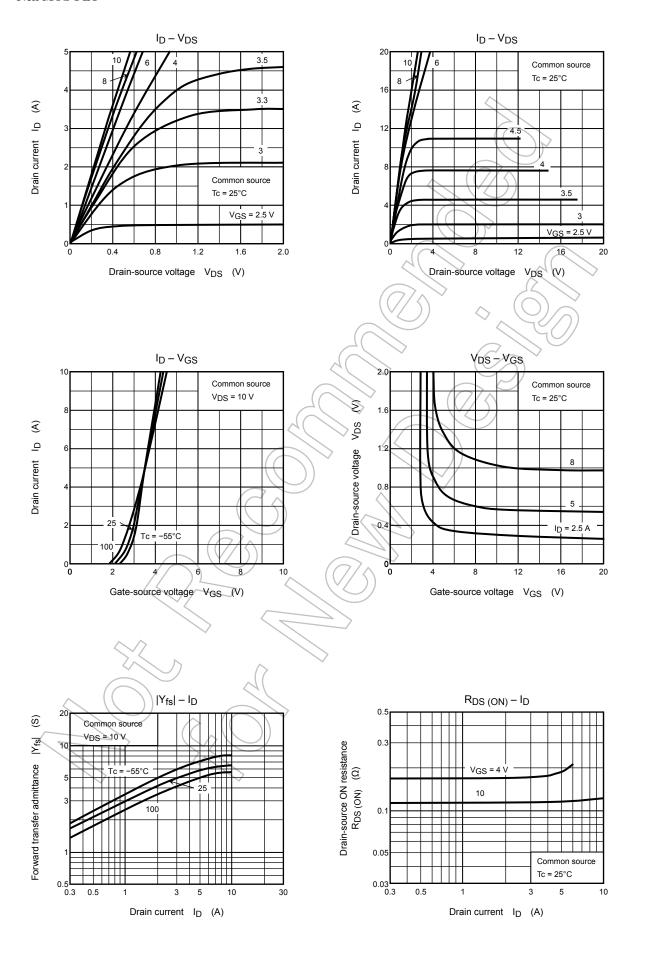
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Marking

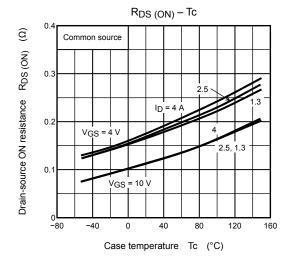


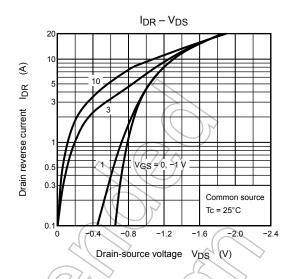
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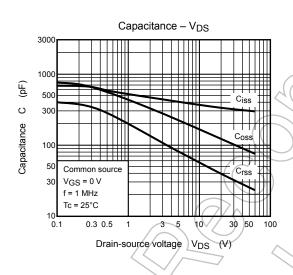
Nch MOS FET

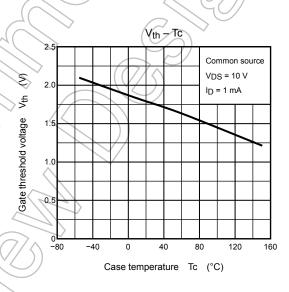


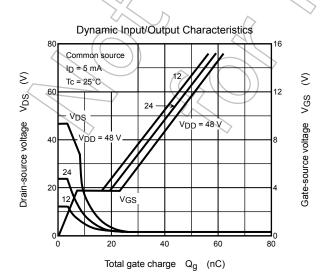
Nch MOS FET







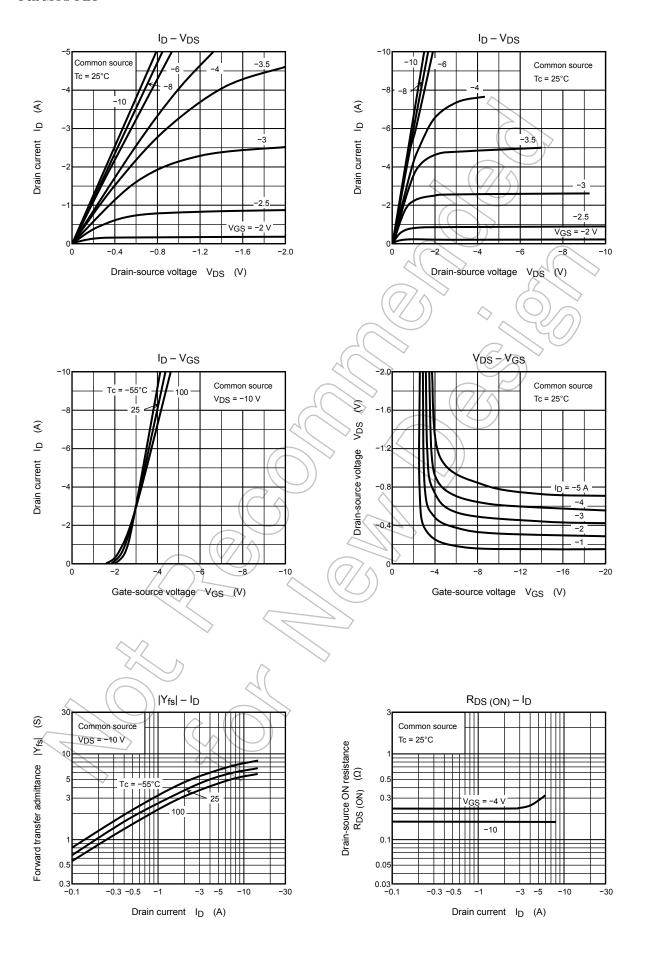




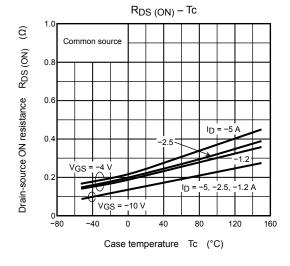
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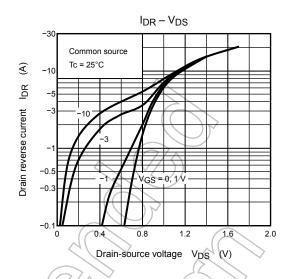
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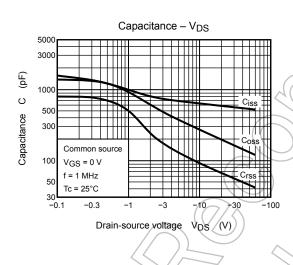
Pch MOS FET

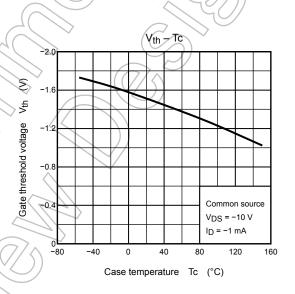


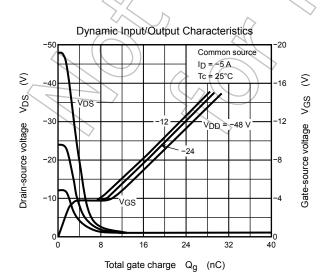
Pch MOS FET



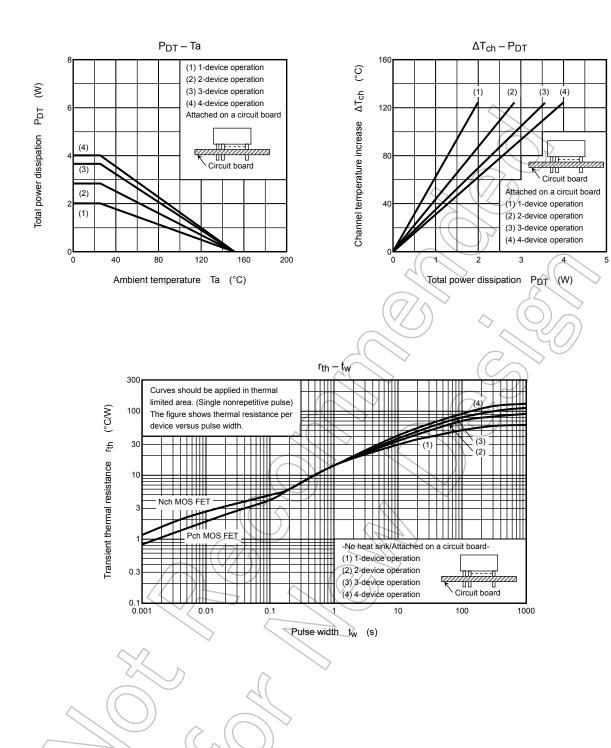


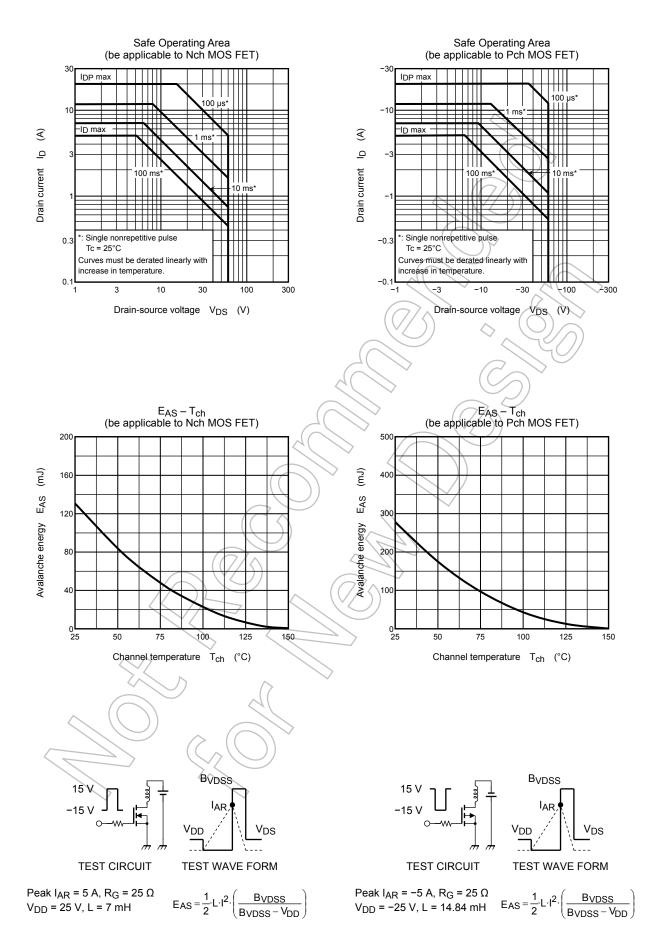






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