32-bit RISC Microcontroller
TXZ+ Family
TMPM4K Group(1)

Reference Manual
Input/Output Ports
(PORT-M4K(1))

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

Terms and Abbreviations

Some of abbreviations used in this document are as follows:

EI2C	I^2C Interface Version A
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
NBDIF	Non- break Debug Interface
SW	Serial Wire

1. Outlines

It is described about the register and setting of port. A list of the functions is indicated below.

Function classification	Function	Description
Ports	-	Programmable pull-up and Programmable pull-down can be selected. Open-drain output can be selected.
Peripheral function pins	Clock Output	System clock output is possible.
	External Interrupt	Interrupt input pin has a noise filter (Filter width: 30ns (typ.)).
	32-bit Timer Event Counter	Input capture input pin, timer output pin
	Serial Peripheral Interface	Data input pin, data output pin, clock input/output pin
	Asynchronous Serial Communication Circuit	Data input pin, data output pin, handshake function pins
	I^2C Interface	Data input/output pin, clock input/output pin
	Analog Digital Convertor	Analog input pins
	Advanced Programmable Motor Control Circuit	X/Y/Z-phase output pins, U/V/W-phase output pins, EMG detection input pin, overvoltage detection input pin.
	Advanced Encoder Input Circuit (32bit)	Encoder input pins
	Trigger Selector	External trigger input pins
Debug pins	JTAG	Test mode select input pin, serial clock input pin, serial data output pin, serial data input pin, test reset input pin
	SW	Serial wire data input/output pin, serial wire clock input pin, serial wire viewer output pin
	Trace	Trace clock output pin, trace data output pins 4pins
	NBDIF	NBD synchronous input pin, NBD clock input pin, NBD data Input/output pins 4pins
Control pins	High-speed oscillation circuit	High-speed oscillator connection pin/external clock input pin
	BOOT mode control	BOOT mode control pin

2. Description of Operation

2.1. Clock Supply

When port is used, set an applicable clock enable bit to "1" (clock supply) in fsys supply stop registers A or B (***[CGFSYSENA]***, ***[CGFSYSENB]***), fc supply stop register (***[CGFCEN]***). The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to Reference Manual "Clock Control and Operation Mode".

3. Signal Connection List

This table is sorted the function pins by the signal name of the block diagram (signal table) which is described each Reference Manual. Register setting of the peripherals function is explained in the port order, so please use for a reverse lookup of port name.

The numerical value shows the pin number.

Table 3.1 Signal Connection List (1/5)

Related reference manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)
Asynchronous Serial Communication Circuit	UT0RXD	PK0	63	48	43
		PK1	64	1	44
		PK2	1	2	1
		PK3	2	3	2
	UT0TXDA	PK1	64	1	44
		PK0	63	48	43
		PK3	2	3	2
		PK2	1	2	1
	UT1RXD	PA1	18	13	-
		PA0	19	14	
		PB0	31	23	22
		PB1	32	24	23
	UT1TXDA	PA0	19	14	-
		PA1	18	13	
		PB1	32	24	23
		PB0	31	23	22
	UT2RXD	PG1	57	42	40
	UT2TXDA	PG0	56	41	39
	UT3RXD	PC1	34	-	-
		PC0	35		
	UT3TXDA	PC0	35		
		PC1	34		
I^2C Interface/ I^2C Interface Version A	I2C0SDA/ EI2C0SDA	PB0	31	23	22
	I2C0SCL/ EI2C0SCL	PB1	32	24	23
Serial Peripheral Interface	TSPI0RXD	PK2	1	2	1
	TSPI0TXD	PK3	2	3	2
	TSPI0SCK	PK4	3	4	3
	TSPI1RXD	PA1	18	-	-
	TSPI1TXD	PA0	19		
	TSPI1SCK	PA2	20		
	TSPI2RXD	PG1	57	42	40
	TSPI2TXD	PG0	56	41	39
	TSPI2SCK	PG2	58	43	41
	TSPI3RXD	PC1	34	-	-
	TSPI3TXD	PC0	35		
	TSPI3SCK	PC2	33		

Table 3.2 Signal Connection List (2/5)

Related reference manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)
32-bit Timer Event Counter	T32A00INA0	PK1	64	1	44
	T32A00OUTA	PK0	63	48	43
	T32A00INC0	PK1	64	1	44
	T32A00OUTC	PK0	63	48	43
	T32A01INA0	PA1	18	13	-
	T32A01INA1	PA2	20	-	-
	T32A01OUTA	PA2	20	-	-
	T32A01INB0	PA0	19	14	13
	T32A01OUTB	PA0	19	14	13
	T32A01INC0	PA1	18	13	-
	T32A01INC1	PA2	20	-	-
	T32A01OUTC	PA2	20	-	-
	T32A02INA0	PG1	57	42	40
	T32A02INA1	PG2	58	43	41
	T32A02OUTA	PG0	56	41	39
	T32A02INC0	PG1	57	42	40
	T32A02INC1	PG2	58	43	41
	T32A02OUTC	PG0	56	41	39
	T32A03INA0	PC1	34	-	-
	T32A03INA1	PC2	33	-	-
	T32A03OUTA	PC0	35	25	24
	T32A03INC0	PC1	34	-	-
	T32A03INC1	PC2	33	-	-
	T32A03OUTC	PC0	35	25	24
	T32A04INA0	PF1	52	-	-
	T32A04INA1	PF2	51	-	-
	T32A04OUTA	PF0	55	40	38
	T32A04INC0	PF1	52	-	-
	T32A04INC1	PF2	51	-	-
	T32A04OUTC	PF0	55	40	38
	T32A05INA0	PB1	32	24	23
	T32A05OUTA	PB0	31	23	22
	T32A05OUTB	PB1	32	24	23
	T32A05INC0	PB1	32	24	23
	T32A05OUTC	PB0	31	23	22

Table 3.3 Signal Connection List (3/5)

Related reference manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)
12-bit Analog to Digital Convertor	AINA11/ AINB11	PD0	37	27	26
	AINA12/ AINB12	PD1	38	28	27
	AINA10/ AINB10	PD2	39	29	28
	AINA09/ AINB09	PD3	40	30	29
	AINA08/ AINB08	PD4	41	31	30
	AINA07/ AINB07	PD5	42	32	31
	AINA06/ AINB06	PD6	43	33	32
	AINA05/ AINB05	PE0	44	34	33
	AINA04/ AINB04	PE1	45	35	34
	AINA03/ AINB03	PE2	46	36	-
	AINA02/ AINB02	PE3	47	-	-
	AINA01/ AINB01	PE4	48	-	-
Exception	INT00a	PK0	63	48	43
	INT00b	PF1	52	-	-
	INT01a	PK1	64	1	44
	INT01b	PF2	51	-	-
	INT02a	PK2	1	2	1
	INT02b	PB0	31	23	22
	INT03a	PK3	2	3	2
	INT03b	PB1	32	24	23
	INT04	PG0	56	41	39
	INT05	PG1	57	42	40
	INT06	PK4	3	4	3
	INT07a	PA0	19	14	13
	INT07b	PC2	33	-	-
	INT08	PC0	35	25	24
	INT09	PA1	18	13	-
	INT10	PC1	34	-	-

Table 3.4 Signal connection list (4/5)

Related reference manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)
Advanced Programmable Motor Control Circuit	EMG0	PJ6	22	15	14
		PD6	43	33	32
		PH2	13	8	8
	OVV0	PJ7	21	-	-
	UO0	PJ0	28	21	20
	VO0	PJ2	26	19	18
	WO0	PJ4	24	17	16
	XO0	PJ1	27	20	19
	YO0	PJ3	25	18	17
	ZO0	PJ5	23	16	15
	PMD0DBG	PB0	31	23	22
		PG0	56	41	39
		PJ0	28	21	20
	EMG1	PF0	55	40	-
	UO1	PG0	56	41	-
	VO1	PG1	57	42	-
	WO1	PG2	58	43	-
	XO1	PG3	59	44	-
	YO1	PG4	60	45	-
	ZO1	PG5	61	46	-
	PMD1DBG	PB1	32	24	-
		PJ1	27	20	-
		PG1	57	42	-
Advanced Encoder Input Circuit (32-bit)	ENC0A	PG0	56	41	39
	ENC0B	PG1	57	42	40
	ENC0Z	PG2	58	43	41
	ENC1A	PJ5	23	16	15
	ENC1B	PJ4	24	17	16
	ENC1Z	PJ3	25	18	17

Table 3.5 Signal connection list (5/5)

Related reference manual	Function pin name	Port name	M4K4 (LQFP64)	M4K2 (LQFP48)	M4K1 (LQFP44)
Product Information (Trigger Selector)	TRGIN0	PF0	55	40	38
	TRGIN1	PB1	32	24	23
	TRGIN2	PF2	51	-	-
Debug Interface (JTAG/SW)	TMS	PK2	1	2	1
	TCK	PK3	2	3	2
	TDO	PK1	64	1	44
	TDI	PK0	63	48	43
	TRST_N	PK4	3	4	3
	SWDIO	PK2	1	2	1
	SWCLK	PK3	2	3	2
	SWV	PK1	64	1	44
Debug Interface (Trace)	TRACECLK	PL4	8	-	-
	TRACEDATA0	PL0	7		
	TRACEDATA1	PL1	6		
	TRACEDATA2	PL2	5		
	TRACEDATA3	PL3	4		
Debug Interface (NBDIF)	NBDSYNC	PK4	3	-	-
	NBDCLK	PL4	8		
	NBDDATA0	PL0	7		
	NBDDATA1	PL1	6		
	NBDDATA2	PL2	5		
	NBDDATA3	PL3	4		
Clock Generator and Operation Mode	X1	PH0	15	10	10
	EHCLKIN	PH0	15	10	10
	X2	PH1	16	11	11
	SCOUT	PJ0	28	21	20
FLASH Memory	BOOT_N	PJ6	22	15	14

4. Registers

The following registers should be set to use the port.

Each register is 32 bits. The configuration of the register depends on the port count and its function assignment.

"x" and "n" in the following table show a port name and a function number, respectively.

Register name		Type	Setting value	Description
[PxDATA]	Data Register	R/W	0 or 1	Read from a port or an output data. And write to an output data.
[PxCR]	Output Control Register	R/W	0: Output disabled 1: Output enabled	Output control
[PxFRn]	Function register n	R/W	0: PORT 1: Function	Function setting When “1” is set, the assigned function is enabled. Each function assigned to a port has its own function register. If multiple functions are assigned to one bit of port, only one function should be enabled.
[PxOD]	Open-drain Control Register	R/W	0: CMOS 1: Open drain	Programmable open-drain control The programmable open drain is a pseudo open drain. An output buffer is disabled by setting ***[PxOD]*** to “1” when the output data is “1”.
[PxPUP]	Pull-up Control Register	R/W	0: Pull-up disabled 1: Pull-up enabled	Programmable pull-up resistor control
[PxPDN]	Pull-down Control Register	R/W	0: Pull-down disabled 1: Pull-down enabled	Programmable pull-down resistor control
[PxIE]	Input Control Register	R/W	0: Input disabled 1: Input enabled	Input control Up to 100ns is required that a state of port is reflected to ***[PxDATA]*** after ***[PxIE]*** is set to “1”.

4.1. List of Registers

When the bit which is not assigned is read, "0" is read. The write to it is ignored.

Table 4.1 Base Address of Port Registers

Peripheral function		Channel/Unit	Base address
Input/output ports	PA	-	0x400C0000
	PB	-	0x400C0100
	PC	-	0x400C0200
	PD	-	0x400C0300
	PE	-	0x400C0400
	PF	-	0x400C0500
	PG	-	0x400C0600
	PH	-	0x400C0700
	PJ	-	0x400C0800
	PK	-	0x400C0900
	PL	-	0x400C0A00

Table 4.2 List of Registers

Register name	Address (Base+)	Port A	Port B	Port C	Port D	Port E	Port F
Data Register	0x0000	*[PADATA]*	*[PBDATA]*	*[PCDATA]*	*[PDDATA]*	*[PEDATA]*	*[PFDATA]*
Output Control Register	0x0004	*[PACR]*	*[PBCR]*	*[PCCR]*	*[PDCR]*	*[PECR]*	*[PFCR]*
Function Register 1	0x0008	*[PAFR1]*	*[PBFR1]*	*[PCFR1]*	-	-	-
Function Register 2	0x000C	*[PAFR2]*	*[PBFR2]*	*[PCFR2]*	-	-	-
Function Register 3	0x0010	*[PAFR3]*	*[PBFR3]*	*[PCFR3]*	-	-	-
Function Register 4	0x0014	*[PAFR4]*	*[PBFR4]*	*[PCFR4]*	-	-	*[PFFR4]*
Function Register 5	0x0018	*[PAFR5]*	*[PBFR5]*	*[PCFR5]*	*[PDFR5]*	-	*[PFFR5]*
Function Register 6	0x001C	*[PAFR6]*	*[PBFR6]*	-	-	-	*[PFFR6]*
Function Register 7	0x0020	*[PAFR7]*	*[PBFR7]*	-	-	-	*[PFFR7]*
Function Register 8	0x0024	-	*[PBFR8]*	-	-	-	-
Open-Drain Control Register	0x0028	*[PAOD]*	*[PBOD]*	*[PCOD]*	*[PDOD]*	*[PEOD]*	*[PFOD]*
Pull-up Control Register	0x002C	*[PAPUP]*	*[PBPUP]*	*[PCPUP]*	*[PDPUP]*	*[PEPUP]*	*[PFPUP]*
Pull-down Control Register	0x0030	*[PAPDN]*	*[PBPDN]*	*[PCPDN]*	*[PDPDN]*	*[PEPDN]*	*[PFPDN]*
Input Control Register	0x0038	*[PAIE]*	*[PBIE]*	*[PCIE]*	*[PDIE]*	*[PEIE]*	*[PFIE]*

Register name	Address (Base+)	Port G	Port H		Port J	Port K	Port L
			PH0/1	PH2/3			
Data Register	0x0000	*[PGDATA]*	*[PHDATA]*	*[PHDATA]*	*[PJDATA]*	*[PKDATA]*	*[PLDATA]*
Output Control Register	0x0004	*[PGCR]*	-	*[PHCR]*	*[PJCR]*	*[PKCR]*	*[PLCR]*
Function Register 1	0x0008	*[PGFR1]*	-	-	-	*[PKFR1]*	-
Function Register 2	0x000C	*[PGFR2]*	-	-	-	*[PKFR2]*	-
Function Register 3	0x0010	*[PGFR3]*	-	-	-	*[PKFR3]*	-
Function Register 4	0x0014	*[PGFR4]*	-	-	*[PJFR4]*	*[PKFR4]*	-
Function Register 5	0x0018	*[PGFR5]*	-	*[PHFR5]*	*[PJFR5]*	*[PKFR5]*	-
Function Register 6	0x001C	*[PGFR6]*	-	-	*[PJFR6]*	*[PKFR6]*	*[PLFR6]*
Function Register 7	0x0020	*[PGFR7]*	-	-	*[PJFR7]*	*[PKFR7]*	*[PLFR7]*
Open-Drain Control Register	0x0028	*[PGOD]*	-	*[PHOD]*	*[PJOD]*	*[PKOD]*	*[PLOD]*
Pull-up Control Register	0x002C	*[PGPUP]*	-	*[PHPUP]*	*[PJPUP]*	*[PKPUP]*	*[PLPUP]*
Pull-down Control Register	0x0030	*[PGPDN]*	*[PHPDN]*	*[PHPDN]*	*[PJPDN]*	*[PKPDN]*	*[PLPDN]*
Input Control Register	0x0038	*[PGIE]*	*[PHIE]*	*[PHIE]*	*[PJIE]*	*[PKIE]*	*[PLIE]*

Note: Do not access the addresses described as "-".

4.2. List of Port Function Register Settings

It is explained about viewpoint of a list of the port function register settings tables.

The column of ***[PxFRn]*** shows the function register which should be set. When this register is set to "1", the corresponding function is enabled. (x is a port name and n is a function number.)

The bit of the "N/A" in the tables returns "0" when it is read. The write to the bit is ignored.

"0" or "1" in the tables shows the setting value. "0/1" means either value can be set.

PORT	Reset status	Input/Output	Port type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	INT07a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	*[PAFR1]*	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	*[PAFR2]*	0/1	0/1	0/1	1
	TSPI1TXD	Output	FTU2a	0/1	1	*[PAFR3]*	0/1	0/1	0/1	0
	T32A01INB0	Input	FTU1a	0/1	0	*[PAFR4]*	0/1	0/1	0/1	1
	T32A01OUTB	Output	FTU1a	0/1	1	*[PAFR5]*	0/1	0/1	0/1	0
PA2	After reset			0	0	0	0	0	0	0
	Input Port	Input		0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output		0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FTU1a	0/1	0	*[PAFR3]*	0/1	0/1	0/1	1
		Output			1					0
	T32A01INA1	Input	FTU1a	0/1	0	*[PAFR4]*	0/1	0/1	0/1	1
	T32A01INC1	Input	FTU1a	0/1	0	*[PAFR5]*	0/1	0/1	0/1	1
	T32A01OUTA	Output	FTU1a	0/1	1	*[PAFR6]*	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1a	0/1	1	*[PAFR7]*	0/1	0/1	0/1	0

[PxFRn]	Pin					
	UT1TXDA	UT1RXD	TSPI1TXD	T32A01INB0	T32A01OUTB	Input Port Output Port
[PAFR1]<bit0>	1	0	0	0	0	0
[PAFR2]<bit0>	0	1	0	0	0	0
[PAFR3]<bit0>	0	0	1	0	0	0
[PAFR4]<bit0>	0	0	0	1	0	0
[PAFR5]<bit0>	0	0	0	0	1	0

4.2.1. Setting of Using Alternated Pin

To use the alternated pins as peripheral function output pins, set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function and then set output control register to enable output (***[PxCR]***<bit m>=1). If output is enabled before setting the function register, the data register value of the port is output until the function register is set.

To use the alternated pins as input pins of the peripheral function, set the input control register to enable input (***[PxIE]***<bit m>=1) and set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function, then set the peripheral functions.

To use the alternated pins as input/output pin of the peripheral functions such as I^2C, set the input control register to enable input (***[PxIE]***<bit m>=1), set the function register (***[PxFRn]***<bit m>=1) to use as the peripheral function and set the output control register to enable output (***[PxCR]***<bit m>=1), then set the peripheral function.

- When some functions are assigned to the same pin, use only one function exclusively.
- When the same function is assigned to some ports, use only one pin exclusively.

4.2.2. PORT A

Table 4.3 Port A Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PADATA]	*[PACR]*	*[PAFRn]*	*[PAOD]*	*[PAPUP]*	*[PAPDN]*	*[PAIE]*
PA0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT07a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PAFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PAFR2]***	0/1	0/1	0/1	1
	TSPI1TXD	Output	FTU2a	0/1	1	***[PAFR3]***	0/1	0/1	0/1	0
	T32A01INB0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01OUTB	Output	FTU1a	0/1	1	***[PAFR5]***	0/1	0/1	0/1	0
PA1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT09	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1RXD	Input	FTU1a	0/1	0	***[PAFR1]***	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PAFR2]***	0/1	0/1	0/1	0
	TSPI1RXD	Input	FTU1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
	T32A01INA0	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01INC0	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
PA2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI1SCK	Input	FTU1a	0/1	0	***[PAFR3]***	0/1	0/1	0/1	1
		Output			1					0
	T32A01INA1	Input	FTU1a	0/1	0	***[PAFR4]***	0/1	0/1	0/1	1
	T32A01INC1	Input	FTU1a	0/1	0	***[PAFR5]***	0/1	0/1	0/1	1
	T32A01OUTA	Output	FTU1a	0/1	1	***[PAFR6]***	0/1	0/1	0/1	0
	T32A01OUTC	Output	FTU1a	0/1	1	***[PAFR7]***	0/1	0/1	0/1	0

4.2.3. PORT B

Table 4.4 Port B Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PBDATA]	*[PBCR]*	*[PBFRn]*	*[PBOD]*	*[PBPUP]*	*[PBPDN]*	*[PBIE]*
PB0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT02a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT1TXDA	Output	FTU1a	0/1	1	***[PBFR2]***	0/1	0/1	0/1	0
	I2C0SDA/ EI2C0SDA (Note)	I/O	FTU1a	0/1	1	***[PBFR3]***	1	0/1	0	1
	T32A05OUTA	Output	FTU1a	0/1	1	***[PBFR4]***	0/1	0/1	0/1	0
	T32A05OUTC	Output	FTU1a	0/1	1	***[PBFR5]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FTU1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PBFR8]***	0/1	0/1	0/1	1
PB1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT03b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A05OUTB	Output	FTU1a	0/1	1	***[PBFR1]***	0/1	0/1	0/1	0
	UT1RXD	Input	FTU1a	0/1	0	***[PBFR2]***	0/1	0/1	0/1	1
	I2C0SCL/ EI2C0SCL (Note)	I/O	FTU1a	0/1	1	***[PBFR3]***	1	0/1	0	1
	T32A05INA0	Input	FTU1a	0/1	0	***[PBFR4]***	0/1	0/1	0/1	1
	T32A05INC0	Input	FTU1a	0/1	0	***[PBFR5]***	0/1	0/1	0/1	1
	TRGIN1	Input	FTU1a	0/1	0	***[PBFR6]***	0/1	0/1	0/1	1
	PMD1DBG	Output	FTU1a	0/1	1	***[PBFR7]***	0/1	0/1	0/1	0
	UT1TXDA	Output	FTU1a	0/1	1	***[PBFR8]***	0/1	0/1	0/1	0

Note: Use I2C and EI2C exclusively.

4.2.4. PORT C

Table 4.5 Port C Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PCDATA]	*[PCCR]*	*[PCFRn]*	*[PCOD]*	*[PCPUP]*	*[PCPDN]*	*[PCIE]*
PC0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT08	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1a	0/1	1	***[PCFR1]***	0/1	0/1	0/1	0
	UT3RXD	Input	FTU1a	0/1	0	***[PCFR2]***	0/1	0/1	0/1	1
	TSPI3TXD	Output	FTU2a	0/1	1	***[PCFR3]***	0/1	0/1	0/1	0
	T32A03OUTA	Output	FTU1a	0/1	1	***[PCFR4]***	0/1	0/1	0/1	0
	T32A03OUTC	Output	FTU1a	0/1	1	***[PCFR5]***	0/1	0/1	0/1	0
PC1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT10	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT3RXD	Input	FTU1a	0/1	0	***[PCFR1]***	0/1	0/1	0/1	1
	UT3TXDA	Output	FTU1a	0/1	1	***[PCFR2]***	0/1	0/1	0/1	0
	TSPI3RXD	Input	FTU1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
	T32A03INA0	Input	FTU1a	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	T32A03INC0	Input	FTU1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1
PC2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT07b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI3SCK	Input	FTU1a	0/1	0	***[PCFR3]***	0/1	0/1	0/1	1
		Output			1					0
	T32A03INA1	Input	FTU1a	0/1	0	***[PCFR4]***	0/1	0/1	0/1	1
	T32A03INC1	Input	FTU1a	0/1	0	***[PCFR5]***	0/1	0/1	0/1	1

4.2.5. PORT D

Table 4.6 Port D Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PDDATA]	*[PDCR]*	*[PDFRn]*	*[PDOD]*	*[PDPUP]*	*[PDPDN]*	*[PDIE]*
PD0	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA11/ AINB11 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD1	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA12/ AINB12 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD2	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA10/ AINB10 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD3	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA09/ AINB09 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD4	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA08/ AINB08 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD5	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA07/ AINB07 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PD6	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	AINA06/ AINB06 (Note)	Input	FTU5a	0/1	0	0	0/1	0	0	0
	EMG0	Input	FTU1a	0/1	0	***[PDFR5]***	0/1	0/1	0/1	1

Note: When using as the analog input pins (AINAx/AINBx), ***[PDIE]*** should be set to disable input "0", ***[PDCR]*** should be set to disable output "0", ***[PDPUP]*** should be set to disable pull-up "0", and ***[PDPDN]*** should be set to disabled pull-down "0".

4.2.6. PORT E

Table 4.7 Port E Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PEDATA]	*[PECR]*	*[PEFRn]*	*[PEOD]*	*[PEPUP]*	*[PEPDN]*	*[PEIE]*
PE0	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA05/ AINB05 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PE1	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA04/ AINB04 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PE2	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA03/ AINB03 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PE3	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA02/ AINB02 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0
PE4	After reset	-	-	0	0	N/A	0	0	0	0
	Input Port	Input	-	0/1	0	N/A	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	N/A	0/1	0/1	0/1	0
	AINA01/ AINB01 (Note)	Input	FTU5a	0/1	0	N/A	0/1	0	0	0

Note: When using as analog input pins (AINAx/AINBx), ***[PEIE]*** should be set to disable input "0", ***[PECR]*** should be set to disable output "0", ***[PEPUP]*** should be set to disable pull-up "0", and ***[PEPDN]*** should be set to disable pull-down "0".

4.2.7. PORT F

Table 4.8 Port F Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PFDATA]	*[PFCR]*	*[PFFRn]*	*[PFOD]*	*[PFPUP]*	*[PFPDN]*	*[PFIE]*
PF0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	T32A04OUTA	Output	FTU1a	0/1	1	***[PFFR4]***	0/1	0/1	0/1	0
	T32A04OUTC	Output	FTU1a	0/1	1	***[PFFR5]***	0/1	0/1	0/1	0
	TRGIN0	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1
	EMG1	Input	FTU1a	0/1	0	***[PFFR7]***	0/1	0/1	0/1	1
PF1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT00b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A04INA0	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A04INC0	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
PF2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT01b	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	T32A04INA1	Input	FTU1a	0/1	0	***[PFFR4]***	0/1	0/1	0/1	1
	T32A04INC1	Input	FTU1a	0/1	0	***[PFFR5]***	0/1	0/1	0/1	1
	TRGIN2	Input	FTU1a	0/1	0	***[PFFR6]***	0/1	0/1	0/1	1

4.2.8. PORT G

Table 4.9 Port G Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PGDATA]	*[PGCR]*	*[PGFRn]*	*[PGOD]*	*[PGPUP]*	*[PGPDN]*	*[PGIE]*
PG0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT04	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2TXDA	Output	FTU1a	0/1	1	***[PGFR1]***	0/1	0/1	0/1	0
	TSPI2TXD	Output	FTU2a	0/1	1	***[PGFR2]***	0/1	0/1	0/1	0
	T32A02OUTA	Output	FTU1a	0/1	1	***[PGFR3]***	0/1	0/1	0/1	0
	T32A02OUTC	Output	FTU1a	0/1	1	***[PGFR4]***	0/1	0/1	0/1	0
	ENC0A	Input	FTU1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	UO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FTU1a	0/1	1	***[PGFR7]***	0/1	0/1	0/1	0
PG1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT05	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT2RXD	Input	FTU1a	0/1	0	***[PGFR1]***	0/1	0/1	0/1	1
	TSPI2RXD	Input	FTU1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
	T32A02INA0	Input	FTU1a	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A02INC0	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	ENC0B	Input	FTU1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	VO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
	PMD1DBG	Output	FTU1a	0/1	1	***[PGFR7]***	0/1	0/1	0/1	0
PG2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	TSPI2SCK	Input	FTU1a	0/1	0	***[PGFR2]***	0/1	0/1	0/1	1
		Output			1					0
	T32A02INA1	Input	FTU1a	0/1	0	***[PGFR3]***	0/1	0/1	0/1	1
	T32A02INC1	Input	FTU1a	0/1	0	***[PGFR4]***	0/1	0/1	0/1	1
	ENC0Z	Input	FTU1a	0/1	0	***[PGFR5]***	0/1	0/1	0/1	1
	WO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG3	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	XO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG4	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	YO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0
PG5	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ZO1	Output	FTU2a	0/1	1	***[PGFR6]***	0/1	0/1	0/1	0

4.2.9. PORT H

Table 4.10 Port H Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PHDATA]	*[PHCR]*	*[PHFRn]*	*[PHOD]*	*[PHPUP]*	*[PHPDN]*	*[PHIE]*
PH0	After reset	-	-	0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input	-	0/1	N/A	N/A	N/A	N/A	0/1	1
	X1	Input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0
	EHCLKIN	Input	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0/1
PH1	After reset	-	-	0	N/A	N/A	N/A	N/A	0	0
	Input Port	Input	-	0/1	N/A	N/A	N/A	N/A	0/1	1
	X2	Output	FTU11a	0/1	N/A	N/A	N/A	N/A	0	0
PH2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FTU1a	0/1	0	***[PHFR5]***	0/1	0/1	0/1	1
PH3	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0

4.2.10. PORT J

Table 4.11 Port J Register Settings

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PJDATA]	*[PJCR]*	*[PJFRn]*	*[PJOD]*	*[PJPUP]*	*[PJPDN]*	*[PJIE]*
PJ0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	UO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	SCOUT	Output	FTU1a	0/1	1	***[PJFR6]***	0/1	0/1	0/1	0
	PMD0DBG	Output	FTU1a	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
PJ1	After reset	-	-	0	0	0	0	0		0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	XO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
	PMD1DBG	Output	FTU1a	0/1	1	***[PJFR7]***	0/1	0/1	0/1	0
PJ2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	VO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ3	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ENC1Z	Input	FTU1a	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	YO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ4	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ENC1B	Input	FTU1a	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	WO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ5	After reset	Input	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	ENC1A	Input	FTU1a	0/1	0	***[PJFR4]***	0/1	0/1	0/1	1
	ZO0	Output	FTU2a	0/1	1	***[PJFR5]***	0/1	0/1	0/1	0
PJ6	During reset (BOOT_N)	Input	FTU16a	0	0	0	0	0 (Note)	0	0 (Note)
	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	EMG0	Input	FTU1a	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1
PJ7	After reset	Input	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	OVV0	Input	FTU1a	0/1	0	***[PJFR5]***	0/1	0/1	0/1	1

Note: During the reset period by the reset pin (RESET_N), the state of the BOOT_N pin can be input to PJ6 with pull-up enabled and input enabled.

4.2.11. PORT K

Table 4.12 Port K Register Settings

PORT	Reset status / Function	Input/Output	PORT type	Control register						
				[PKDATA]	*[PKCR]*	*[PKFRn]*	*[PKOD]*	*[PKPUP]*	*[PKPDN]*	*[PKIE]*
PK0	After reset (TDI)	Input	FTU2a	0	0	***[PKFR7]***	0	1	0	1
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT00a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FTU1a	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	T32A00OUTA	Output	FTU1a	0/1	1	***[PKFR4]***	0/1	0/1	0/1	0
	T32A00OUTC	Output	FTU1a	0/1	1	***[PKFR5]***	0/1	0/1	0/1	0
PK1	After reset (TDO/SWV)	Output	FTU2a	0	1 (Note)	***[PKFR7]***	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT01a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	T32A00INA0	Input	FTU1a	0/1	0	***[PKFR4]***	0/1	0/1	0/1	1
	T32A00INC0	Input	FTU1a	0/1	0	***[PKFR5]***	0/1	0/1	0/1	1
PK2	After reset (TMS/SWDIO)	Input/Output	FTU2a	0	1 (Note)	***[PKFR7]***	0	1	0	1
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT02a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0RXD	Input	FTU1a	0/1	0	***[PKFR1]***	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PKFR2]***	0/1	0/1	0/1	0
	TSPI0RXD	Input	FTU1a	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
PK3	After reset (TCK/SWCLK)	Input	FTU2a	0	0	***[PKFR7]***	0	0	1	1
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT03a	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	UT0TXDA	Output	FTU1a	0/1	1	***[PKFR1]***	0/1	0/1	0/1	0
	UT0RXD	Input	FTU1a	0/1	0	***[PKFR2]***	0/1	0/1	0/1	1
	TSPI0TXD	Output	FTU2a	0/1	1	***[PKFR3]***	0/1	0/1	0/1	0
PK4	After reset (TRST_N)	Input	FTU3a	0	0	***[PKFR7]***	0	1	0	1
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	INT06	Input	FTU4a	0/1	0	0	0/1	0/1	0/1	1
	TSPI0SCK	Input	FTU1a	0/1	0	***[PKFR3]***	0/1	0/1	0/1	1
		Output			1					0
	NBDSYNC	Input	FTU3a	0/1	0	***[PKFR6]***	0/1	0/1	0/1	1

Note: These pins are enabled to output after receiving the command from a debug tool.

4.2.12. PORT L

Table 4.13 Port L Register Settings

PORT	Reset status / Function	Input/Output	Port type	Control register						
				[PLDATA]	*[PLCR]*	*[PLFRn]*	*[PLOD]*	*[PLPUP]*	*[PLPDN]*	*[PLIE]*
PL0	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	NBDDATA0	Input/Output	FTU2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA0	Output	FTU1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL1	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	NBDDATA1	Input/Output	FTU2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA1	Output	FTU1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL2	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	NBDDATA2	Input/Output	FTU2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA2	Output	FTU1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL3	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	NBDDATA3	Input/Output	FTU2c	0/1	1	***[PLFR6]***	0/1	0/1	0	1
	TRACEDATA3	Output	FTU1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0
PL4	After reset	-	-	0	0	0	0	0	0	0
	Input Port	Input	-	0/1	0	0	0/1	0/1	0/1	1
	Output Port	Output	-	0/1	1	0	0/1	0/1	0/1	0
	NBDCLK	Input	FTU3a	0/1	0	***[PLFR6]***	0/1	0/1	0/1	1
	TRACECLK	Output	FTU1a	0/1	1	***[PLFR7]***	0/1	0/1	0/1	0

5. Port Circuit Diagram

The port has 8 types of circuits, FTU1a to FTU5a, FTU11a and FTU16a. Each circuit diagram is shown in the following page and after. The dot line block shows "Equivalent Circuit" which is described in "Datasheet".

The "I/O Reset" shown in the circuit diagram is described the power on reset (POR).

5.1. Type FTU1a

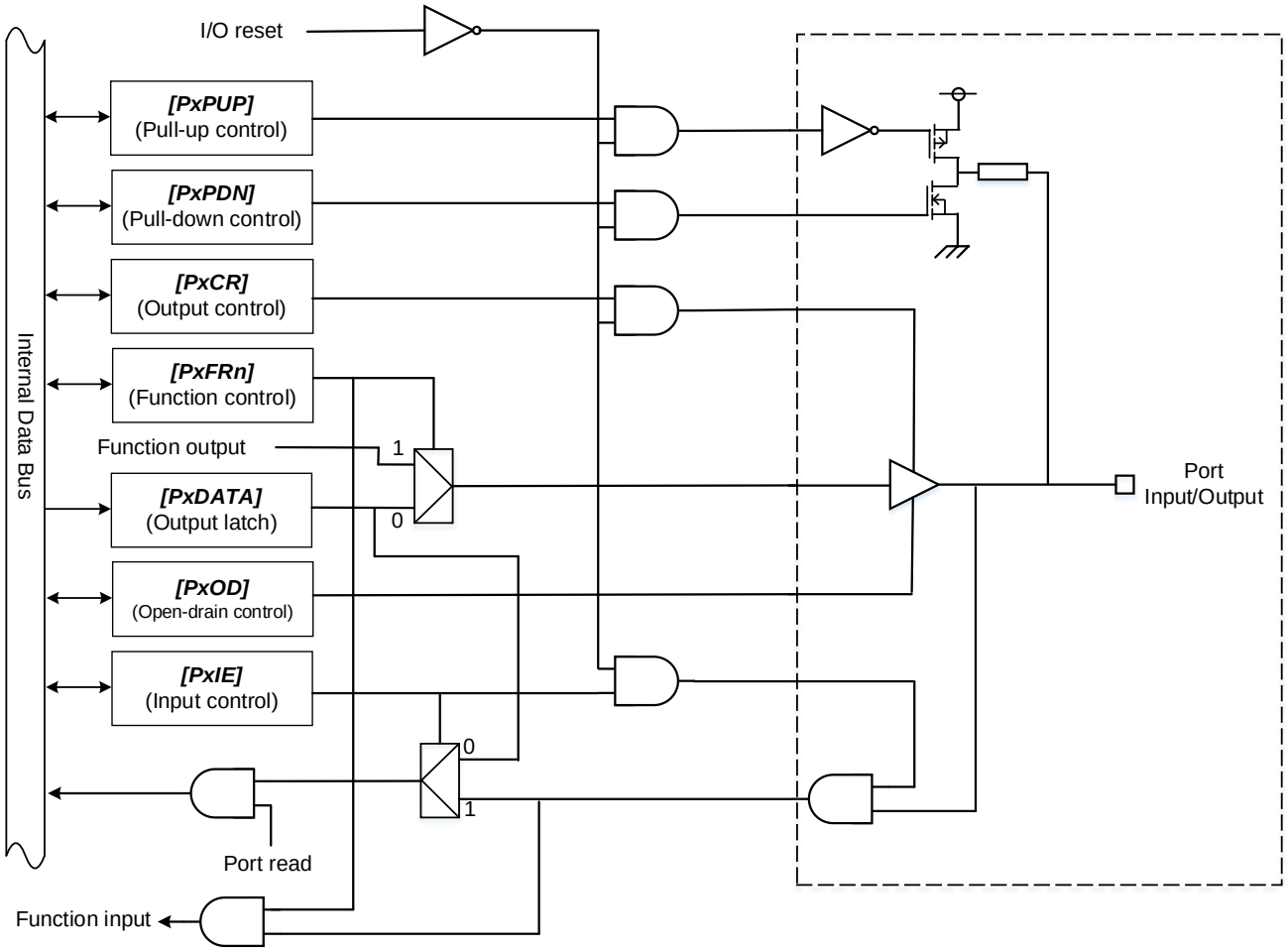

Figure 5.1 Port Type FTU1a

5.2. Type FTU2a

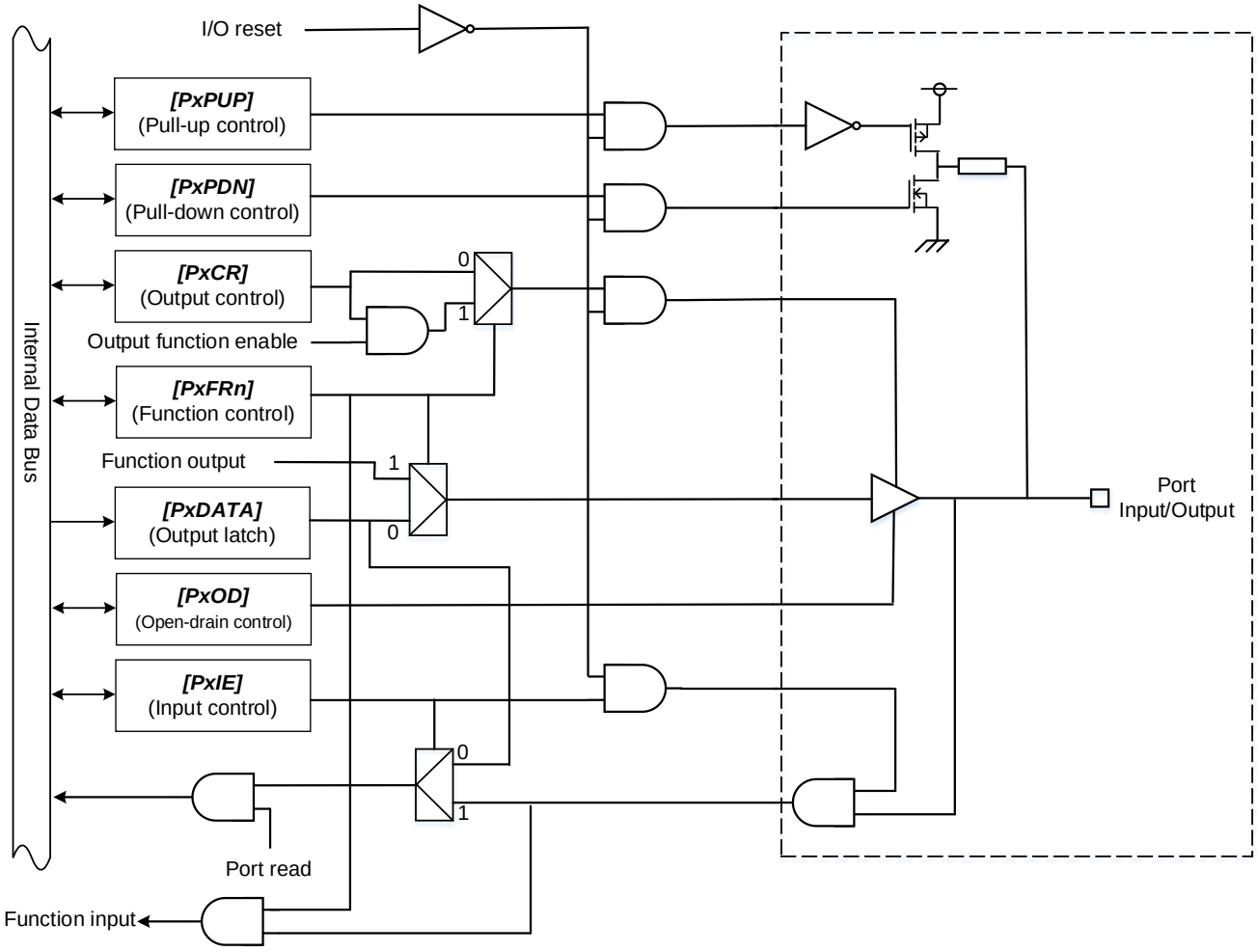

Figure 5.2 Port Type FTU2a

5.3. Type FTU2c

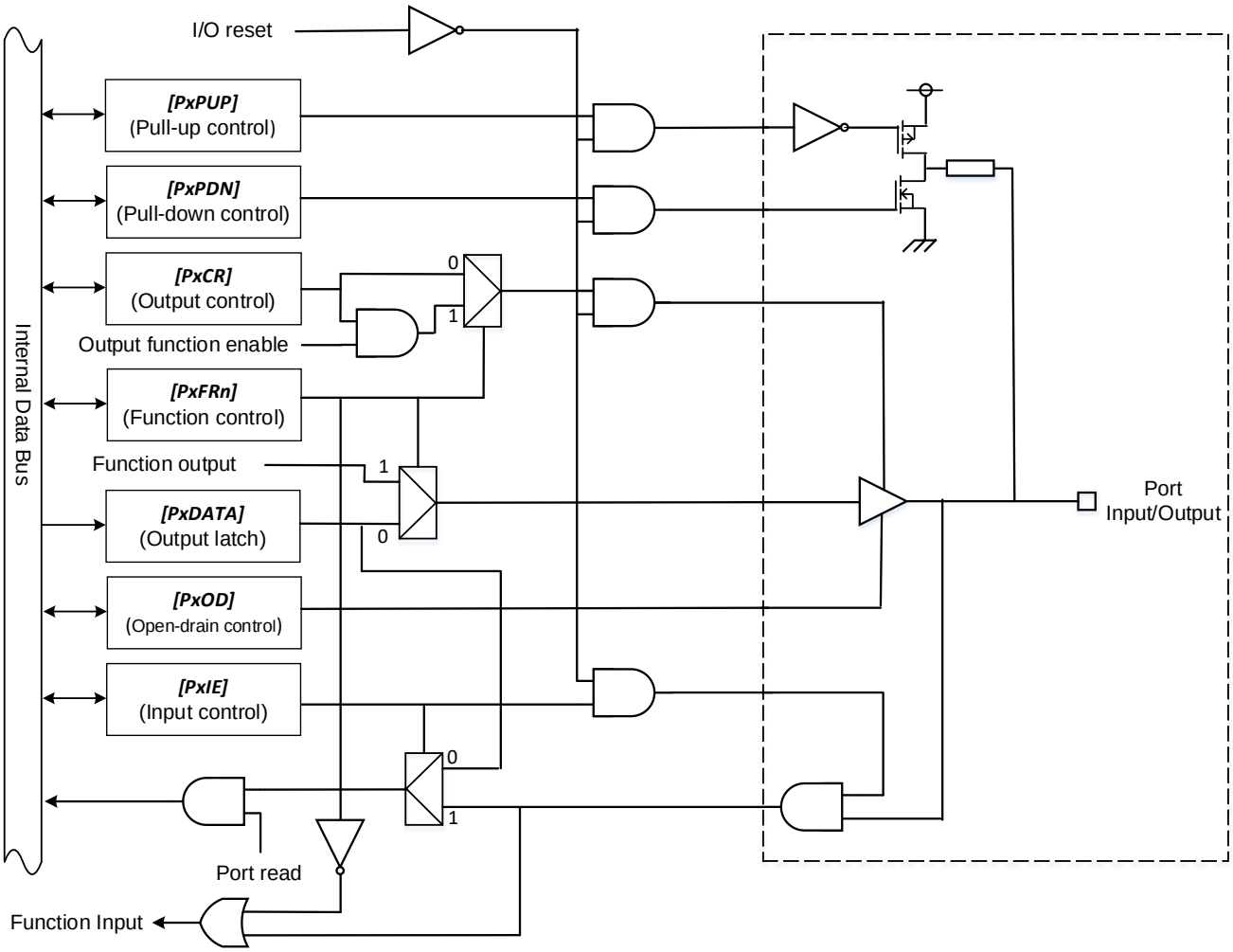

Figure 5.3 Port Type FTU2c

5.4. Type FTU3a

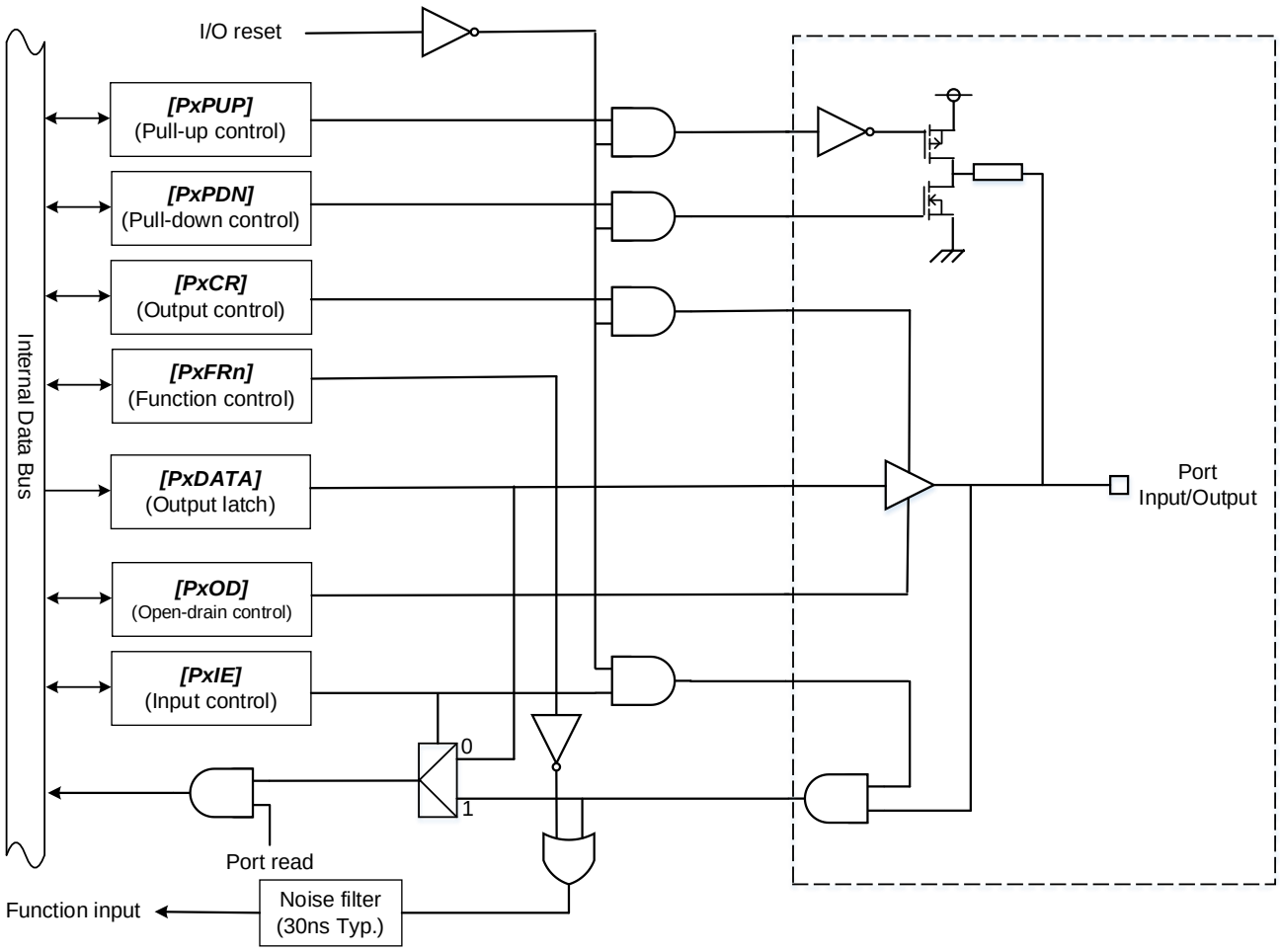

Figure 5.4 Port Type FTU3a

5.5. Type FTU4a

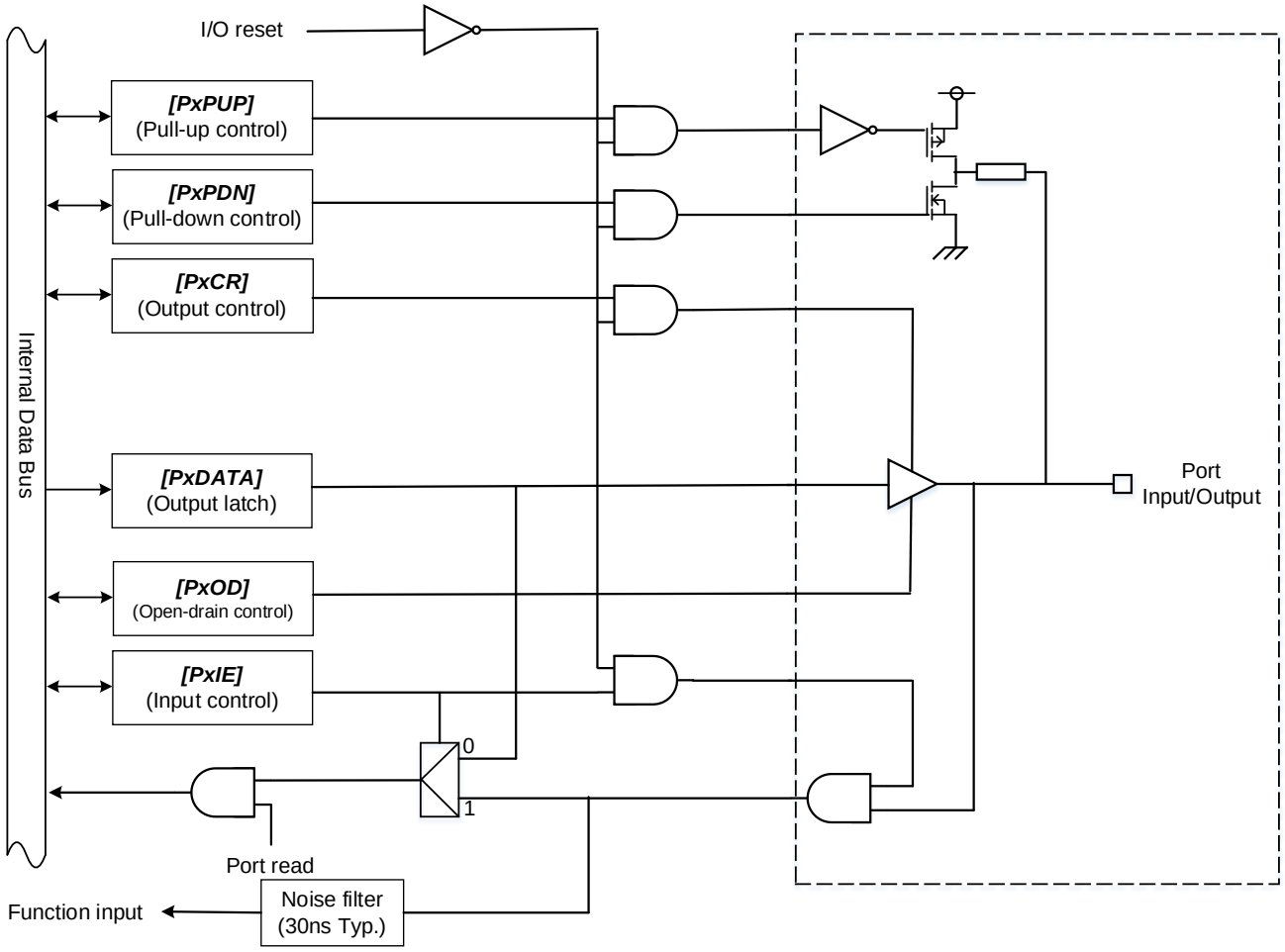

Figure 5.5 Port Type FTU4a

5.6. Type FTU5a

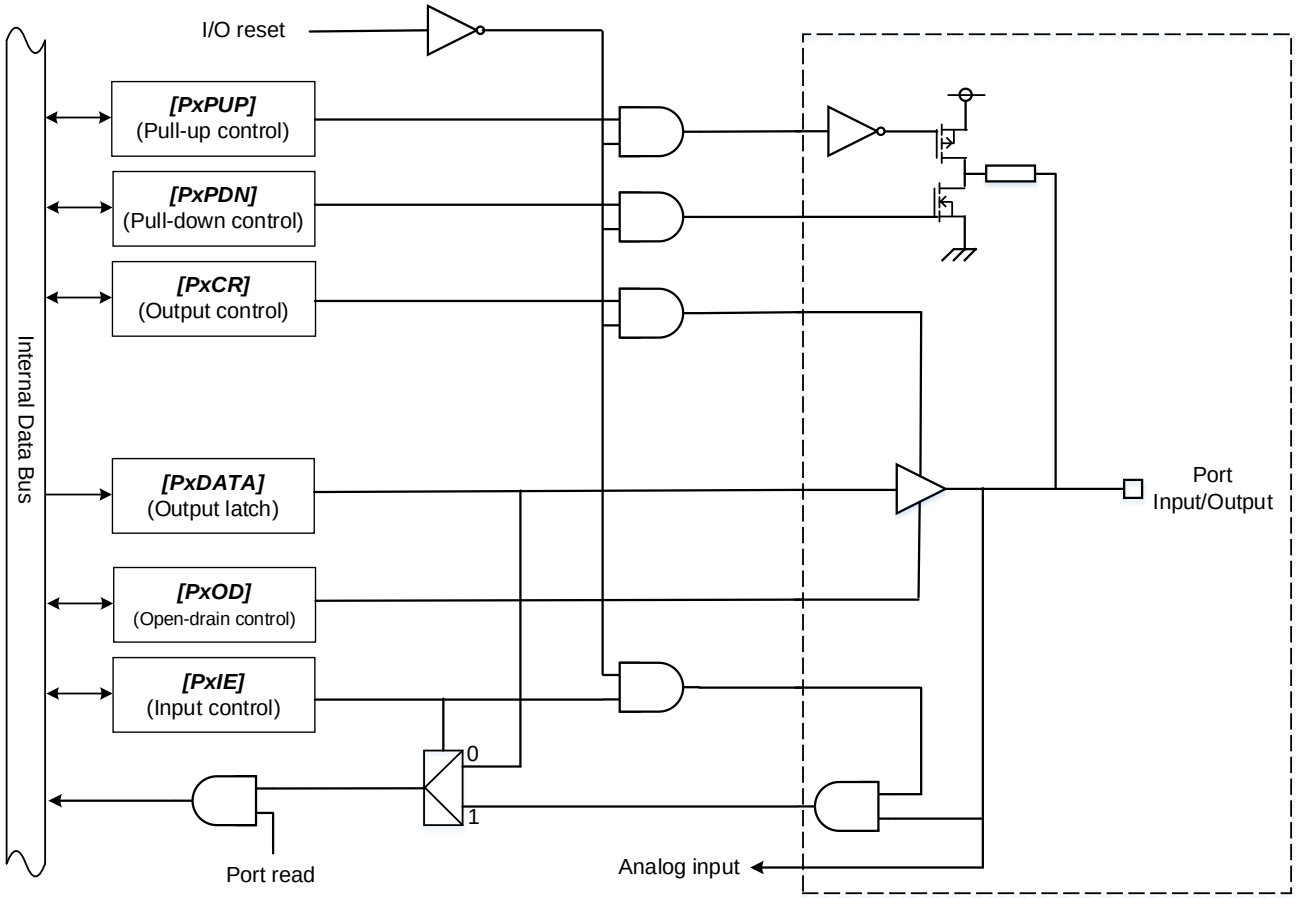

Figure 5.6 Port Type FTU5a

5.7. Type FTU11a

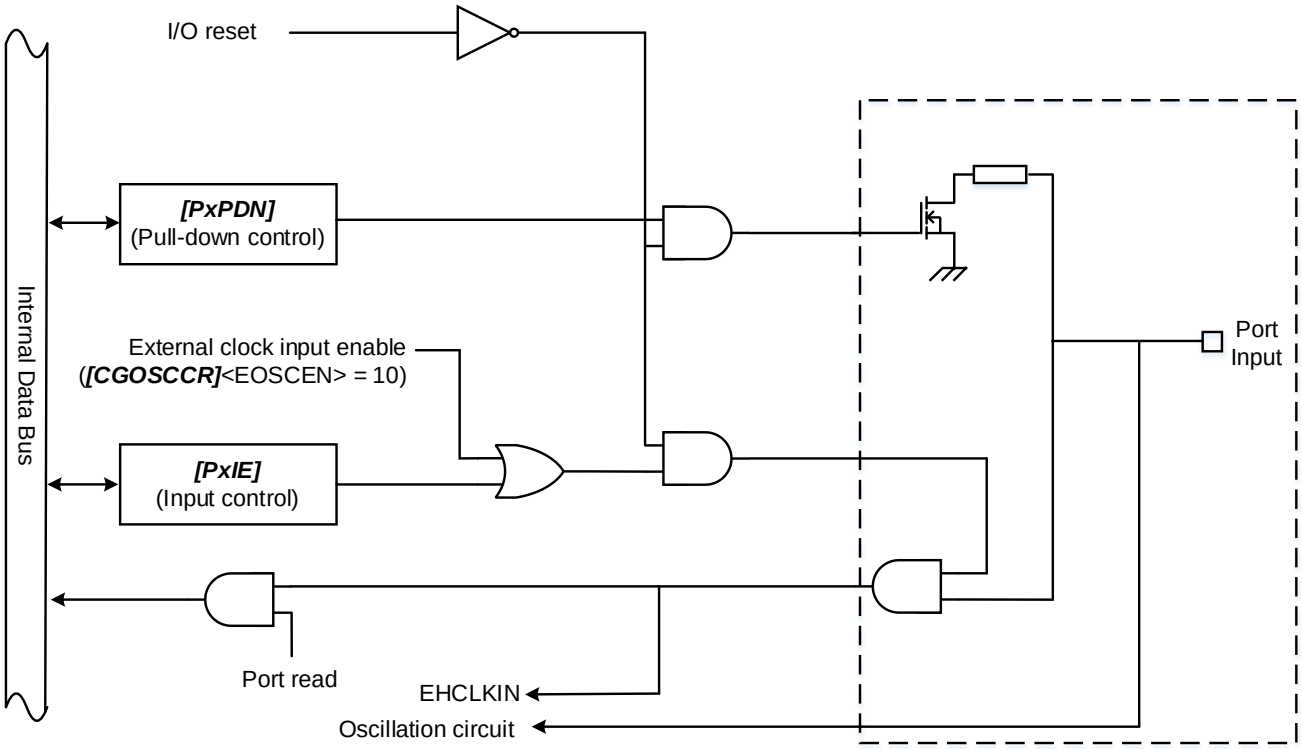

Figure 5.7 Port Type FTU11a

5.8. Type FTU16a

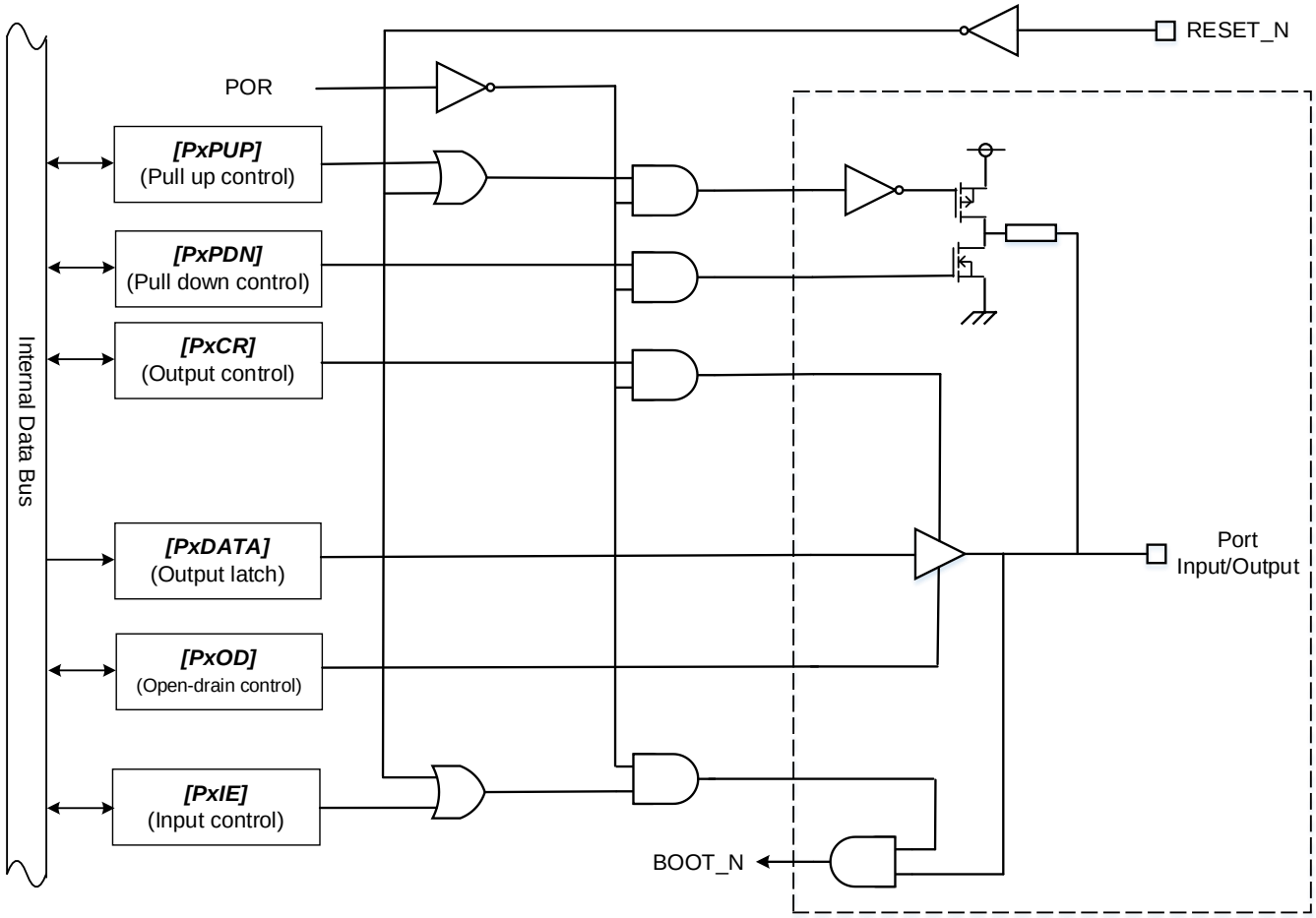

Figure 5.8 Port Type FTU16a

6. Precaution

6.1. Pin Status During Reset Period

During the reset period, the pin status is high impedance except for below pins. And, the pull-up/pull-down is disabled.

- The debug interface alternate pins (PK0 to PK4) are used as debug pins.
- PJ6 (BOOT_N) is enabled to input and pulled-up during reset period by RESET_N pin.
  At the rising edge of the RESET_N pin, if PJ6 is "High" level, MCU enters single chip mode and boots from the on-chip flash memory.
  If PJ6 is "Low" level, MCU enters single BOOT mode and boots from the internal BOOT ROM.

6.2. Unused Pins

We recommend that each unused pin should be connected to the power supply pin or GND pin via resistor.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

6.3. Important Points of Using Debug Interface Pins Used as General-purpose Ports

After releasing reset, if the debug interface pins are used as the general I/O ports by the user program, the debug tool cannot be connected with MCU and control the MCU.

When the debug tool cannot debug the MCU, it can be connected with the MCU again by setting the MCU to the single BOOT mode and erasing the internal flash memory via the UART.

For details, refer to the Reference Manual "Flash memory".

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
1.0	2024-07-22	- First release

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