

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# XPN52016MC

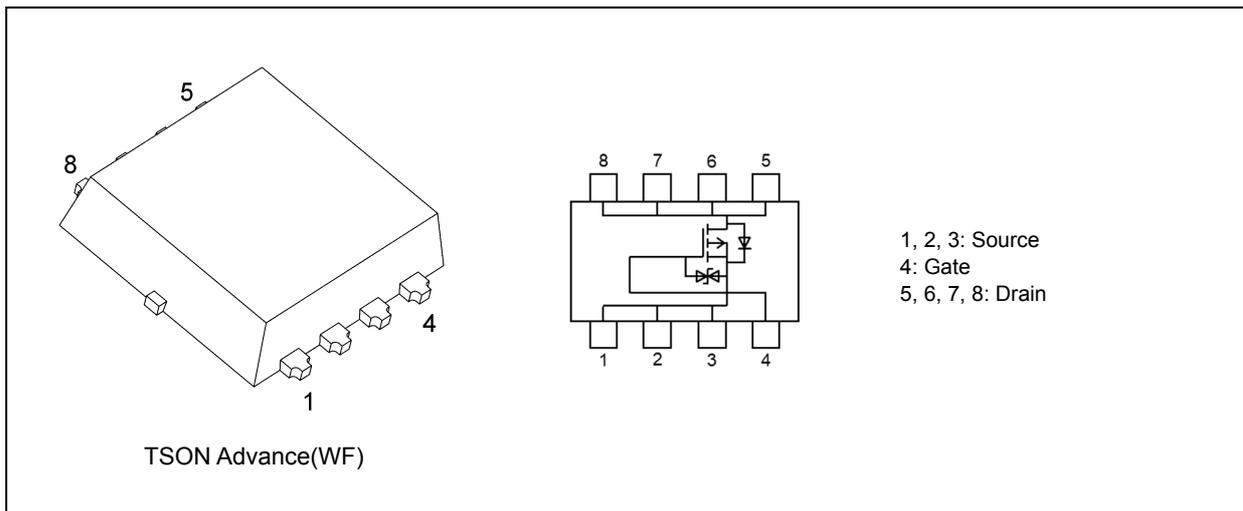
## 1. Applications

- Automotive
- Switching Voltage Regulators
- DC-DC Converters
- Motor Drivers

## 2. Features

- (1) AEC-Q101 qualified
- (2) Small, thin package
- (3) Low drain-source on-resistance:  $R_{DS(ON)} = 40.0 \text{ m}\Omega$  (typ.) ( $V_{GS} = -10 \text{ V}$ )
- (4) Low leakage current:  $I_{DSS} = -10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = -60 \text{ V}$ )
- (5) Enhancement mode:  $V_{th} = -1.0$  to  $-2.1 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -0.2 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2024-10

### 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics  | Symbol    | Rating     | Unit             |
|--|-----------|------------|------------------|
| Drain-source voltage                                   | $V_{DSS}$ | -60        | V                |
| Gate-source voltage                                    | $V_{GSS}$ | +10/-20    |                  |
| Drain current (DC) (Note 1)                            | $I_D$     | -15        | A                |
| Drain current (pulsed) (Note 1)                        | $I_{DP}$  | -30        |                  |
| Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ ) | $P_D$     | 65         | W                |
| Power dissipation ( $t = 10\text{ s}$ ) (Note 2)       |           | 2.27       |                  |
| Power dissipation ( $t = 10\text{ s}$ ) (Note 3)       |           | 0.84       |                  |
| Single-pulse avalanche energy (Note 4)                 | $E_{AS}$  | 20         | mJ               |
| Single-pulse avalanche current                         | $I_{AS}$  | -15        | A                |
| Channel temperature (Note 5)                           | $T_{ch}$  | 175        | $^\circ\text{C}$ |
| Storage temperature (Note 5)                           | $T_{stg}$ | -55 to 175 |                  |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### 5. Thermal Characteristics

| Characteristics  | Symbol         | Max | Unit               |
|--|----------------|-----|--------------------|
| Channel-to-case thermal impedance ( $T_c = 25\text{ }^\circ\text{C}$ ) | $Z_{th(ch-c)}$ | 2.3 | $^\circ\text{C/W}$ |
| Channel-to-ambient thermal impedance ( $t = 10\text{ s}$ ) (Note 2)    | $Z_{th(ch-a)}$ | 66  |                    |
| Channel-to-ambient thermal impedance ( $t = 10\text{ s}$ ) (Note 3)    | $Z_{th(ch-a)}$ | 178 |                    |

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4:  $V_{DD} = -48\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 67\text{ }\mu\text{H}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = -15\text{ A}$ ,  $V_{GS} = 0/-15\text{ V}$

Note 5: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

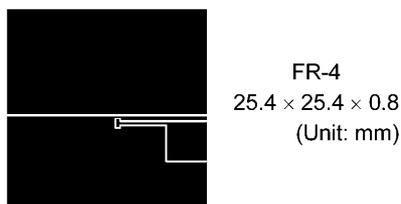


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

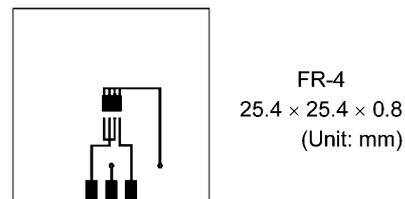


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol        | Test Condition                                   | Min  | Typ. | Max      | Unit             |
|--------------------------------|---------------|--|------|------|----------|------------------|
| Gate leakage current           | $I_{GSS}$     | $V_{GS} = +10/-16\text{ V}, V_{DS} = 0\text{ V}$ | —    | —    | $\pm 10$ | $\mu\text{A}$    |
| Drain cut-off current          | $I_{DSS}$     | $V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$     | —    | —    | -10      |                  |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$       | -60  | —    | —        | V                |
|                                | $V_{(BR)DSX}$ | $I_D = -10\text{ mA}, V_{GS} = 10\text{ V}$      | -50  | —    | —        |                  |
| Gate threshold voltage         | $V_{th}$      | $V_{DS} = -10\text{ V}, I_D = -0.2\text{ mA}$    | -1.0 | —    | -2.1     |                  |
| Drain-source on-resistance     | $R_{DS(ON)}$  | $V_{GS} = -4.5\text{ V}, I_D = -7.5\text{ A}$    | —    | 44.0 | 66.0     | $\text{m}\Omega$ |
|                                |               | $V_{GS} = -10\text{ V}, I_D = -7.5\text{ A}$     | —    | 40.0 | 52.0     |                  |

#### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition   | Min | Typ. | Max  | Unit        |
|--------------------------------|-----------|--|-----|------|------|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | —   | 1680 | 2360 | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |  | —   | 130  | 182  |             |
| Output capacitance             | $C_{oss}$ |  | —   | 170  | —    |             |
| Gate resistance                | $r_g$     |  | —   | 13   | 26   | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Fig. 6.2.1   | —   | 25   | —    | ns          |
| Switching time (turn-on time)  | $t_{on}$  | See Fig. 6.2.1   | —   | 33   | —    |             |
| Switching time (fall time)     | $t_f$     |  | —   | 108  | —    | ns          |
| Switching time (turn-off time) | $t_{off}$ |  | —   | 401  | —    |             |

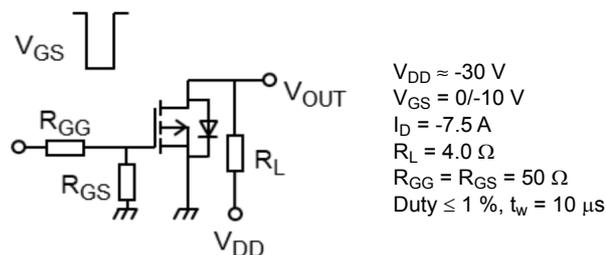


Fig. 6.2.1 Switching Time Test Circuit

#### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

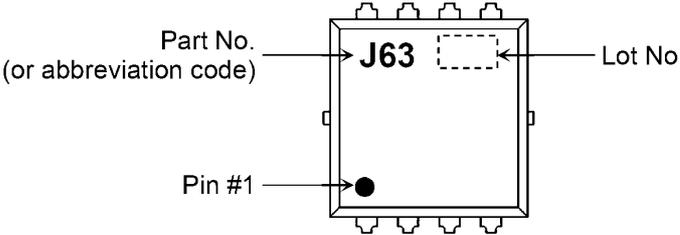
| Characteristics                                 | Symbol    | Test Condition   | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx -48\text{ V}, V_{GS} = -10\text{ V}, I_D = -15\text{ A}$ | —   | 47   | —   | nC   |
| Gate-source charge 1                            | $Q_{gs1}$ |  | —   | 4    | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |  | —   | 12   | —   |      |

#### 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol    | Test Condition   | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Reverse drain current (DC) (Note 6)     | $I_{DR}$  | —  | —   | —    | -15 | A    |
| Reverse drain current (pulsed) (Note 6) | $I_{DRP}$ | —  | —   | —    | -30 | A    |
| Diode forward voltage                   | $V_{DSF}$ | $I_{DR} = -15\text{ A}, V_{GS} = 0\text{ V}$   | —   | —    | 1.2 | V    |
| Reverse recovery time                   | $t_{rr}$  | $I_{DR} = -15\text{ A}, V_{GS} = 0\text{ V}$<br>$dI_{DR}/dt = 50\text{ A}/\mu\text{s}$ | —   | 40   | —   | ns   |
| Reverse recovery charge                 | $Q_{rr}$  |  | —   | 20   | —   |      |

Note 6: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

**7. Marking**



**Fig. 7.1 Marking**

## 8. Characteristics Curves (Note)

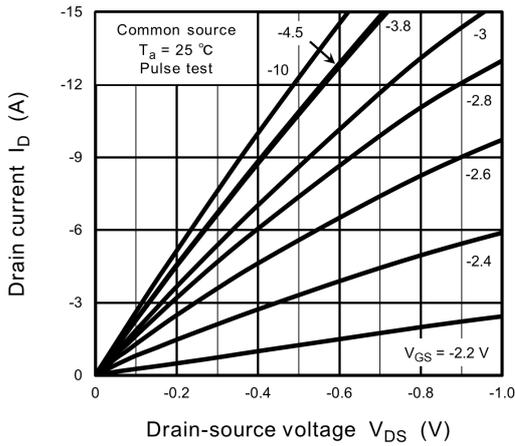


Fig. 8.1  $I_D - V_{DS}$

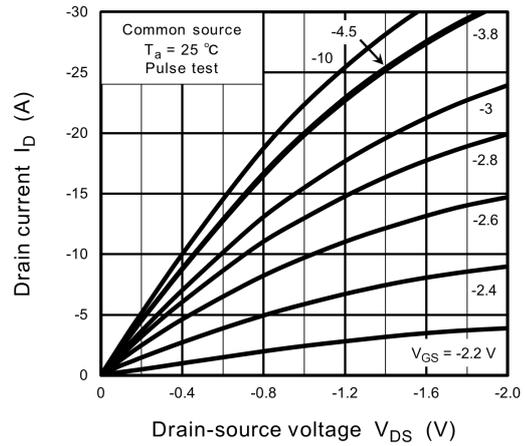


Fig. 8.2  $I_D - V_{DS}$

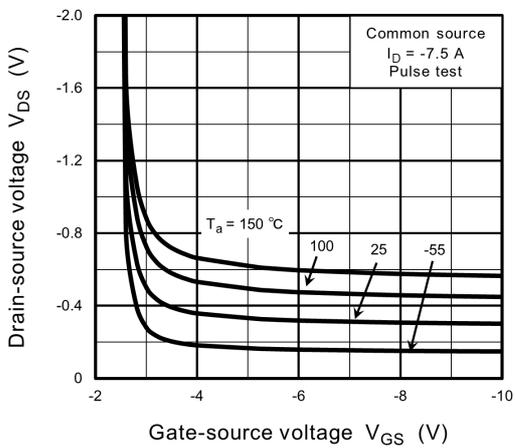


Fig. 8.3  $V_{DS} - V_{GS}$

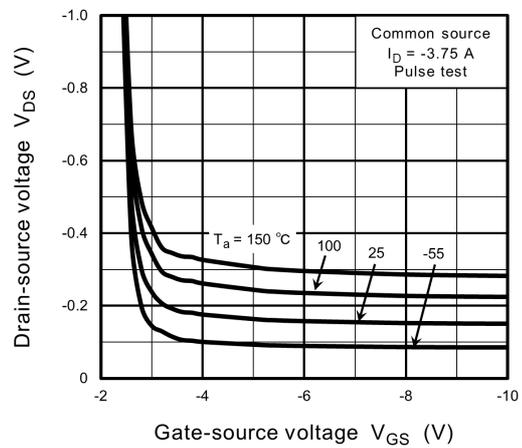


Fig. 8.4  $V_{DS} - V_{GS}$

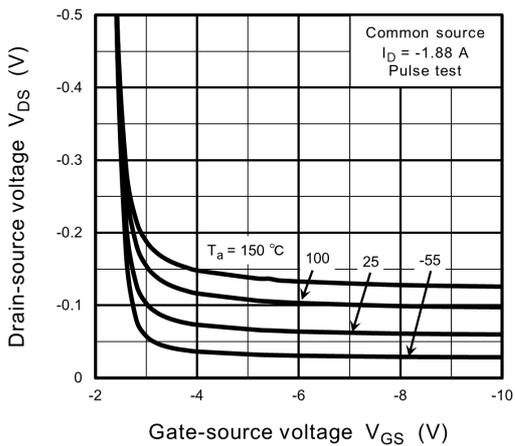


Fig. 8.5  $V_{DS} - V_{GS}$

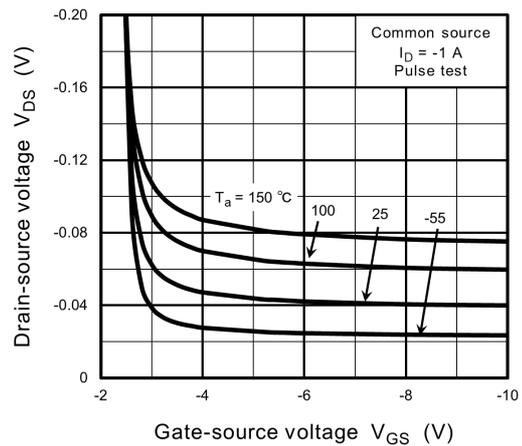
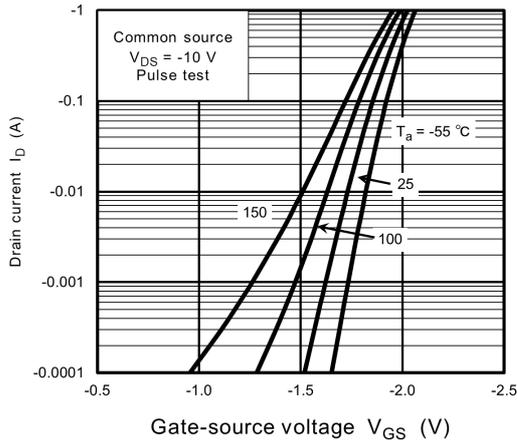
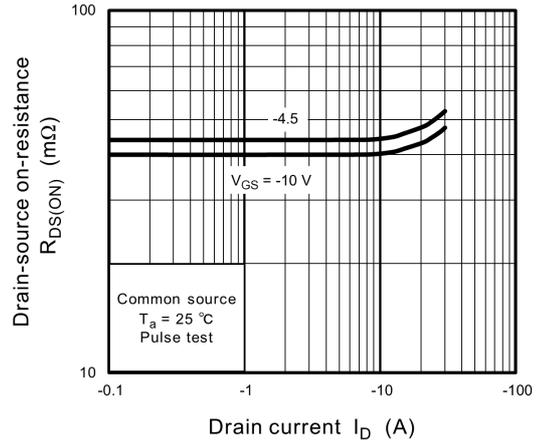


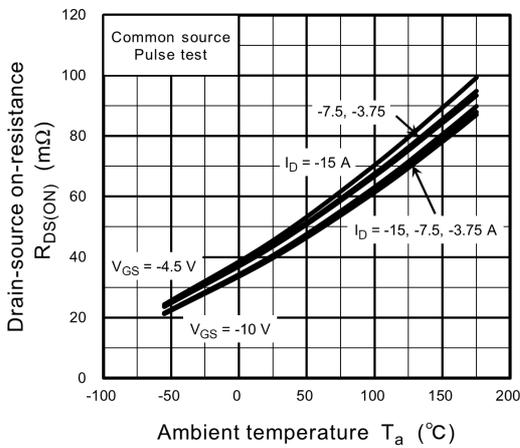
Fig. 8.6  $V_{DS} - V_{GS}$



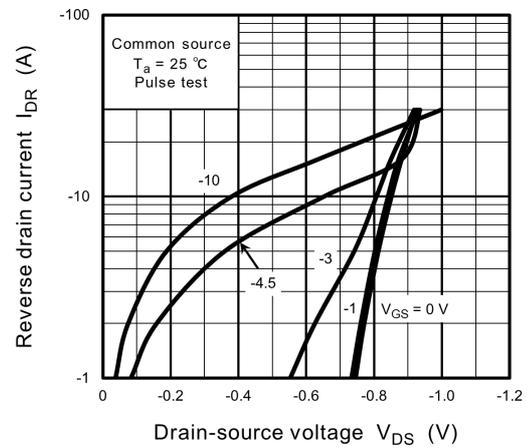
**Fig. 8.7  $I_D - V_{GS}$**



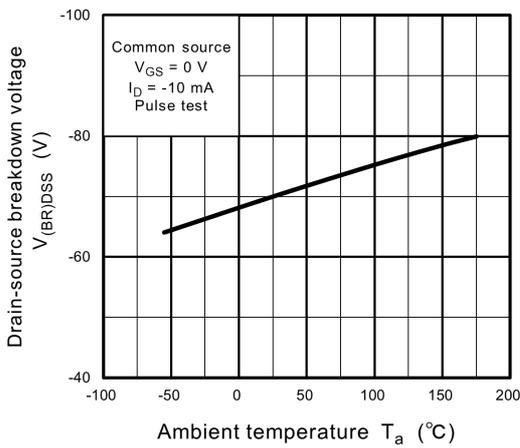
**Fig. 8.8  $R_{DS(ON)} - I_D$**



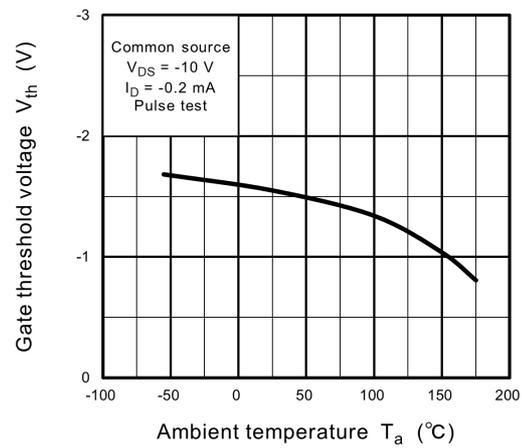
**Fig. 8.9  $R_{DS(ON)} - T_a$**



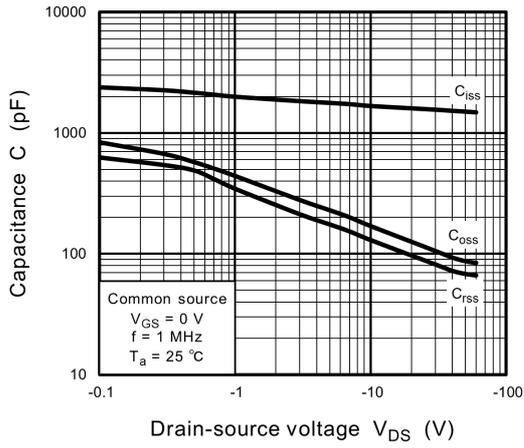
**Fig. 8.10  $I_{DR} - V_{DS}$**



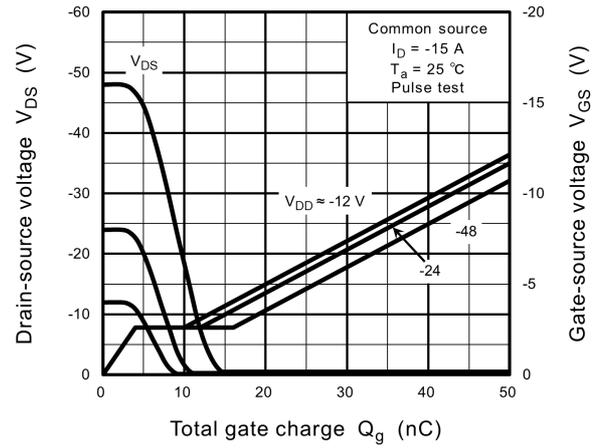
**Fig. 8.11  $V_{(BR)DSS} - T_a$**



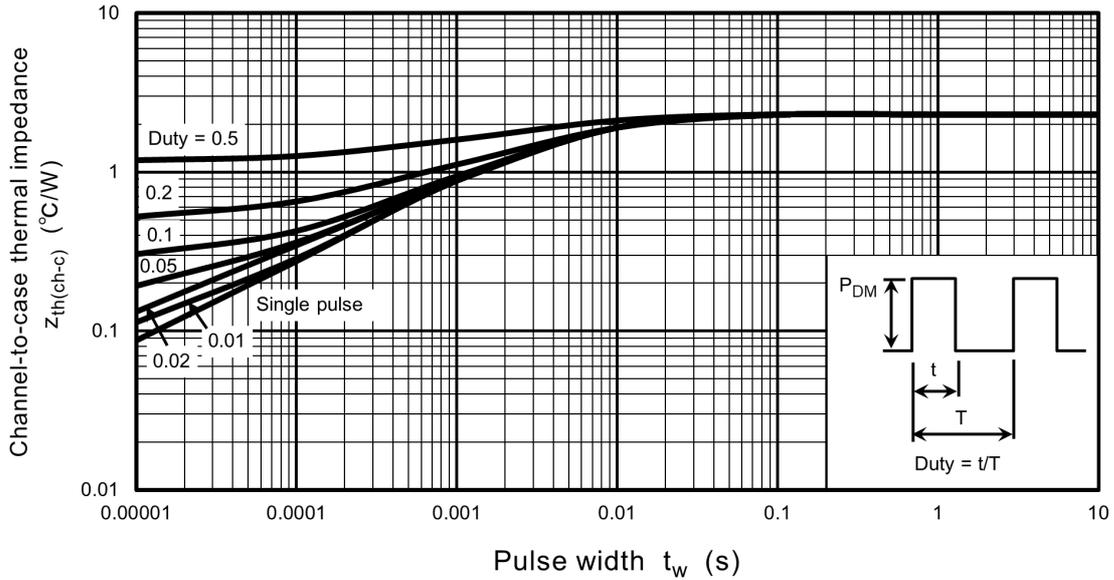
**Fig. 8.12  $V_{th} - T_a$**



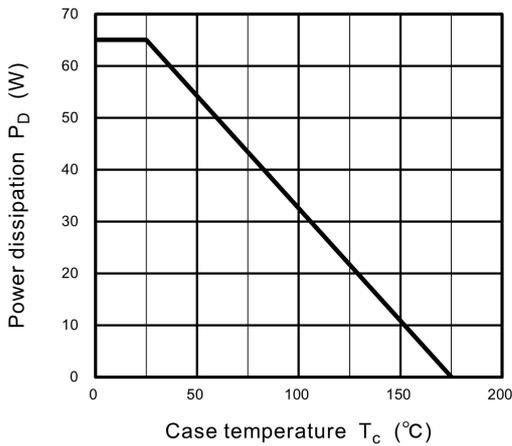
**Fig. 8.13 Capacitance -  $V_{DS}$**



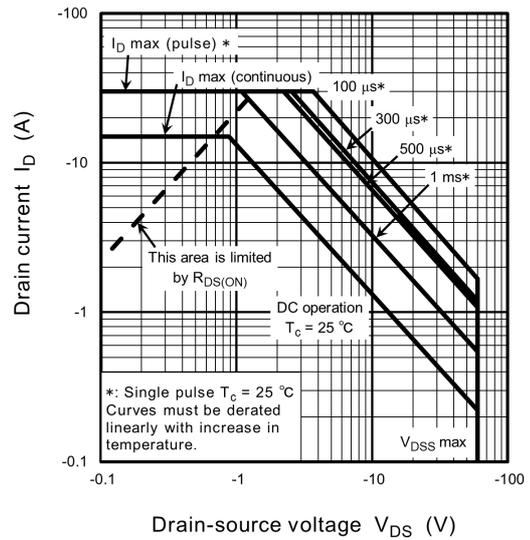
**Fig. 8.14 Dynamic Input/Output Characteristics**



**Fig. 8.15  $Z_{th(ch-c)} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.16  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.17 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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