32-bit RISC Microcontroller
Reference manual

RAM Parity
(RAMP-B)

Revision 1.1

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Related Document

Document name
Product Information
Exception

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

RAM	Random Access Memory
INT	Interrupt

1. Outline

RAM parity function is as follows.

Function classification	Function	Description
RAM parity control	Parity data generation	Generate parity data and save, when write to RAM.
	Parity judgement	Detect error which is judged parity error when read from RAM.
Error detection	Error status	Status of each RAM area saves to status register.
	Error occasion address	Address of error occurred save to address register.
Interrupt	RAM parity interrupt	INTPARIx is generated when parity error occurred.

2. Composition

A RAM parity circuit consists of a parity function control circuit, and parity generating and a judgment circuit.

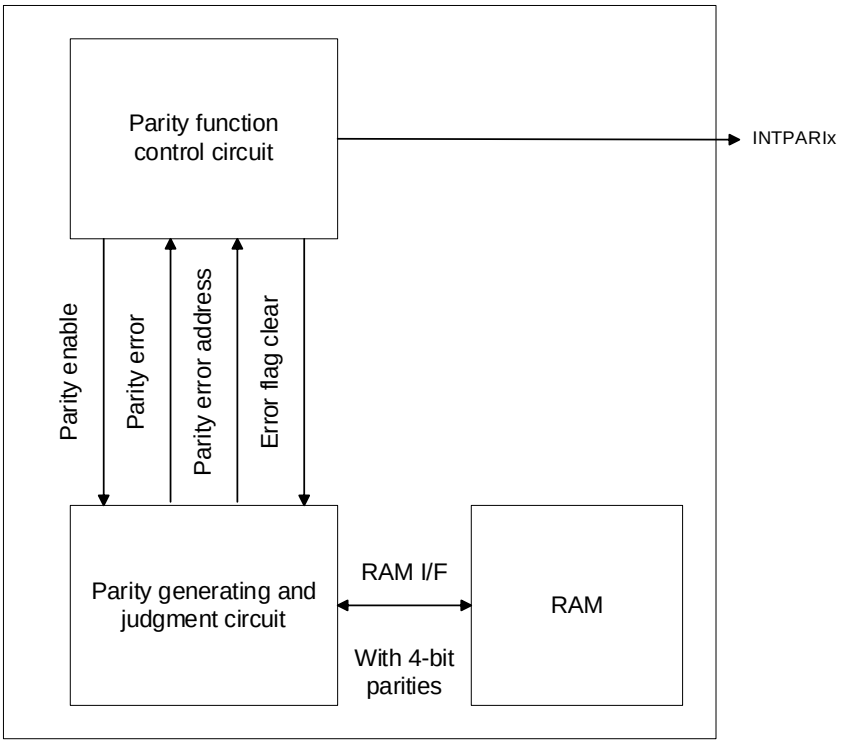

Figure 2.1 Composition of RAM Parity Circuit

Table 2.1 Signal List

No	Symbol	Signal name	I/O	Related reference manual
1	INTPARIx	RAM parity interrupt	Output	Exception, Product Information

3. Operation Description

RAM parity function generates parity data when write to RAM. And read RAM data with parity and do parity check (judgment) the parity. At that time, detected parity error, then generates RAM parity interrupt (INTPARIx).

3.1. Parity Data

1-bit parity is generated and added per byte data. Thus, four bits parity data are generated and added per one word (32 bits).

Note: This circuit generates even parity. Cannot read and write parity data only.

3.2. Operation

Selection of enable/ disable of parity error function control can be performed in ***[RPARxCTL]***<RPAREN>, and selection of enable/ disable of the interrupt output control when parity error detection can be performed in ***[RPARxCTL]***<RPARF>.

[RPARxCTL]<RPAREN>=1 (parity error function enabled) and ***[RPARxCTL]***<RPARF>=0 (interrupt disabled) after reset.

In order to use a parity function normally, initialize all area of RAM first (Note) and set up interrupt.

Note: Since the initial data of RAM is undefined, RAM initialization (data writing) is required with ***[RPARxCTL]***<RPAREN>=1(enable) and ***[RPARxCTL]***<RPARF>=0(disable interrupt) setting before RAM reading.

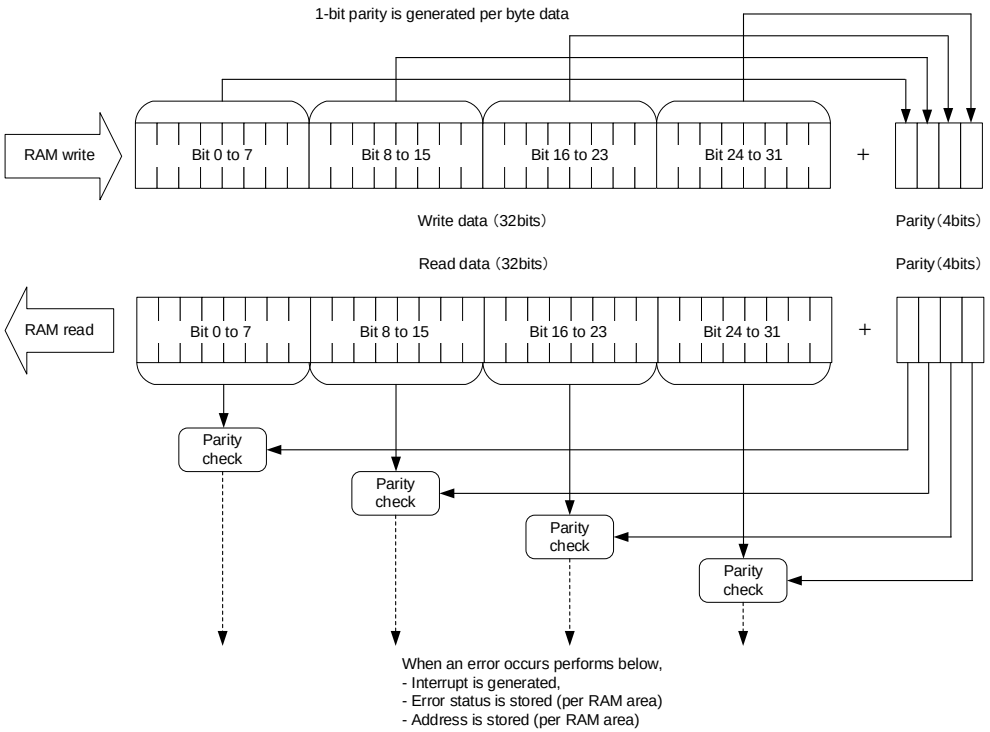

Figure 3.1 RAM Parity Operation

3.3. Error Detection

It can be observed that the RAM parity error was detected by occurrence of INTPARIx.

The RAM area that generated error can be observed by reading the RAM parity status register ***[RPARxST]***<RPARFGn>=1 (error occurrence) in the INTPARIx interrupt service routine. By reading the RAM parity error address register ***[RPARxEADn]*** corresponding to the RAM area where the error occurred, a specific error occurrence address can be obtained.

Note: The quota address of RAM area is different for each product. Please refer to the reference manual "Product Information" for detail.

4. Registers

4.1. Register List

The control registers and their addresses are follows.

Peripheral		Channel/unit	Base address		
			TYPE1	TYPE2	TYPE3
RAM parity	RAMP	ch 0	0x400BBB00	-	0x40043000
		ch 1	-	0x400A3000	-

Note: The channel/unit and base address type are different by products. Please refer to "Product Information" of the reference manual for the details.

Register name		Base address (Base+)
RAM Parity Control Register	***[RPARxCTL]***	0x0000
RAM Parity Status Register	***[RPARxST]***	0x0004
RAM Parity Status Clear Register	***[RPARxCLR]***	0x0008
RAM Parity Error Address Register 0	***[RPARxEAD0]***	0x000C
RAM Parity Error Address Register 1	***[RPARxEAD1]***	0x0010
RAM Parity Error Address Register 2	***[RPARxEAD2]***	0x0014
RAM Parity Error Address Register 3	***[RPARxEAD3]***	0x0018
RAM Parity Error Address Register 4	***[RPARxEAD4]***	0x001C
RAM Parity Error Address Register 5	***[RPARxEAD5]***	0x0020
RAM Parity Error Address Register 6	***[RPARxEAD6]***	0x0024
RAM Parity Error Address Register 7	***[RPARxEAD7]***	0x0028

4.2. Detail of Registers

4.2.1. *[RPARxCTL]* (RAM Parity Control Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as "0"
1	RPARF	0	R/W	Interrupt output control at a parity error occurred (Note2) 1: Enabled 0: Disabled
0	RPAREN	1	R/W	Parity error detection function control (Note1) (Note2) 1: Enabled 0: Disabled

Note1: When set to <RPAREN>=0 (disabled), the parity generation and the parity storage, and the parity check (judgment) at RAM read are not executed.

Note2: Since the initial data of RAM is undefined, RAM initialization (data writing) is required with <RPAREN>=1(enabled) and <RPARF>=0(interrupt disabled) setting before RAM reading.

4.2.2. *[RPARxST]* (RAM Parity Status Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7	RPARFG7	0	R	RAM parity error status flag 7 (RAM area 7) 1: Error occurs 0: No errors
6	RPARFG6	0	R	RAM parity error status flag 6 (RAM area 6) 1: Error occurs 0: No errors
5	RPARFG5	0	R	RAM parity error status flag 5 (RAM area 5) 1: Error occurs 0: No errors
4	RPARFG4	0	R	RAM parity error status flag 4 (RAM area 4) 1: Error occurs 0: No errors
3	RPARFG3	0	R	RAM parity error status flag 3 (RAM area 3) 1: Error occurs 0: No errors
2	RPARFG2	0	R	RAM parity error status flag 2 (RAM area 2) 1: Error occurs 0: No errors
1	RPARFG1	0	R	RAM parity error status flag 1 (RAM area 1) 1: Error occurs 0: No errors
0	RPARFG0	0	R	RAM parity error status flag 0 (RAM area 0) 1: Error occurs 0: No errors

Note1: If a parity error occurs, the flag <RPARFGn> of the RAM area containing the address of the data that caused the error is set to "1". Check the RAM parity error address register n (***[RPARxEADn]***) corresponding to <RPARFGn> that has become "1" for the actual error address.
Example: When n=0 "RAM parity error address register 0 (***[RPARxEAD0]***)".

Note2: The status flag can be cleared by setting the corresponding bit in ***[RPARxCLR]*** register to "1".

Note3: When a status flag <RPARFGn>=1 (error occurs) and a parity error occur in another address within the same area n, the parity error address storage register (***[RPARxEADn]***) is not updated.

4.2.3. *[RPARxCLR]* (RAM Parity Status Clear Register)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as "0"
7	RPARCLR7	0	W	Clearing RAM parity error status flag 7 (RAM area 7) 0: - 1: Status is cleared. (Note1)
6	RPARCLR6	0	W	Clearing RAM parity error status flag 6 (RAM area 6) 0: - 1: Status is cleared. (Note1)
5	RPARCLR5	0	W	Clearing RAM parity error status flag 5 (RAM area 5) 0: - 1: Status is cleared. (Note1)
4	RPARCLR4	0	W	Clearing RAM parity error status flag 4 (RAM area 4) 0: - 1: Status is cleared. (Note1)
3	RPARCLR3	0	W	Clearing RAM parity error status flag 3 (RAM area 3) 0: - 1: Status is cleared. (Note1)
2	RPARCLR2	0	W	Clearing RAM parity error status flag 2 (RAM area 2) 0: - 1: Status is cleared. (Note1)
1	RPARCLR1	0	W	Clearing RAM parity error status flag 1 (RAM area 1) 0: - 1: Status is cleared. (Note1)
0	RPARCLR0	0	W	Clearing RAM parity error status flag 0 (RAM area 0) 0: - 1: Status is cleared. (Not 1)

Note1: The error status in RAM area is cleared by setting the corresponding bit to "1".

Note2: When the flag clearing and error occurrence at the same timing, the error detection is prior.

Note3: Check the error address before clearing the flag.

4.2.4. *[RPARxEAD0]* (RAM Parity Error Address Register 0)

The address which the error generated in the RAM area 0 is stored in ***[RPARxEAD0]***.
[RPARxEAD1] to ***[RPARxEAD7]*** is the same composition and operation.

Bit	Bit symbol	After reset	Type	Function
31:0	RPAREADD0	0x00000000	R	RAM parity error generated address 0x00000000: No errors. 0x200XXXXX: Address which is error occurs.

Note: While the error status flag ***[RPARxST]***<RPARFG0> is "1", the error address ***[RPARxEAD0]*** <RPAREADD0> is not updated even if an error occurs in another address in the same area 0.

5. Example for Use

5.1. Example 1

When the address "0x20000102" is read by 32-bit access, the contents of "0x20000102" to "0x20000105" are read. When a parity error occurs at address "0x20000104", the address "0x20000104" is stored in the RAM parity error address register ***[RPARxEADn]***.

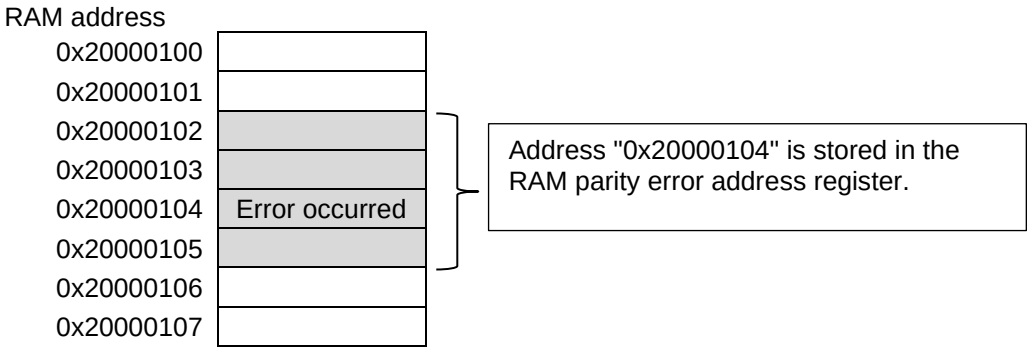

Figure 5.1 Example1 of RAM Address

5.2. Example 2

When the address "0x20000102" is read by 32-bit access, the contents of "0x20000102" to "0x20000105" are read. When a parity error occurs at addresses "0x20000103" and "0x20000104", the address "0x20000103" is stored in the RAM parity error address register ***[RPARxEADn]***.

If a parity error occurs at more than one address during 32-bit access, the smallest address is stored. Parity error cannot be detected at the second and subsequent addresses.

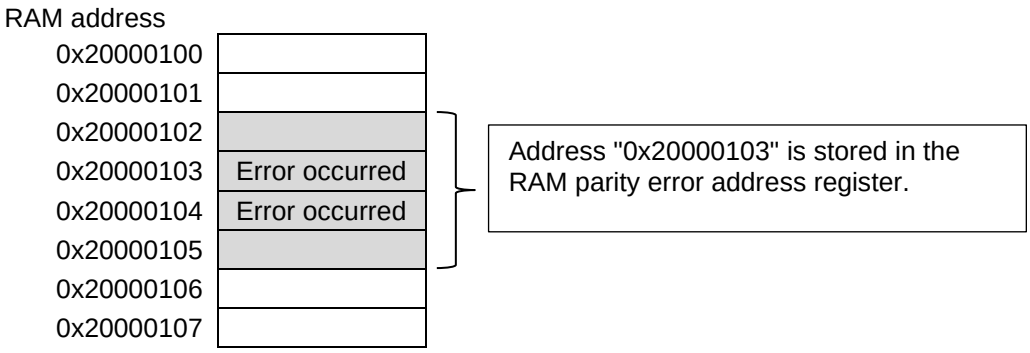

Figure 5.2 Example2 of RAM Address

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2018-06-14	- First release
1.1	2024-05-10	- Appearance updated

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