32-bit RISC Microcontroller
Reference Manual

Oscillation Frequency Detector (OFD-A)

Revision 1.2

2024-05

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Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 - Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 - It is possible to omit the "0b" when the number of bits can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m:n].
  Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "N" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1]***, ***[XYZ2]***, ***[XYZ3]*** → ***[XYZn]***
- "x" substitutes suffix number or character of units and channels in the register list.
- In case of unit, "x" means A, B, and C, ...
  Example: ***[ADACR0]***, ***[ADBCR0]***, ***[ADCCR0]*** → ***[ADxCR0]***
- In case of channel, "x" means 0, 1, and 2, ...
  Example: ***[T32A0RUNA]***, ***[T32A1RUNA]***, ***[T32A2RUNA]*** → ***[T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and write are possible.
- Unless otherwise specified, register access supports only word access.
- The register defined as "Reserved" must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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Terms and Abbreviations

Some of abbreviations used in this document are as follows:

OFD	Oscillation Frequency Detector
EHOSC	External High-speed Oscillator
IHOSC2	Internal High-speed Oscillator 2

1. Outlines

Oscillation frequency detector (OFD) detects abnormalities as the clock signal to monitor exceeding the range of the set-up frequency. The lists of functions are as follows.

Function classification	Function	Operation
Abnormal detection of the clock frequency	Monitor clock	External high-speed oscillator clock (f_{EHOSC}) or High-speed clock (fc)
	Standard clock (Note)	Internal high-speed oscillator 2 clock (f_{IHOSC2})
	Frequency detective range	The maximum, the minimum are settable.
	State monitor	Status register. - operation / no operation - abnormality / no abnormality
	Reset output	Prohibition/permission of a reset output are possible.
Protection	Protection function	Incorrect writing is prevented.

Note: When stopping the standard clock during OFD operation (***[OFDRST]***<OFDRSTEN> = 1), OFD reset occurs. (When stopping the standard clock before OFD operation, OFD reset does not occur.)

2. Configuration

The block diagram of the frequency detection circuit is shown as follows:

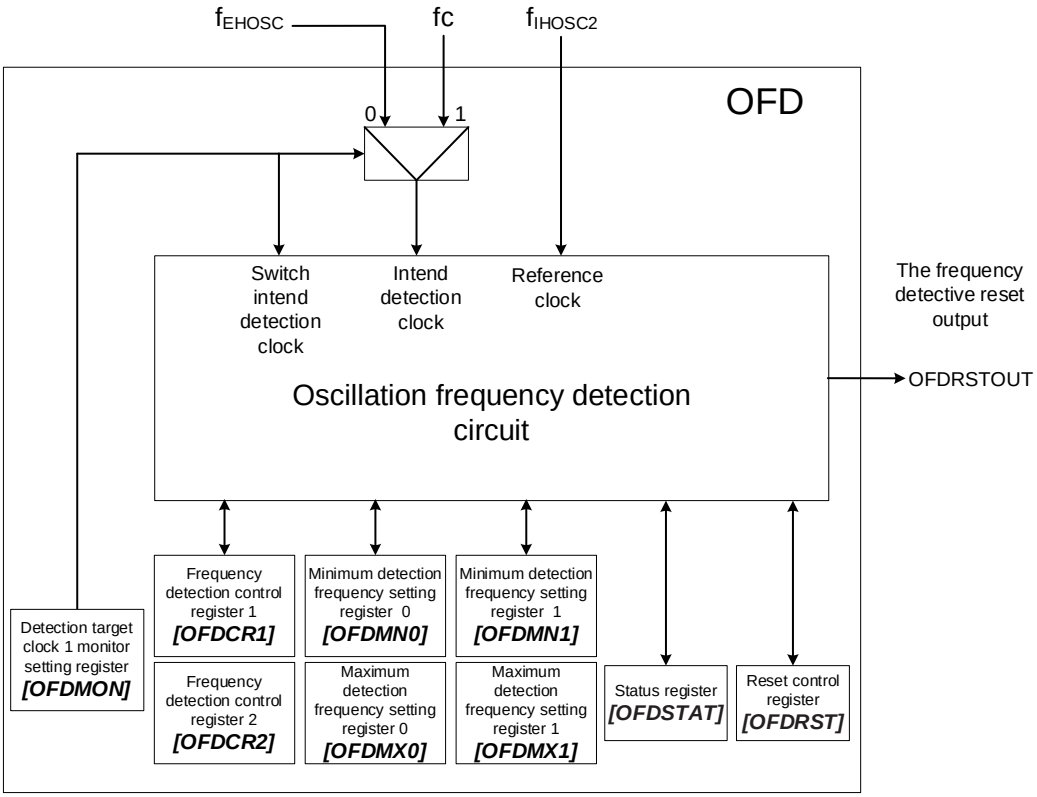

Figure 2.1 Oscillation Frequency Detector Block Diagram

Table 2.1 List of Signals

No.	symbol	Signal name	I/O	Related reference manual
1	f_{IHOSC2}	Internal high-speed oscillator 2 clock	Input	Clock Control and Operation Mode
2	f_{EHOSC}	External high-speed oscillator clock	Input	Clock Control and Operation Mode
3	fc	Internal high-speed oscillator (The clock that the clock was chosen in ***[CGOSCCR]***<OSCSEL>and ***[CGPLL0SEL]*** <PLL0SEL>.)	Input	Clock Control and Operation Mode
4	OFDRSTOUT	OFD reset	Output	Power Supply and Reset Operation Clock Control and Operation Mode

3. Function and Operation

Oscillation Frequency Detector (OFD) is a function to detect the abnormality of the clock.

3.1. Setting Method

When you use OFD, please set an applicable clock enable bit to “1” (clock supply) in fsys supply stop register A (***[CGFSYSENA]***, ***[CGFSYSMENA]***), fsys supply stop register B (***[CGFSYSENB]***,***[CGFSYSMENB]***), and fc supply stop registers (***[CGFCEN]***). In addition, please set a standard clock (internal high-speed oscillator (IHOSC2) for OFD) for an oscillation.

The corresponding registers and the bit locations depend on a product. Some products do not have all registers. For the details, refer to “Clock Control and Operation Mode” in Reference manual.

After the reset is deasserted, the registers other than ***[OFDCR1]*** cannot be written. The write is enabled by setting 0xF9 to ***[OFDCR1]***.

- When the measuring object is f_{EHOSC}.

  [OFDMON] is set as “0” and the measuring object is used as the external high-speed oscillator clock (f_{EHOSC}). A lower limit level in the range of the frequency to detect is set by ***[OFDMN0]*** <OFDMN0>. An upper limit level in the range of the frequency to detect is set by ***[OFDMX0]*** <OFDMX0>.

- When the measuring object is fc.

  [OFDMON] is set as “1” and the measuring object is used as the high-speed clock (fc). A lower limit level in the range of the frequency to detect is set by ***[OFDMN1]*** <OFDMN1>. An upper limit level in the range of the frequency to detect is set by ***[OFDMX1]*** <OFDMX1>.

Permission/prohibition of reset generating is set up by ***[OFDRST]***. The operation will be started if “0xE4” is written in ***[OFDCR2]***.

In order to prevent erroneous write, please set “0x06” as ***[OFDCR1]*** after the setup of all the registers, and forbid the writing. Moreover, after the operation has stopped, please make the change of the setup.

3.2. Detection Frequency

There are detected frequency ranges and undetected frequency ranges in the frequency detection function depending on the oscillation accuracy of the reference clock. The frequency detection is not ensured in the range between the detected frequency and undetected frequency.

The maximum and the minimum detection frequencies are calculated with the target clock frequency, the reference clock frequency, and their frequency deviations.

The maximum values and the minimum values of the detected range and the undetected range depend on the round-up and round-down of the frequency values as follows. The round-up or round-down of <OFDMX0/1> and <OFDMN0/1> should be selected according to the deviation of the target clock frequency.

- <OFDMX1> is rounded up and <OFDMN1> is rounded down: At the time of fc selection

  To the detection object clock, the maximum of the non-detecting range becomes high and the minimum of the non-detecting range becomes low.

- <OFDMX1> is rounded down and <OFDMN1> is rounded up: At the time of fc selection

  To the detection object clock, the maximum of the non-detecting range becomes low and the minimum of the non-detecting range becomes high.

(In the case of fc selection)

The detection frequency range is shown in the Figure 3.1 detection frequency range.

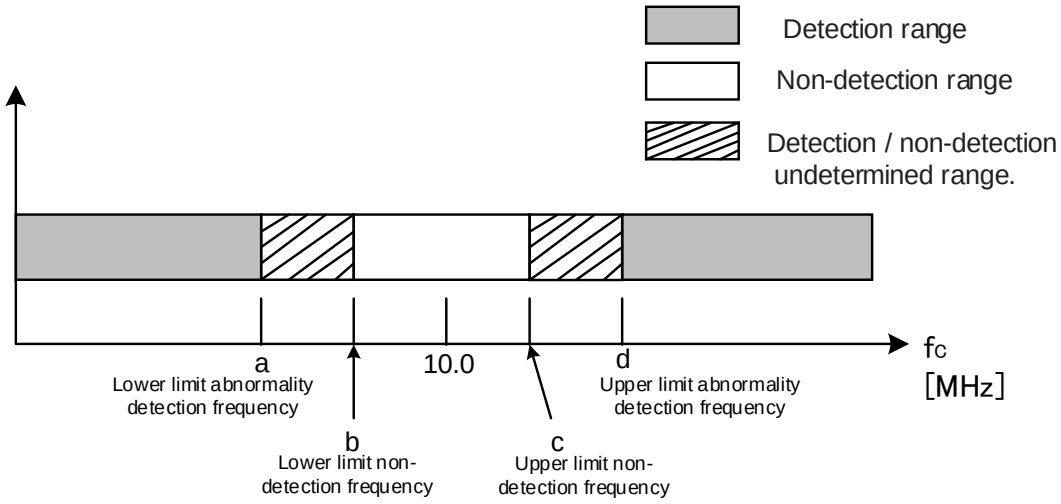

Figure 3.1 Example of Detection Frequency Range (In Case of 10MHz)

When the deviation of the reference clock frequency is ±10 % and the deviation of the target clock frequency is ±1 % (Undetected area), the setting values of ***[OFDMN1]***<OFDMN1> and ***[OFDMX1]***<OFDMX1> are calculated as follows. In this example, <OFDMX1> is rounded up and <OFDMN1> is rounded down.

Table 3.1 Clock Examples

Detection target clock	10MHz ± 1 %	Max 10.1 MHz	----------	e
		Min 9.9 MHz	----------	f
Reference clock	10MHz ± 10 %	Max 11.0 MHz	----------	g
		Min 9.0 MHz	----------	h

・Calculating formula

Register set point = (Detective target clock frequency / 4) / (Standard clock frequency / 256)
= (Detective target clock frequency / Standard clock frequency) × 64

Note: The above is the example from which dividing of the reference clock is 256 dividing. The numerical value of dividing changes with products. For detail, refer to the "Product Information" of Reference manual.

The preset value is calculated as follows by the formula.

<OFDMX1> value = e / h × 64 = 71.82 = 72 (Decimal fraction is rounded up) = 0x48
<OFDMN1> value = f / g × 64 = 57.6 = 57 (Decimal fraction is rounded down) = 0x39

Then the range of the detected area is defined as follows:
a = h × <OFDMN1> / 64 = 8.01 (round-down)
d = g × <OFDMX1> / 64 = 12.38 (round-up)

The range of the undetected area is defined as follows:
b = g × <OFDMN1> / 64 = 9.80 (round-up)
C = h × <OFDMX1> / 64 = 10.12 (round-down)

That is, <OFDMX1> and <OFDMN1> are set to 0x48 and 0x39, respectively. Then, the frequency detection reset is generated when the frequency of 12.38 MHz or more, and 8.01 MHz or less is detected.
And if the frequency of 9.80 MHz to 10.12 MHz is detected, the frequency detection reset is not generated.

3.3. Detection Start Timing

The time for two periods of detective periods is necessary from operation start to a detective start. During detective operation, it is ***[OFDSTAT]*** I can confirm it in <OFDBUSY>.

3.4. Detection

The time for the two cycles of the detection cycle is required after OFD detects the abnormalities until it generates reset. If a reset occurs, OFD will be initialized and will stop.

Note: There are multiple causes of the reset. The reset factor can be checked with the exception/interrupt register ***[RLMRSTFLG1]***. For the ***[RLMRSTFLG1]*** register, refer to an exception chapter in the reference manual system.

3.5. Available Operation Mode of MCU

The frequency detection circuit is available only in the NORMAL mode and the IDLE mode. When the transition to the other mode is done, the frequency detection circuit should be stopped.

3.6. External High-speed Oscillation Clock Detection

In changing a system clock into an external high-speed oscillation clock (EHOSC), please check an oscillation state by a monitoring function, and set ***[OFDMON]*** <OFDMON> as "0". At this time, disable reset generation and monitor the oscillation condition by ***[OFDSTAT]***<FRQERR>. Since the ***[OFDSTAT]***<OFDBUSY> changes to operating until the state of ***[OFDSTAT]***<FRQERR> changes valid, time length as two cycles of detecting clock is needed.

4. Registers

4.1. List of Registers

The control registers and their addresses are shown in the following table.

Peripheral function	Function name	Channel/unit	Base address		
			TYPE 1	TYPE 2	TYPE 3
Oscillation frequency detector	OFD	-	0x400F1000	0x400E4000	0x40084000

Note: The channel/unit and base address type are different by products. Please refer to "Products Information" of the reference manual for the details.

Register name		Base address (Base+)
Frequency Detection Control Register 1	***[OFDCR1]***	0x0000
Frequency Detection Control Register 2	***[OFDCR2]***	0x0004
Minimum Detection Frequency Setting Register 0	***[OFDMN0]***	0x0008
Minimum Detection Frequency Setting Register 1	***[OFDMN1]***	0x000C
Maximum Detection Frequency Setting Register 0	***[OFDMX0]***	0x0010
Maximum Detection Frequency Setting Register 1	***[OFDMX1]***	0x0014
Reset Control Register	***[OFDRST]***	0x0018
Status Register	***[OFDSTAT]***	0x001C
Detection Target Clock 1 Monitor Setting Register	***[OFDMON]***	0x0020

4.2. *[OFDCR1]* (Frequency Detection Control Register 1)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as 0.
7:0	OFDWEN[7:0]	0x06	R/W	Register write control 0x06: Disabled. 0xF9: Enabled. When “0xF9” is set, the registers other than ***[OFDCR1]*** can be written. If a value other than “0x06” and “0xF9” is written, “0x06” is written. Each register can be read even though the register write is disabled.

4.3. *[OFDMON]* (Detection Target Clock 1 Monitor Setting Register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as 0.
0	OFDMON	1	R/W	Detection target clock selection 0: f_{EHOSC} 1: fc

Note: This register cannot be written when the frequency detection is enabled.

4.4. *[OFDMN0]* (Minimum Detection Frequency Setting Register 0)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as 0.
11:0	OFDMN0[11:0]	0x000	R/W	The lower limit value of the detection frequency is set. (f_{EHOSC})

Note: This register cannot be written when the frequency detection is enabled.

4.5. *[OFDMN1]* (Minimum Detection Frequency Setting Register 1)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as 0.
11:0	OFDMN1[11:0]	0x000	R/W	The lower limit value of the detection frequency is set. (fc)

Note: This register cannot be written when the frequency detection is enabled.

4.6. *[OFDMX0]* (Maximum Detection Frequency Setting Register 0)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as 0.
11:0	OFDMX0[11:0]	0x000	R/W	The upper limit value of the detection frequency is set. (f_{EHOSC})

Note: This register cannot be written when the frequency detection is enabled.

4.7. *[OFDMX1]* (Maximum Detection Frequency Setting Register 1)

Bit	Bit symbol	After reset	Type	Function
31:12	-	0	R	Read as 0.
11:0	OFDMX1[11:0]	0x000	R/W	The upper limit value of the detection frequency is set. (fc)

Note: This register cannot be written when the frequency detection is enabled.

4.8. *[OFDRST]* (Reset Control Register)

Bit	Bit symbol	After reset	Type	Function
31:1	-	0	R	Read as 0.
0	OFDRSTEN	1	R/W	Reset generation control (OFDRSTOUT) 0: Disabled. 1: Enabled.

Note: This register cannot be written when the frequency detection is enabled.

4.9. *[OFDCR2]* (Frequency Detection Control Register 2)

Bit	Bit symbol	After reset	Type	Function
31:8	-	0	R	Read as 0.
7:0	OFDEN[7:0]	0x00	R/W	Frequency detection control 0x00: Disabled. 0xE4: Enabled. Writing a value except “0x00” or “0xE4” is invalid and a value will not be changed.

4.10. *[OFDSTAT]* (Status Register)

Bit	Bit symbol	After reset	Type	Function
31:2	-	0	R	Read as 0.
1	OFDBUSY	0	R	OFD operation status 0: Stop. 1: Operating.
0	FRQERR	0	R	Error detecting flag 0: No Error 1: Error

5. Usage Example

The operation procedure of the frequency detection circuit is as follows:

When a reset is asserted, the cause of the reset should be checked in the ***[RLMRSTFLG1]*** register. If the cause is not the frequency detection reset, the external oscillation should be enabled, the register settings should be done to use the frequency detection circuit, and its operation should be enabled. And the reset output of OFD should be disabled.

After the detection starts, the abnormality detection flag in the ***[OFDSTAT]*** register should be checked. If any abnormalities are not present, the clock should be changed to the external oscillation clock.

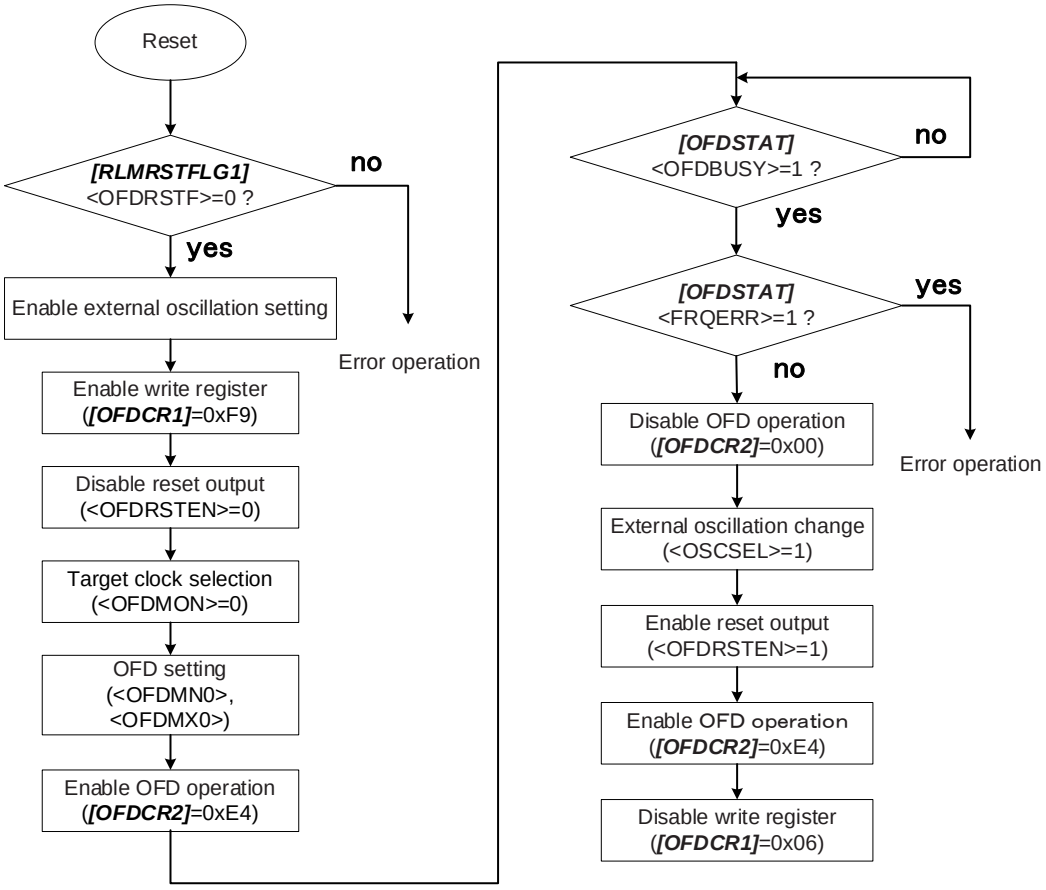

Figure 5.1 Example of Operational Procedure

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2017-09-08	- First release
1.1	2018-03-09	- 1. Outlines Added (Note) in Standard clock - 3.2 Detection Frequency Added note on Table 3.1 Corrected: “<OFDM1>”->” <OFDMN1>” - 4.1. List of Registers Added: Base address (TYPE 3)
1.2	2024-05-10	- Appearance updated

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