Bi-CMOS Linear Integrated Circuit Silicon Monolithic

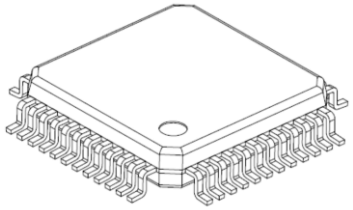
TB9M003FG

IC for automotive three-phase brushless DC motor

1. Description

The TB9M003FG is a gate driver IC with a microcontroller unit (MCU) for automotive brushless DC (BLDC) motor applications, which incorporates Toshiba's unique Vector Engine (VE) to simplify motor vector control and offload the CPU.

The TB9M003FG is designed to be used with external N-channel FET pairs, making it suitable for BLDC motors with a wide range of output. The TB9M003FG also incorporates a CPU and a flash ROM, making it possible to program a control method and parameters according to the motor and application requirements. The TB9M003FG can be configured to transition to Standby mode in the idle state in order to reduce power consumption.



HTQFP48-0707-0.50

weight: 0.14 g (typ.)

2. Applications

For automotive (electric pumps and fans), three-phase brushless motor control and drive.

3. Features

- Integrated MCU and gate drivers enable downsizing of the system
- Built-in vector engine for our original sensorless control

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Start of commercial production
2024-01

4. Functions

- 32 bit Arm® Cortex®-M0 core
  - Serial Wire Debug Support
  - 32ch Interrupt Controller1 cycle multiplier
  - Up to 40 MHz clock frequency
- Single Bus Master System
- 12 KBytes ROM(BootLoader, Flash API) (incECC SEC/DED)
- 64 KBytes Code Flash(incl. ECC SEC/DED)
- 4 KBytes SRAM (incl. ECC SEC/DED)
- 32-bit Compare Timers (DTIMER)
- 28-bit Capture Timer (8 inputs, 6 measurement)
- Watchdog Timer(WATCHDOG)
- Power saving modes (CPU Sleep, Standby)
- 4ch Pulse Width Modulator Generator(PWMGEN)
- 12 General-purpose I/O Ports (GPIO)
- 10-bit A/D Converter (GADC) with 2 analog inputs + internal temperature, VMON
- 12-bit A/D Converter (MADC)
- Vector Engine(VE)
- Programmable Motor Driver(PMD)
- Encoder(ENC)
- LDOs (LDO5V, LDO15V)
- Power On Reset (POR5V, PORL)
- 2 on-chip OSCs (IOSCH, IOSCL)
- External X'tal OSC
- PLL
- LIN　ISO17987/SAEJ2602　transceiver + controller
- 2 full duplex serial interfaces (UART1, UART2), UART1 with LIN support
- SPI-I/F
- MOSFET driver including charge pump
- High-speed operational amplifier for motor current sensing via shunt
- Over current protection (LDO, MOSFET driver)
- Over temperature protection
- Package HTQFP48-0707-0.50
- Single power supply from 6.0V to 18V
- Temperature Range Tj = -40°C to +175°C
- Green package (RoHS compliant)
- AEC-Q100 grade 0 qualified

5. Block Diagram

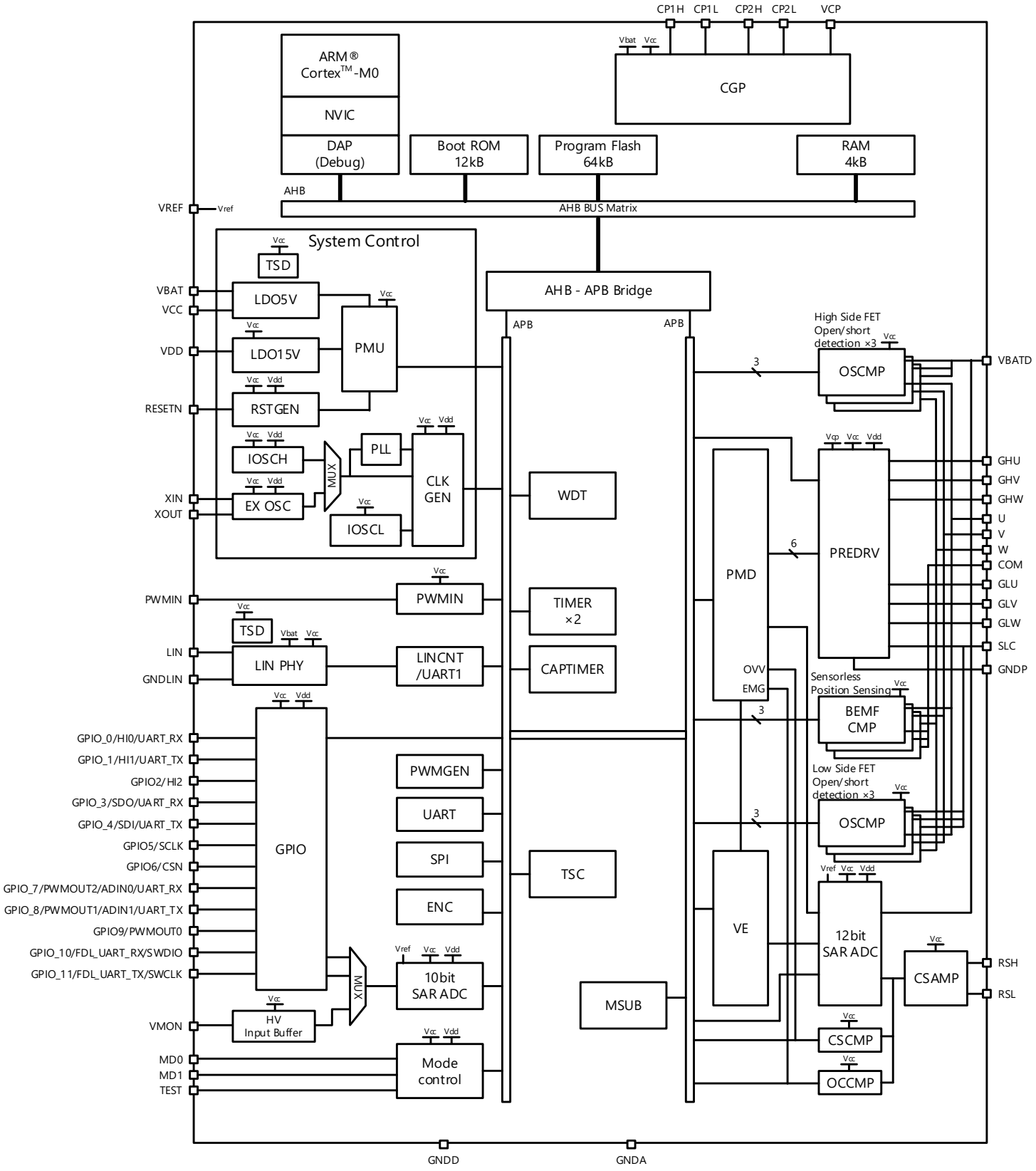


Figure 5.1 Block Diagram

6. Pin Assignments

(Top view)

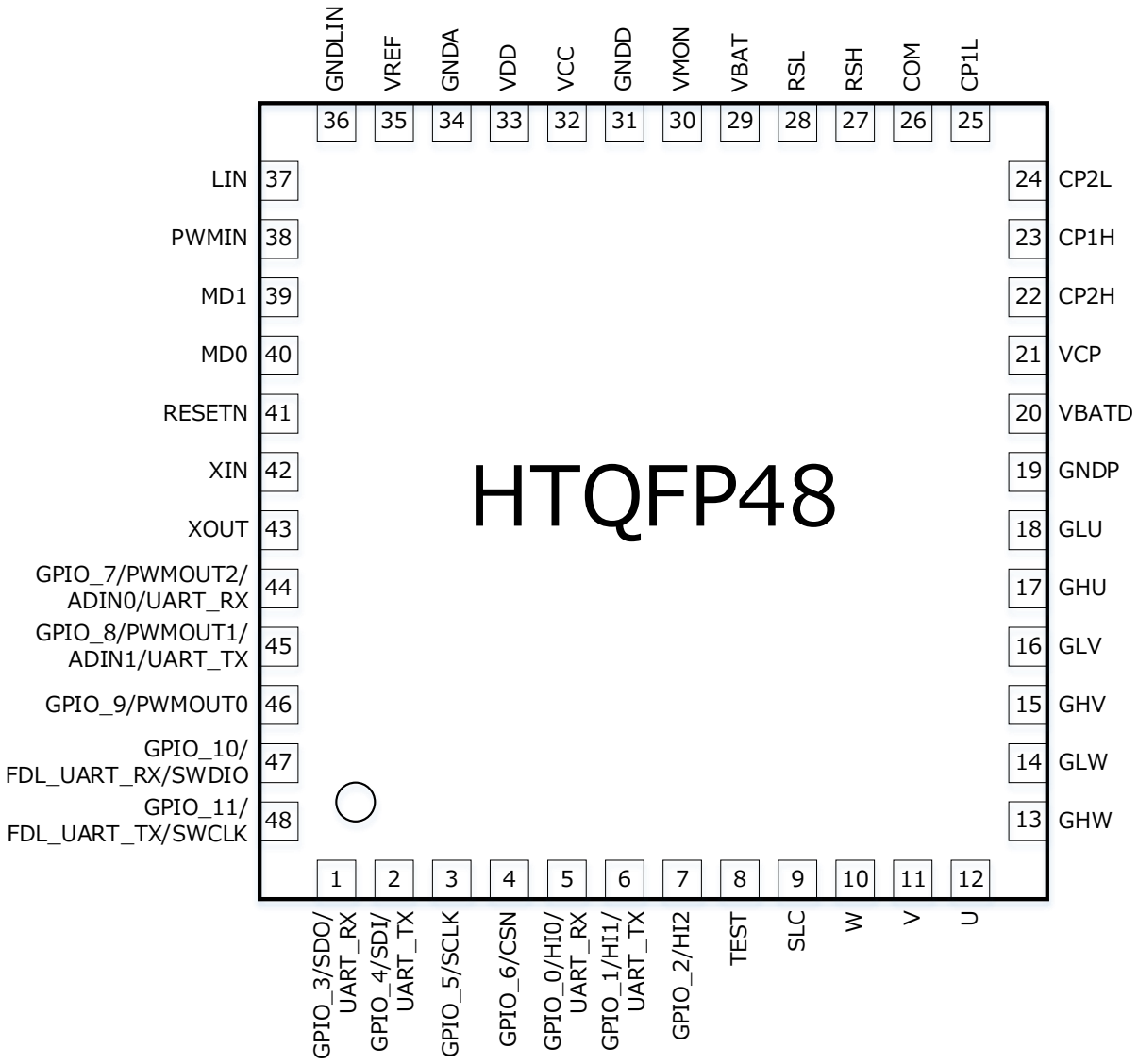


Figure 6.1 Pin Assignment Diagram

7. Pin Description

Table 7.1 Pin Description

Pin	Symbol	I/O	Description
1	GPIO_3/SDO/UART_RX	I/O	General-purpose I/O port / SPI data output/UART_RX
2	GPIO_4/SDI/UART_TX	I/O	General-purpose I/O port / SPI data input/UART_TX
3	GPIO_5/SCLK	I/O	General-purpose I/O port / SPI data clock
4	GPIO_6/CSN	I/O	General-purpose I/O port / SPI chip select
5	GPIO_0/HI0/UART_RX	I/O	General-purpose I/O port/ Hall sensor input/UART_RX
6	GPIO_1/HI1/UART_TX	I/O	General-purpose I/O port/ Hall sensor input/UART_TX
7	GPIO_2/HI2	I/O	General-purpose I/O port/ Hall sensor input
8	TEST	I	Test mode select
9	SLC	I	Low-side FET source input
10	W	I	Phase-W motor connection pin
11	V	I	Phase-V motor connection pin
12	U	I	Phase-U motor connection pin
13	GHW	O	Phase-W high-side FET gate output
14	GLW	O	Phase-W low-side FET gate output
15	GHV	O	Phase-V high-side FET gate output
16	GLV	O	Phase-V low-side FET gate output
17	GHU	O	Phase-U high-side FET gate output
18	GLU	O	Phase-U low-side FET gate output
19	GNDP	-	Power ground
20	VBATD	I	Battery voltage regulator input for driver circuit
21	VCP	O	Voltage regulator output for charge pump
22	CP2H	O	Boost capacitor connection pin for charge pump
23	CP1H	O	Boost capacitor connection pin for charge pump
24	CP2L	O	Boost capacitor connection pin for charge pump
25	CP1L	O	Boost capacitor connection pin for charge pump
26	COM	I	Motor pseudo-neutral point input
27	RSH	I	VCC side of current-sense resistor
28	RSL	I	Ground side of current-sense resistor
29	VBAT	I	Battery voltage regulator input
30	VMON	I	Battery voltage regulator input (for ADC input)
31	GNDD	-	Logic ground
32	VCC	O	5-volt regulator output
33	VDD	O	1.5-volt regulator output
34	GNDA	-	Analog ground
35	VREF	I	ADC reference voltage input
36	GNDLIN	-	Ground for LIN Phy
37	LIN	I/O	LIN bus line
38	PWMIN	I	PWM speed input
39	MD1	I	Mode select

40	MD0	I	Mode select
41	RESETN	I/O	Reset I/O
42	XIN	I	Crystal or ceramic oscillator connection pin
43	XOUT	O	Crystal or ceramic oscillator connection pin
44	GPIO_7/PWMOUT2/ADIN0/UART_RX	I/O	General-purpose I/O port / ADC input/UART_RX
45	GPIO_8/PWMOUT1/ADIN1/UART_TX	I/O	General-purpose I/O port / ADC input/UART_TX
46	GPIO_9/PWMOUT0	I/O	General-purpose I/O port / PWM output
47	GPIO_10/FDL_UART_RX/SWDIO	I/O	General-purpose I/O port / UART RX for FDL_UART/ SWDIO for Debug
48	GPIO_11/FDL_UART_TX/SWCLK	I/O	General-purpose I/O port / UART TX for FDL_UART/ SWCLK for Debug

8. I/O Equivalent Circuits

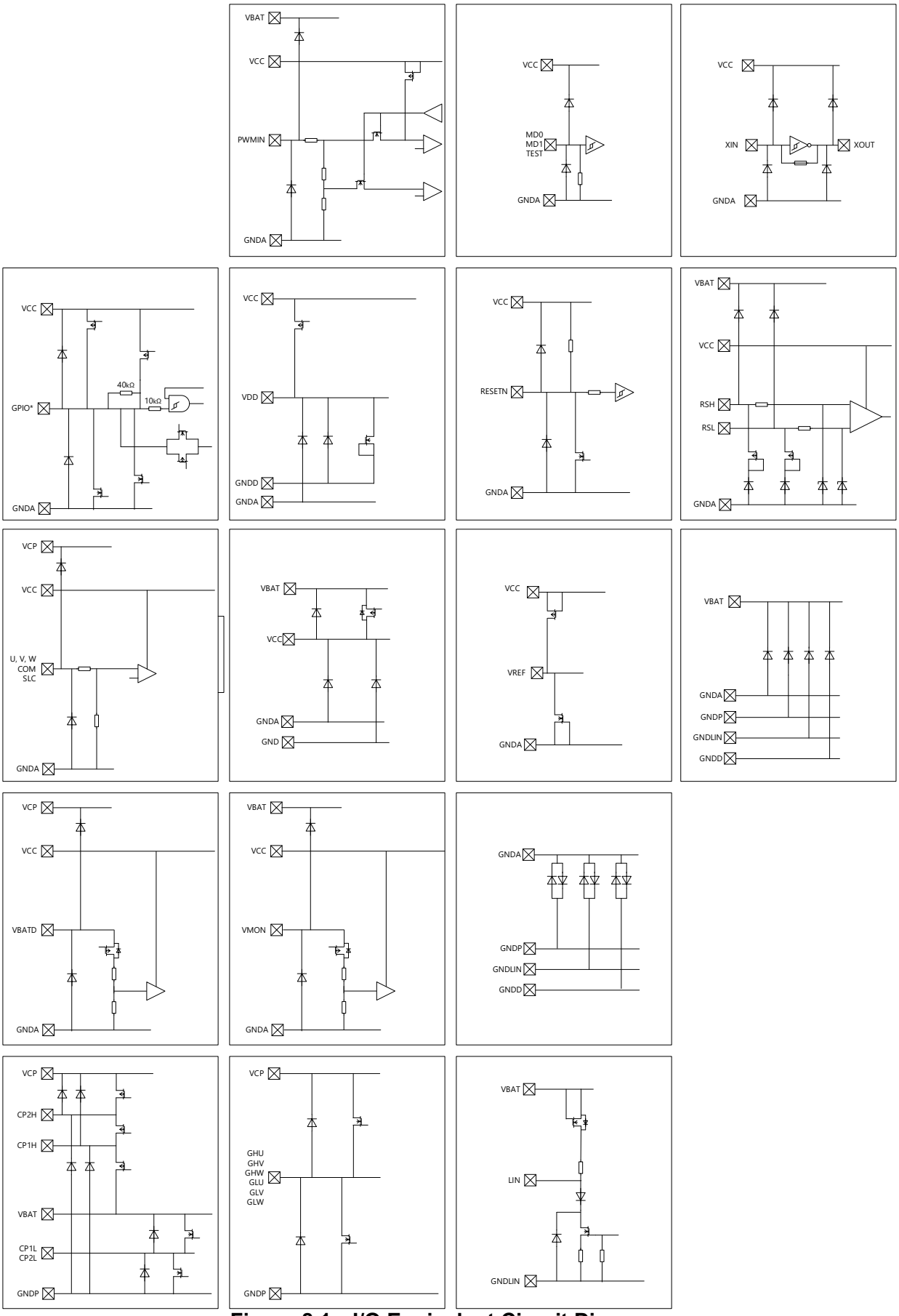


Figure 8.1 I/O Equivalent Circuit Diagrams

9. Functional Description

9.1. Predriver Circuit

- Six-channel predriver circuit for driving a three-phase inverter (consisting of high-side and low-side N-channel MOSFETs) for a BLDC motor
- Turns on and off the predrivers according to the drive signals from digital logic

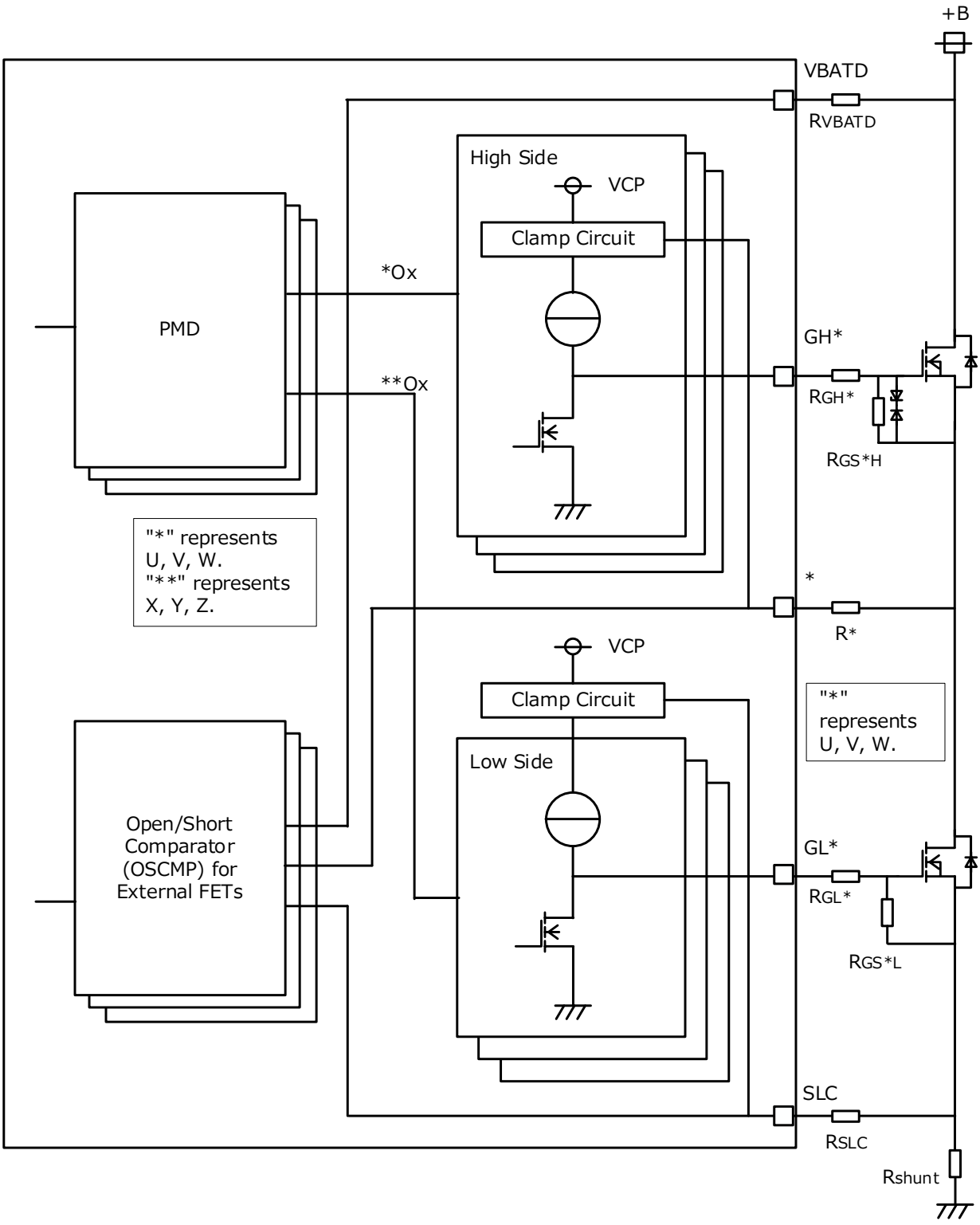


Figure 9.1.1 Predriver Circuit Diagram

9.2. Charge Pump Circuit

The CGP generates a voltage for the PREDRV to drive external high-side N-channel FETs.

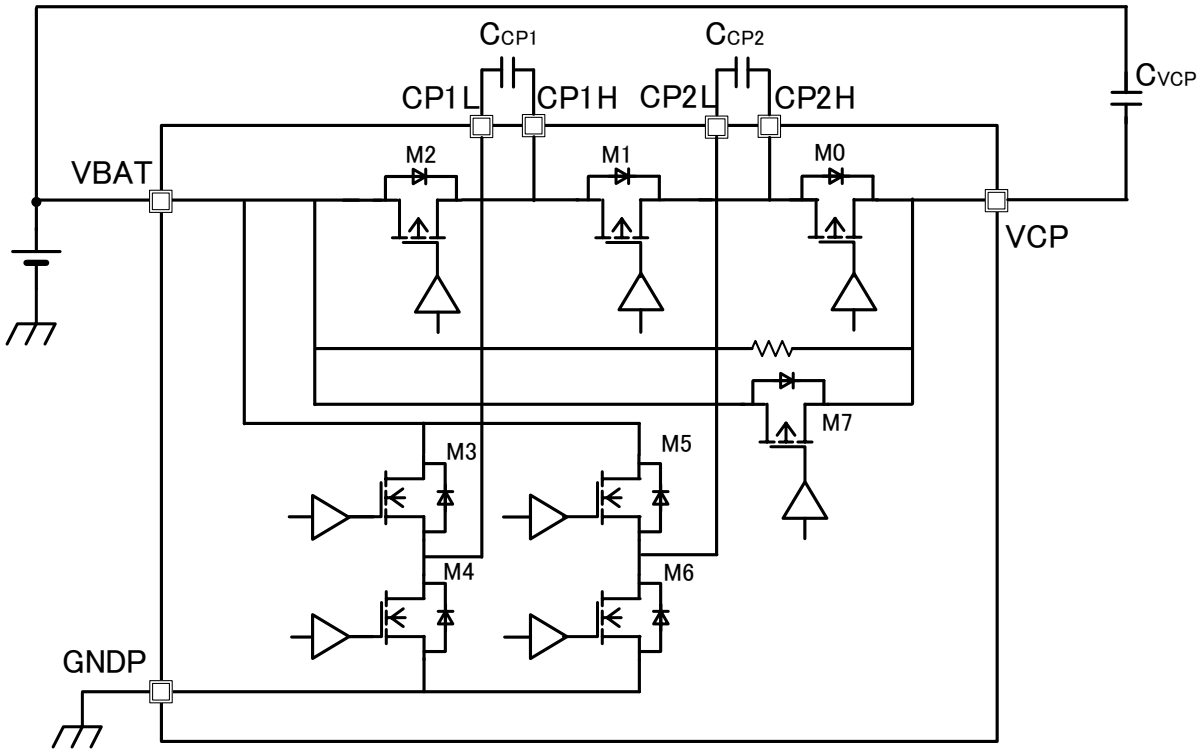


Figure 9.2.1 Charge Pump Circuit Diagram

9.3. Current-Sense Amplifier (CSAMP)

- The Current-Sense Amplifier (CSAMP) amplifies the voltage across an external shunt resistor by the gain programmed via a 3-bit register field.
- The amplified voltage is applied to the MADC, Overcurrent Detection Comparator (OCCMP), and Current Clamp Comparator (CLCMP).
- The output offset voltage can be adjusted prior.

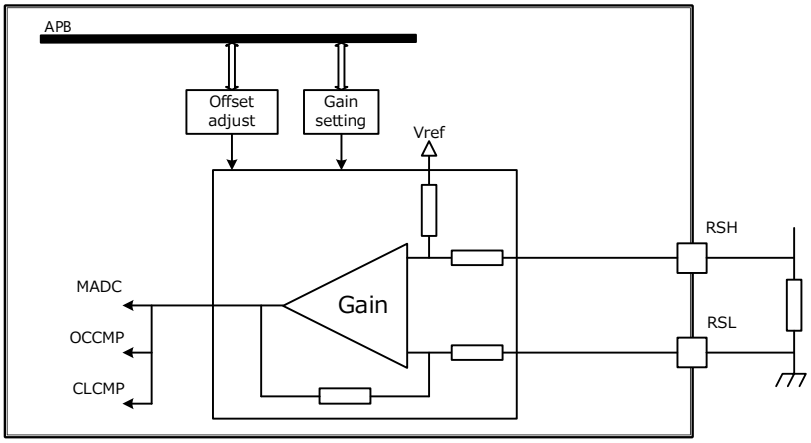


Figure 9.3.1 Current-Sense Amplifier Circuit Diagram

9.4. Current Clamp Comparator (CLCMP)

- The CLCMP limits current if the output from the Current-Sense Amplifier (CSAMP) exceeds the programmed voltage threshold.
- The output voltage of the CSAMP is applied to the CLCMP.
- This threshold is programmable in 32 steps (i.e., with a 5-bit value)
- The CLCMP incorporates a digital filter to prevent malfunction caused by noise.

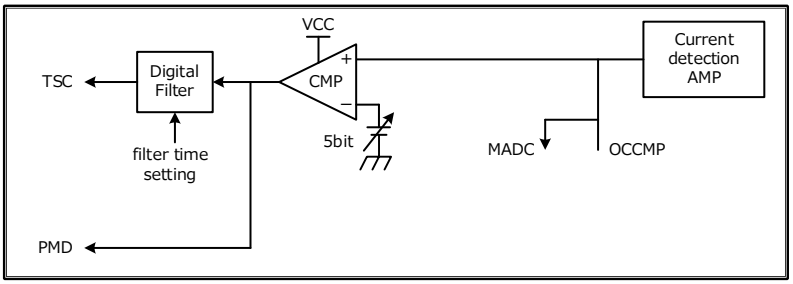


Figure 9.4.1 Current Clamp Comparator Circuit Diagram

9.5. Overcurrent Detection Comparator (OCCMP)

- The OCCMP reports an error when the output from the Current-Sense Amplifier (CSAMP) exceeds the programmed threshold.
- The OCCMP can be enabled and disabled via the ANASTBY register.
- The overcurrent threshold is programmable with a four-bit value via a special function register.
- The OCCMP incorporates a digital filter to prevent malfunction caused by noise.

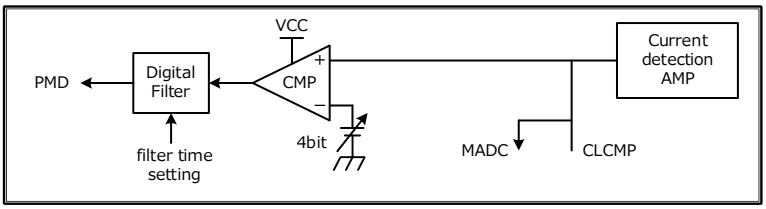


Figure 9.5.1 Overcurrent Detection Comparator Circuit Diagram

9.6. Open/Short Comparator (OSCMP) for External FETs

The Open/Short Comparator detects open- and short-circuits involving external FETs.

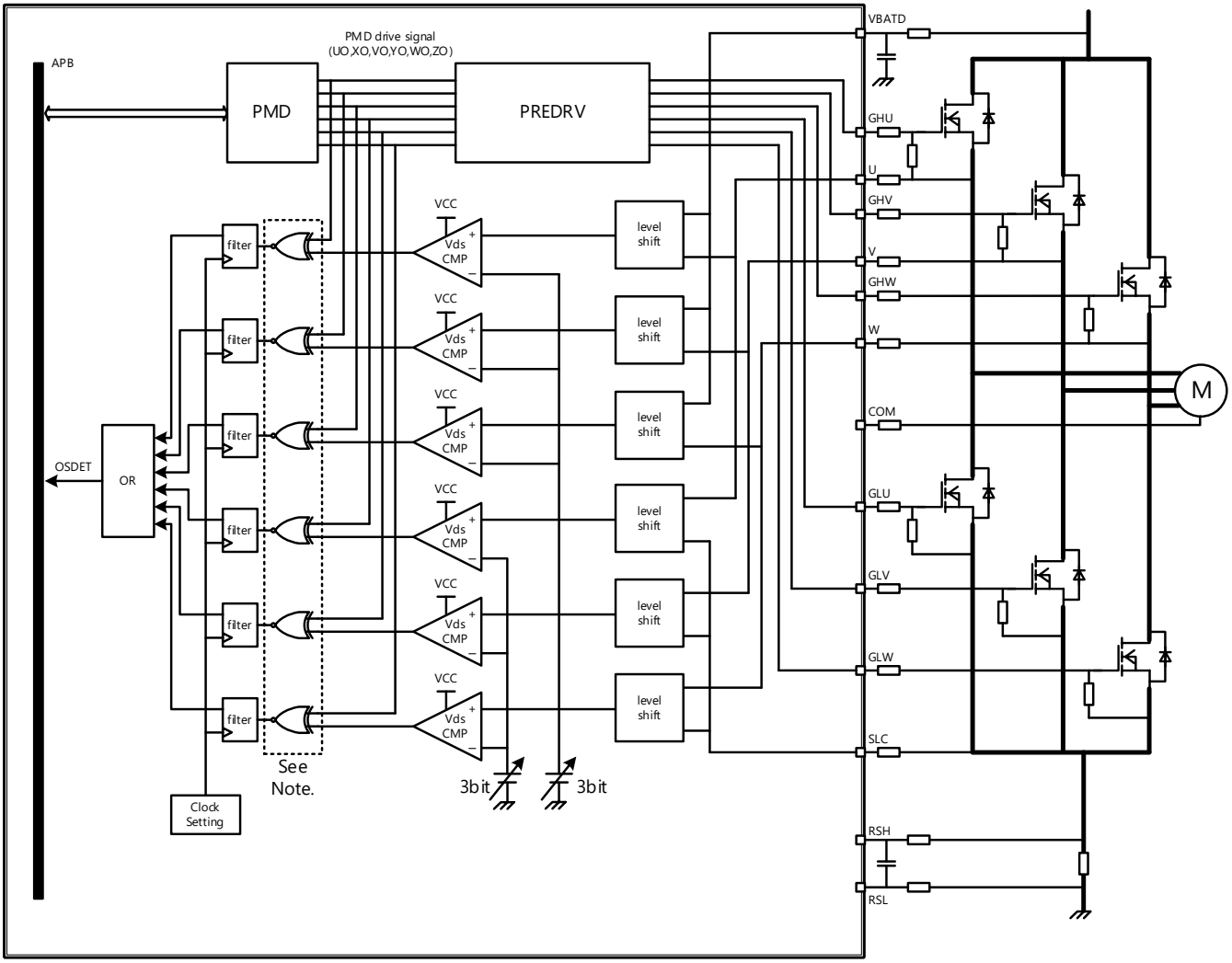


Figure 9.6.1 OSCMP Block Diagram

9.7. Vector Engine(VE)

Table 9.7.1 VE Function List

Category	Function	Description
Calculation	Basic functions	Fixed-point calculation Vector control tasks Tasks for interfacing with the PMD and MADC
	Current control tasks	PI control of d-axis and q-axis currents ・Non-interference control ・Output limiting based on scalar voltage values
	SIN/COS Calculation 1 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	SIN/COS Calculation 2 task	Calculates the sine and cosine values of phase θ
	SIN/COS Calculation 3 task	Calculates the sine and cosine values of phase θ ・Allows phase interpolation and clipping
	Output Voltage Transformation task	・Coordinate axis transformation (inverse Park transformation) Two types of phase transformation (space vector modulation and inverse Clark transformation)
	Output Control task	Converts three-phase voltage into PWM output settings for the PMD (two types) ・Allows output limiting ・Allows dead-time compensation
	Trigger Generation task	Calculates the PMD's AD conversion sampling timing from three-phase duty cycles
	Current Correction Preparation task	Corrects detected current values for low inductance motor. Used in combination with Input Process 3 and Input Process 6 tasks.
	Input Process tasks	Reads conversion results from the MADC and converts them into fixed-point values (six types) Supports current polarity determination (hysteresis/reverse hysteresis)
	Input current transformation	・Phase transformation (Clark transformation) ・Coordinate axis transformation
	Individual functions	・Arctangent (ATAN) calculation ・Square-root calculation ・No Operation(NOP)
	Position Estimation task	・Calculates electrical angle speed and phase θ from motor parameters, voltage, and current
	Position Sensor Input Process task	Calculates phase θ and electric angular velocity from the inputs from a position sensor such as an encoder that generates multiple pulses per revolution
Schedule management	Program Schedule control	・Program schedule capable of defining the order in which to execute tasks and their start-up control ・Supports up to 32 tasks
	Start-up control	・Repetition start ・Starts the input schedule upon completion of an AD conversion Starts executing an Input Process task upon ADC-complete interrupt when the VE is in the Standby state following the completion of an output schedule
Interrupt control	Schedule-complete interrupt	Generates an interrupt when a task with the END flag set to "1" is executed repeatedly for the specified number of times ([REPTIME]).

	Error interrupt	Interrupt generated when the VE receives a PWM interrupt from the PMD during the execution of an output schedule, judging it as an error.
Other	Outputs for debugging	Outputs a signal that indicates that the task is running by toggling the debug output when the task starts and stops. For example, depending on the timing of the PMD debug output, the period indicating the operation may appear to be inverted (L output). This can be monitored by the debug output function of the PMD.

9.8. Programmable Motor Driver(PMD)

Table 9.8.1 PMD Function List

Category	Function	Description
PWM output	Resolution	The count resolution for PWM carriers is 1/VECLK. The PWM frequency and duty cycle are programmed with 15-bit values.
	PWM carrier generation	Capable of generating PWM carriers with a frequency between 0.06 kHz and 117.18 kHz (when VECLK=60 MHz) and with a 15-bit amplitude ・ Four types of carrier waveform (triangular, sawtooth, inverted triangular, and inverted sawtooth) ・ Selectable carrier waveforms for each phase ・ Capable of producing phase differences between the base carrier and each of the U, V, and W phases independently.
	Three-phase PWM generation	Three-phase PWM waveforms are generated by comparing the PWM carriers and the programmed duty cycles. The duty cycles of the three phases can be the same or independently programmed.
	Commutation control	Each of the six output ports can be programmed to be driven to the PWM output level, logic High, or logic Low. PWM waveforms can be generated independently for each of the three phases with a common PWM carrier (three-phase complementary PWM).
AD conversion triggering	Synchronous ADC trigger generation	Generates MADC synchronous trigger signals to start AD conversion at any timing synchronous to the PWM carrier
Protection functions	Protection control	Turns off the PWM outputs in response to a protection input signal ・ Provides two types of protection control (EMG and OVV)
	Dead-time control	Inserts a dead-time period to prevent a short-circuit between high-side and low-side switches (U/X, V/Y, W/Z) during their switching when generating three-phase complementary PWM signals
Register buffering	–	Double- and triple-buffered registers allow the PWM period, duty cycles, ADC trigger timing, and the commutation control settings for the six output ports to be changed dynamically. ・ The update timing of execute buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, and 4) the center and end of the PWM period. ・ The update timing of intermediate buffers is selectable from: 1) asynchronous, 2) the center of the PWM period, 3) the end of the PWM period, 4) the 1/4 point of the PWM period, 5) the 3/4 point of the PWM period, 6) center and end point of the PWM period, and 7) the 1/4 and 3/4 point of the PWM period.
Interrupt requests	PWM interrupt (INTPWM)	Capable of generating interrupt requests synchronous to a PWM waveform ・ The interrupt timing is selectable from the center and end of the base carrier. ・ The interval between PWM interrupts is selectable from one-half, one, two, and four PWM periods. ・ Capable of enabling and disabling the decimation of synchronous MADC triggers and buffer updates when interrupts are decimated
	EMG interrupt (INTEMC)	Interrupt request generated in the event of a protection event via an EMGx input
	OVV interrupt (INTOVV)	Interrupt request generated in the event of a protection event via an OVVx input
Debug output	–	Capable of monitoring the operating timing of the motor-related peripherals via an output port ・ Monitor timing of the synchronous MADC trigger output from the PMD ・ Monitor timing of interrupt requests from motor-related peripherals ・ Monitor MADC conversion ・ Monitor timing of VE task transitions ・ Monitor ENC internal signal.

9.9. Memory Map

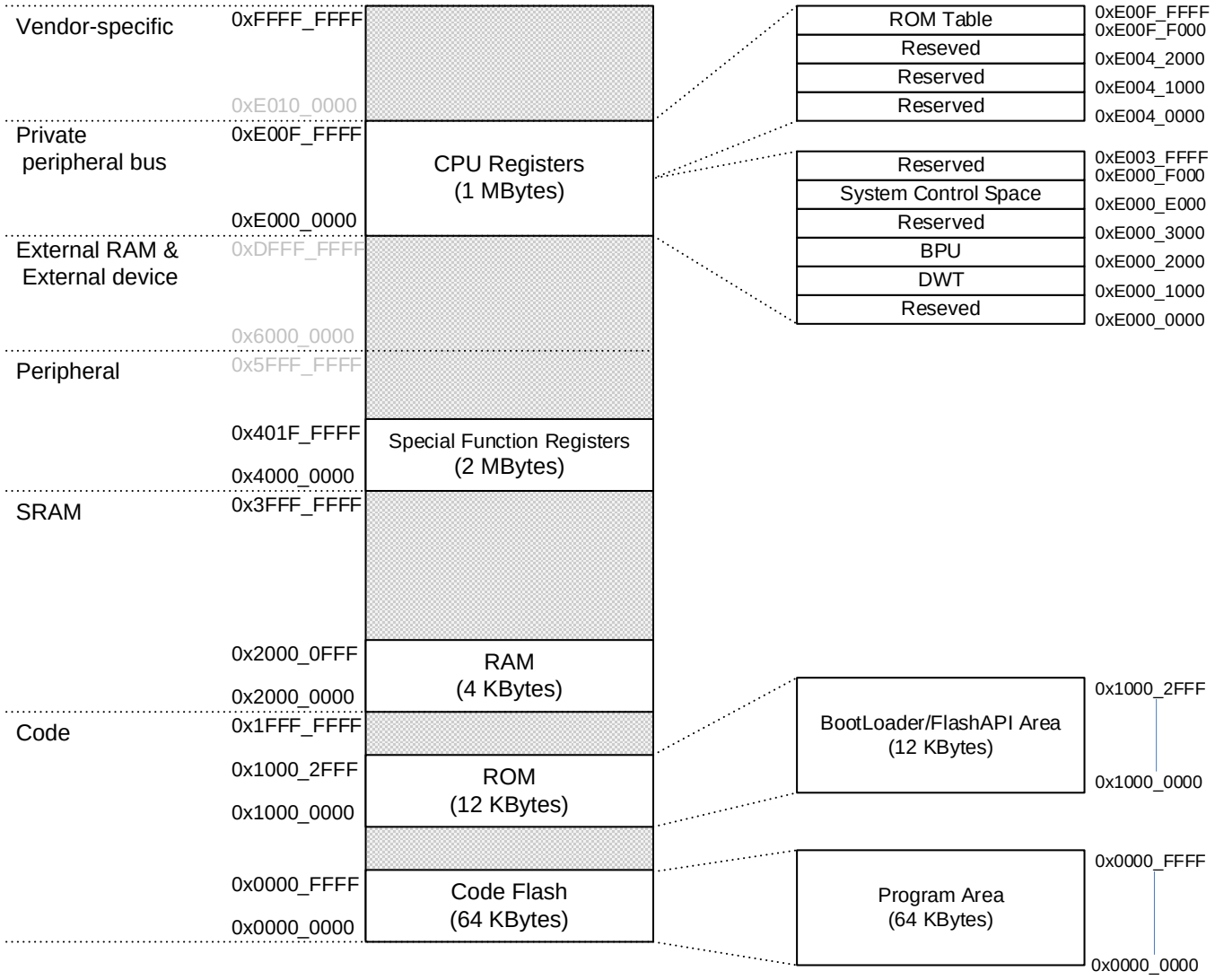


Figure 9.9.1 Memory Map

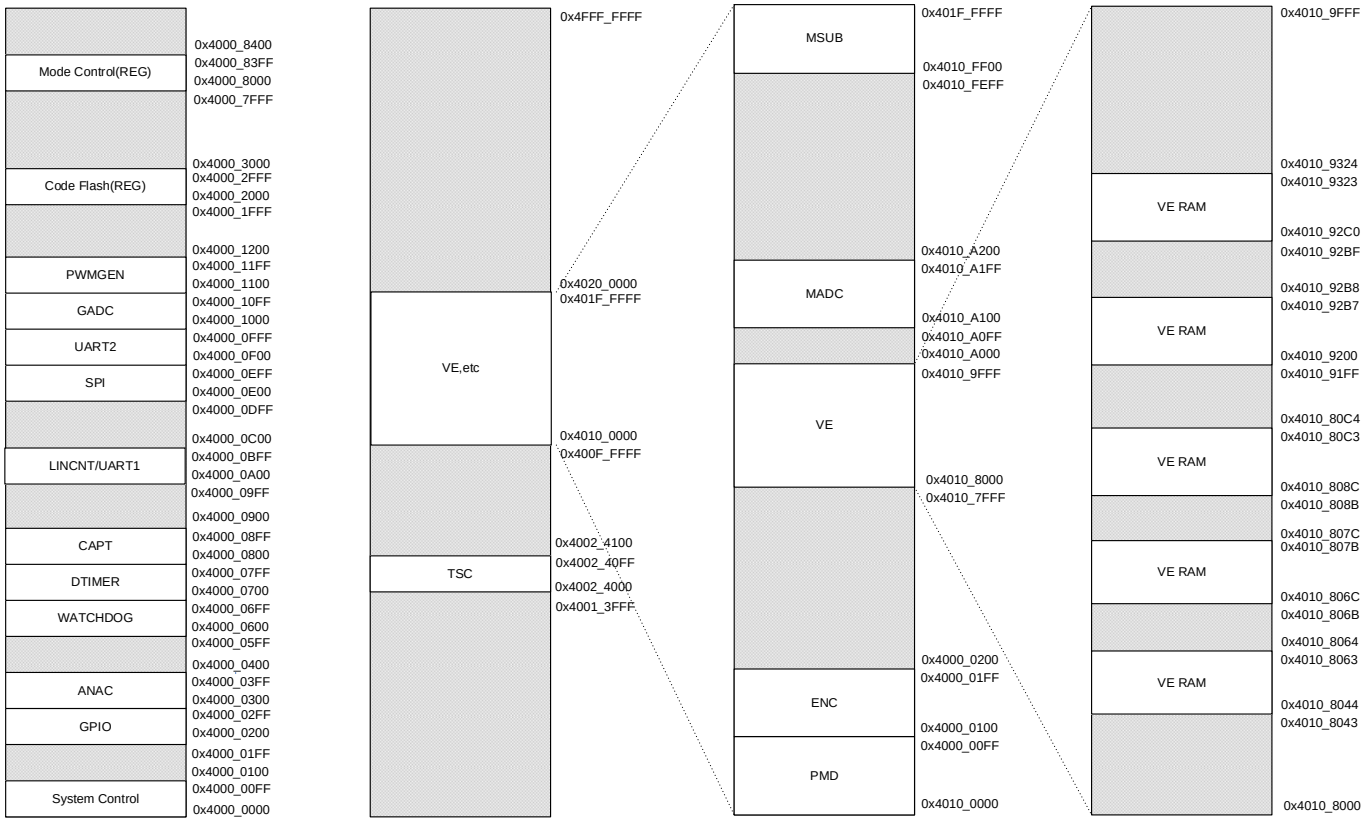


Figure 9.9.2 Memory Map

10. Absolute Maximum Ratings

Table 10.1 Absolute Maximum Ratings

Characteristic	Symbol	Pin(s)	Rating	Unit
Supply voltage	Vbat	VBAT	-0.3 to +40	V
	Vcp	VCP	-0.3 to +40	
	Vcc	VCC, VREF	-0.3 to +6	
	Vdd	VDD	-0.3 to +2.1	
Ground-to-ground voltage differential	Vgnd	GNDA, GNDD, GNDP, GNDLIN	-0.3 to +0.3	
Input voltage	Vin1	LIN	-27 to +40 *1	V
	Vin2	VBATD,	-0.3 to Vcp+0.3 (40 V max)	
	Vin3	PWMIN	-4 to Vbat+0.3 (40 V max) *2, *5	
	Vin4	VMON	-0.3 to Vbat+0.3 (40 V max)	
	Vin5	U, V, W, COM, SLC	-2.5 to Vcp+0.3 (40 V max) *3, *6	
	Vin6	RSH, RSL	-2 to Vbat+0.3 (40 V max)*5	
	Vin7	TEST, MD0, MD1, RESETN GPIO_x, XIN	-0.3 to Vcc+0.3 (6 V max)	
Output voltage	Vout1	LIN	-27 to +40 *1	V
	Vout2	GHU, GHV, GHW GLU, GLV, GLW	-0.3 to Vcp+0.3 (40 V max) *4	
	Vout3	CP1H, CP2H	-0.3 to Vcp+0.3 (40 V max)	
	Vout4	CP1L, CP2L	-0.3 to Vbat+0.3 (40 V max)	
	Vout5	XOUT, RESETN GPIO_x	-0.3 to Vcc+0.3 (6 V max)	
Operating temperature	Ta	-	-40 to +150	℃
Storage temperature	Tstg	-	-55 to +150	℃

* None of the absolute maximum ratings must be exceeded even instantaneously. Exposure to stress exceeding absolute maximum ratings might cause permanent destruction or degradation of an IC and adversely affect other components.
Ensure that none of the absolute maximum ratings is exceeded under any operating conditions.
Use the IC within the specified operating ranges.
* At outside the ±18-V range, there is a limit to the period during which the TB9M003FG may be exposed to such conditions: ≤ 90 minutes at 18 to 28 V and ≤ 400 ms at 28 to 40 V

*1: VBAT = 6.0 to 18 V
*2: Vin3 is the voltage applied by connecting 10kΩ minimum in series.
*3: Vin5 is the voltage applied by connecting 47Ω minimum in series.
*4: Vout2 is the voltage applied by connecting 47Ω minimum in series.
*5: The voltage between VBAT and RSH, RSL should not exceed -0.3V to +40V.
*6: The voltage between VCP and U, V, W, COM, SLC should not exceed -0.3V to +40V.

11. Operating Ranges

Table 11.1 Operating Ranges

Characteristic	Symbol	Rating	Unit	Remarks
Supply voltage	Vbat	18 to 27	V	Electrical characteristics are not guaranteed(*).
		6 to 18		Vbat range in which electrical characteristics are guaranteed.
		4.8 to 6		Electrical characteristics are not guaranteed(*).
Operating temperature	Topr	-40 to 150	°C	Ambient temperature, Ta
		-40 to 175		Junction temperature, Tj(*)

* Not tested in a pre-shipment test

12. Electrical Characteristics

12.1. Overall Electrical Characteristics

Table 12.1.1 Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Standby current 1	Istby1	VBAT VBATD VMON	Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=25°C	-	-	20	µA
Standby current 2	Istby2		Standby mode LFCLK OFF VBAT=VBATD=12 V, Ta=70°C Guaranteed by design	-	-	90	µA

Reference information

The current consumption at the VBAT pin is approximately 33mA under the following conditions.

VBAT=12V, room temperature, HFCLK used, SYSCLK=40MHz, VECLK=60MHz (reset state),

LIN is disabled, CGP is enable, PREDRV is disabled (no external FET gate drive),

No other IC external load.

Current consumption varies depending on usage conditions such as CPU load and operating frequency.

12.2. 5-V Regulator (LDO5V)

Table 12.2.1 Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VCC output voltage 1	Vcc1	VCC	Iload = -10 µA to -135 mA (Total VCC/VDD current consumption of maximum self-consumption current inside the IC and external load current (max 60mA)) Tj = -40 to 150°C	4.9	5.0	5.1	V
VCC output voltage 3	Vcc3		Iload = -10 µA to -135 mA (Total VCC/VDD current consumption of maximum self-consumption current inside the IC and external load current (max 60mA)) Tj = 150 to 175°C	4.8	5.0	5.2	V
Current limit 1	Ilimit1		VCC ≥ 4.0 V	-850	-475	-250	mA
Current limit 2	Ilimit2		VCC ≤ 3.0 V	-250	-112	-10	mA
Dropout voltage	Vdrop		Vbat = 4.8 V,Iload = -120 mA < (-5mA + current consumed by LDO5V)	-	0.2	0.45	V
Undervoltage detection voltage 1	Vrst1		VCC falling (UV_VCC)	4.0	-	4.35	V
Undervoltage release voltage 1	Vrstr1		VCC rising (UV_VCC)	4.2	-	4.75	V
Undervoltage detection voltage 3	Vrst3		VCC falling (POR5V)	3.07	3.45	3.83	V
Undervoltage release voltage 3	Vrstr3		VCC rising (POR5V)	3.22	3.60	3.98	V

Note:
Connect a capacitor of 1.0 µF or more as close as possible to the VCC pin.
The current limit at VCC in Standby mode is Current Ilimit2.

12.3. 1.5-Voltage Regulator (LDO15V)

Table 12.3.1 Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
VDD output voltage	Vdd	VDD	Iload = -10 µA to -60 mA + (Total VDD current consumption of maximum self-consumption current inside the IC and external load current (max 1mA))	1.45	1.5	1.55	V
Current limit 3	Ilimit3		-	-250	-150	-70	mA
Undervoltage detection voltage 2	Vrst2		VDD falling	1.3	-	1.4	V
Undervoltage release voltage 2	Vrstr2		VDD rising	1.35	-	1.45	V
Overvoltage detection/release voltage	Vddov		-	1.55	-	1.65	V

Note: Connect a capacitor of 2.2 µF or more as close as possible to the VDD pin.

12.4. Charge Pump

Table 12.4.1 Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Output voltage 1	Vcp1	VCP	VBAT = 6 V, Iload = -10 µA to -31.8mA, Cload=15,000 pF	VBAT +6.5	-	-	V
Output voltage 2	Vcp2		VBAT = 8 to 18V, Iload = -10 µA to -31.8mA, Cload=15,000 pF	VBAT +10	VBAT +12	VBAT +14	V
Output voltage 3	Vcp3		VBAT=5 V, Iload = -10 µA to -13.8mA, Cload=5,500 pF	VBAT +6.5	VBAT +8.7	-	V
Boost overvoltage detection threshold voltage	Vcplim1		-	31	33	35	V
Boost overvoltage recovery threshold voltage	Vcplim_r1		-	29.5	31.5	33.5	V
Boost disable threshold voltage 1	Vcpstop1	VBAT	-	27	28.5	30	V
Boost enable threshold voltage 1	Vcpstop_r1		-	26	27.5	29	V
Boost disable threshold voltage 2	Vcpstop2	VCP	-	34	36	38	V
Boost enable threshold voltage 2	Vcpstop_r2		-	32	34	36	V
Boost frequency	Fcp	-	-	237.5	250	262.5	kHz
Rise time	Tcp	VCP	Time from when the boost start signal is asserted to when the output voltage reaches 90% of VCP (See Figure 12.4.1)	-	-	1	ms

Note: Enable the charge pump when VBAT ≥ 5 V.

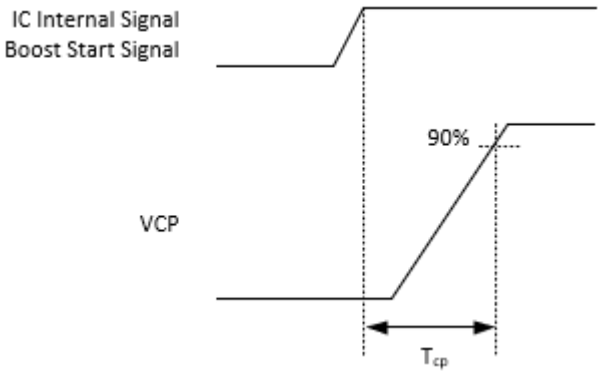


Figure 12.4.1 Measurement of Rise Time

12.5. Oscillator

Table 12.5.1 Electrical Characteristics

VBAT=6 to 18 V, VCC=4.8 to 5.2 V, VDD=1.45 to 1.55 V, and Tj=-40 to 175°C unless otherwise noted

Characteristic	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Oscillation frequency 1 (HFCLK)	Fosc1	-	-	19	20	21	MHz
Oscillation frequency 2 (LFCLK)	Fosc2	-	-	24	32	40	kHz
Oscillation frequency 3 (XCLK)	Fosc3	XIN XOUT	Values of a usable external ceramic resonator or crystal	16(*)	-	20(*)	MHz

Note: Typical value of an external oscillator.
Contact the manufacturer of external components for the matching with XCLK.
Toshiba has tested the CSTNE16M0VH3C000R0 and CSTNE20M0VH3C000R0 and confirmed that they operate with the XCLK properly.

13. Application Circuit Example

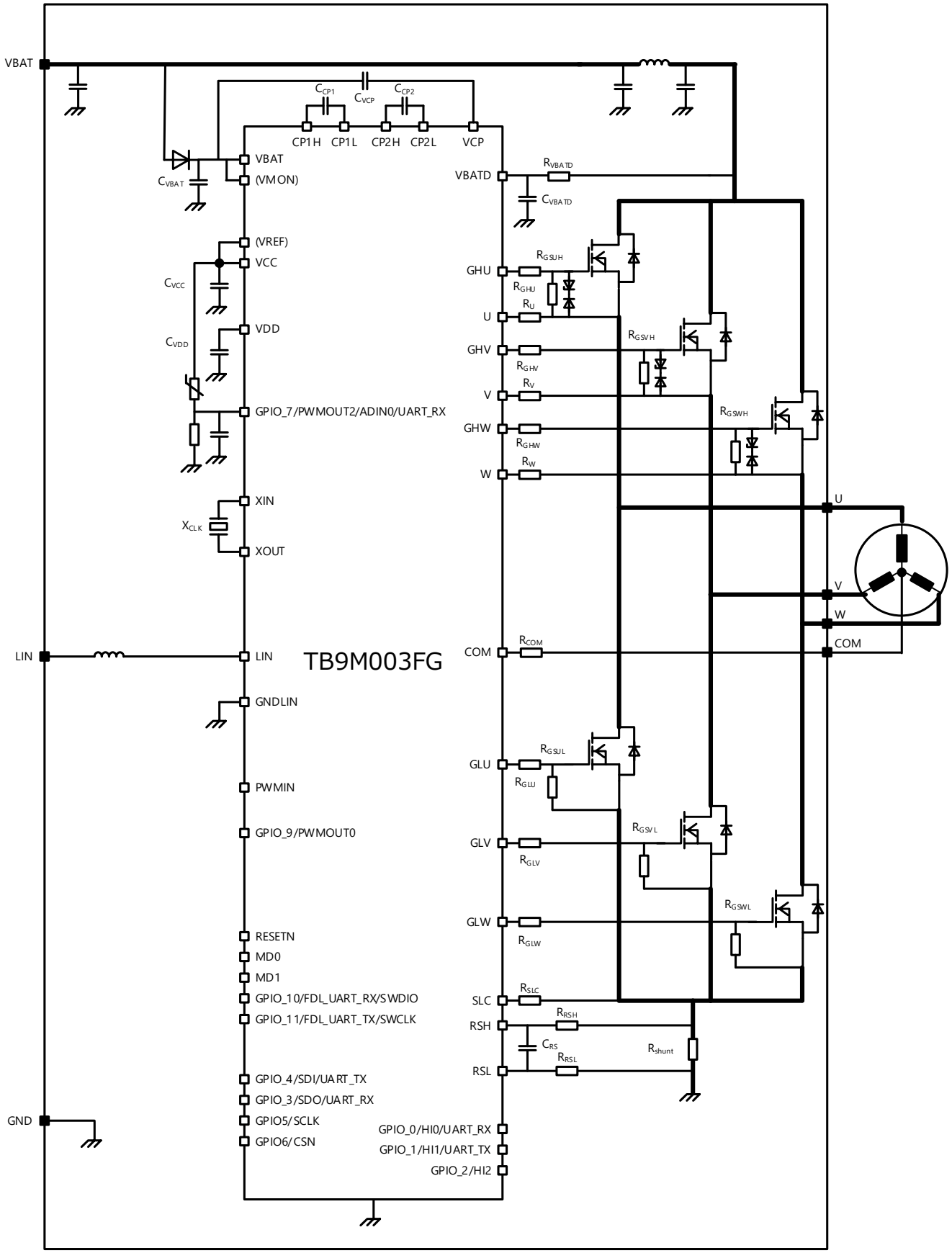
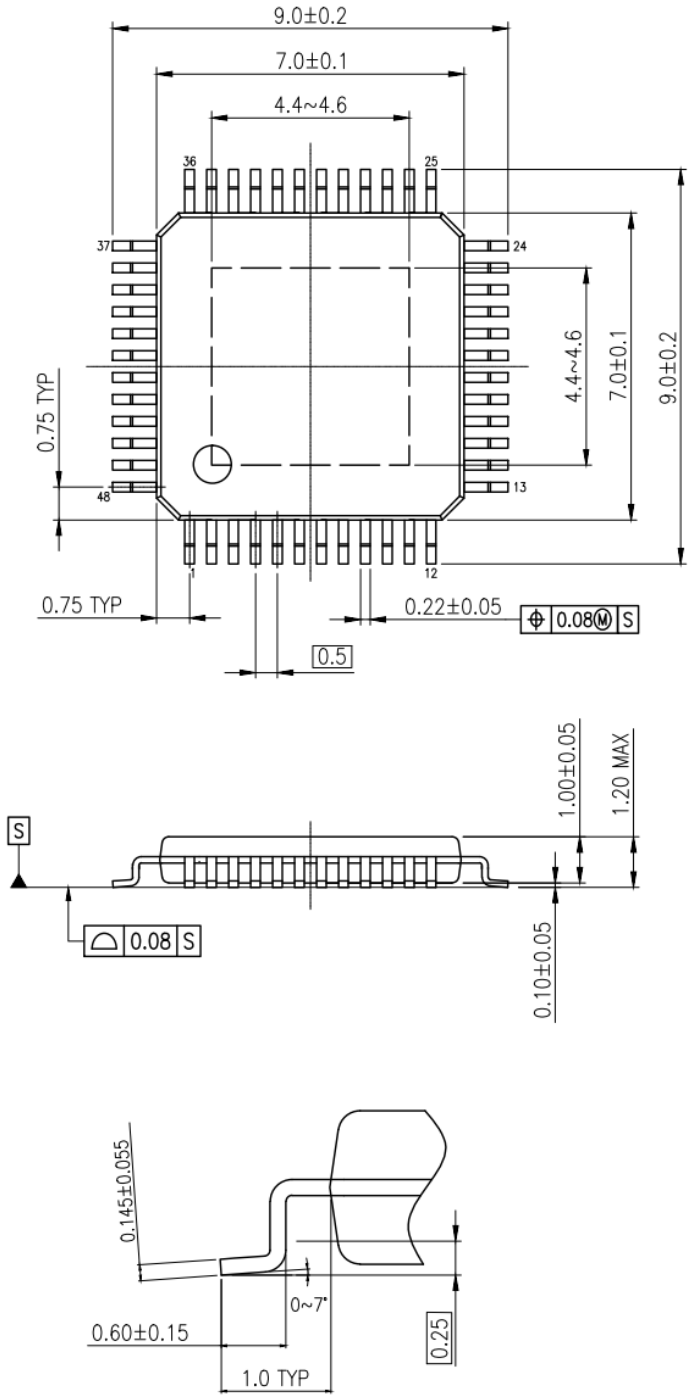


Figure 13.1 Application Circuit Example

14. Package Information

14.1. Package Dimensions

P-HTQFP48-0707-0.50-001 "Unit:mm"



Weight: 0.14 g (typ.)

Figure 14.1 Package Dimensions

14.2. Marking

Product name：TB9M003FG

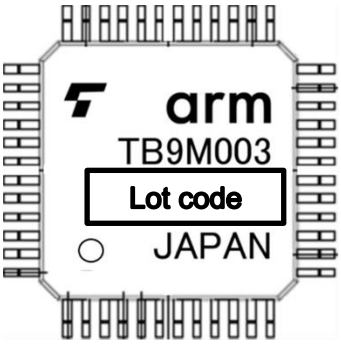
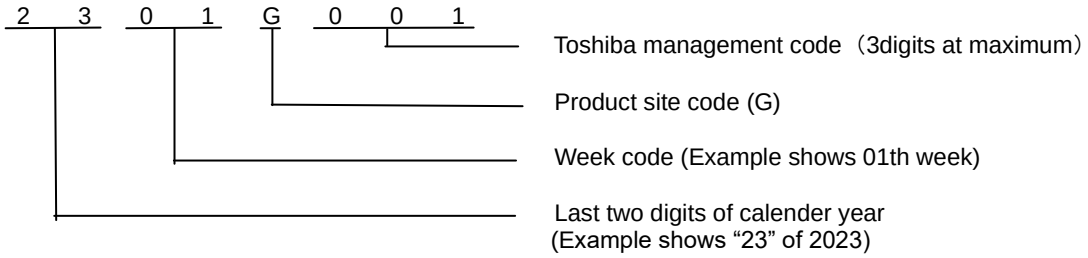


Figure 14.2 Marking

Example : Lot code



15. IC Usage Considerations

15.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure.

15.2. Points to Remember on Handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature clears the heat generation status immediately.

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