MOSFETs Silicon P-Channel MOS

SSM3J65CT

1. Applications

- Power Management Switches

2. Features

(1) 1.2 V drive

(2) Low drain-source on-resistance

: $R_{DS(ON)}$ = 1110 mΩ (typ.) (@V_{GS} = -1.2 V)

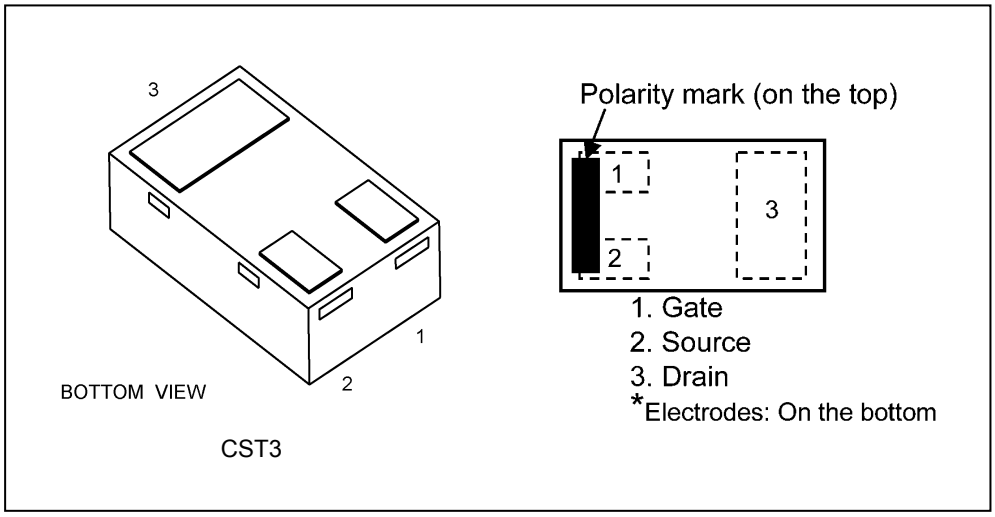
$R_{DS(ON)}$ = 780 mΩ (typ.) (@V_{GS} = -1.5 V)

$R_{DS(ON)}$ = 650 mΩ (typ.) (@V_{GS} = -1.8 V)

$R_{DS(ON)}$ = 510 mΩ (typ.) (@V_{GS} = -2.5 V)

$R_{DS(ON)}$ = 400 mΩ (typ.) (@V_{GS} = -4.5 V)

3. Packaging and Pin Assignment



Start of commercial production
2023-12

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4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	±10	
Drain current (DC)	(Note 1)	I_D	-700	mA
Drain current (pulsed)	(Note 1)	I_{DP}	-1400	
Power dissipation	(Note 2)	P_D	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm^2)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

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5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 5 V	-15	—	—	
Gate threshold voltage	(Note 2)	V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	
Drain-source on-resistance	(Note 3)	$R_{DS(ON)}$	I_D = -10 mA, V_{GS} = -1.2 V	—	1110	11300	mΩ
			I_D = -50 mA, V_{GS} = -1.5 V	—	780	1550	
			I_D = -100 mA, V_{GS} = -1.8 V	—	650	1070	
			I_D = -300 mA, V_{GS} = -2.5 V	—	510	700	
			I_D = -500 mA, V_{GS} = -4.5 V	—	400	500	
Forward transfer admittance	(Note 3)	$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -700 mA	—	2.2	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 3: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	48	—	pF
Reverse transfer capacitance	C_{rss}		—	4.6	—	
Output capacitance	C_{oss}		—	8.9	—	
Switching time (turn-on time)	t_{on}	V_{DD} = -10 V, I_D = -100 mA, V_{GS} = 0 to -4.5 V, R_{GS} = 50 Ω	—	130	—	ns
Switching time (turn-off time)	t_{off}	Duty ≤ 1 %, V_{IN}: t_r, t_f < 5 ns, Common source, See Chapter 5.3.	—	1075	—	

5.3. Switching Time Test Circuit

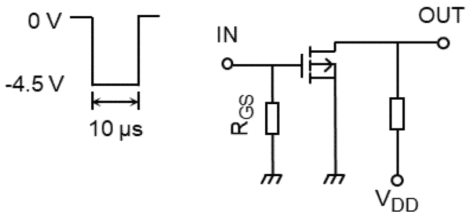


Fig. 5.3.1 Switching Time Test Circuit

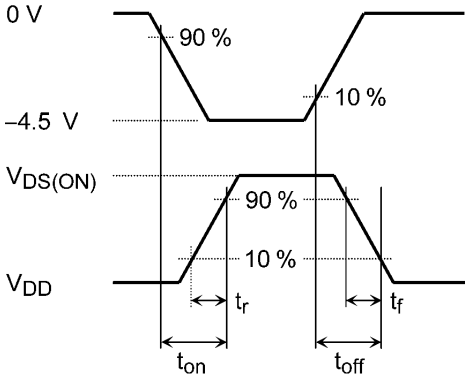


Fig. 5.3.2 Input Waveform/Output Waveform

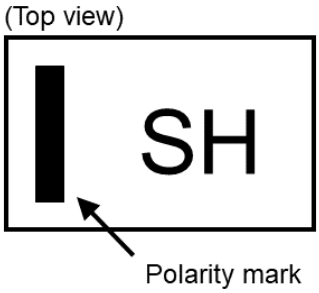
5.4. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	I_D = 700 mA, V_{GS} = 0 V	—	0.94	1.2	V

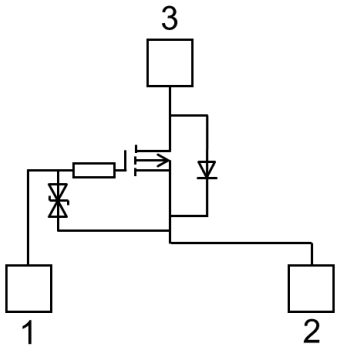
Note 1: Pulse measurement.

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6. Marking



7. Equivalent Circuit



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8. Characteristics Curves (Note)

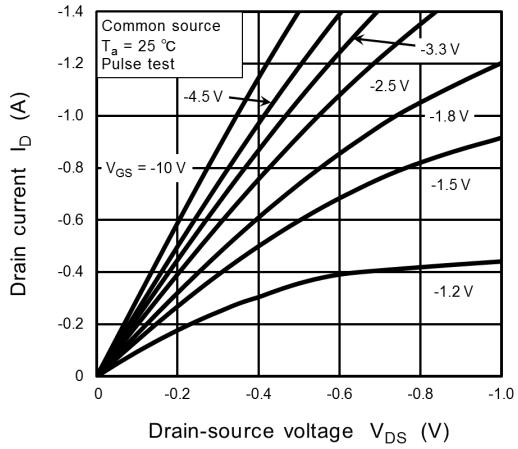


Fig. 8.1 I_D - V_{DS}

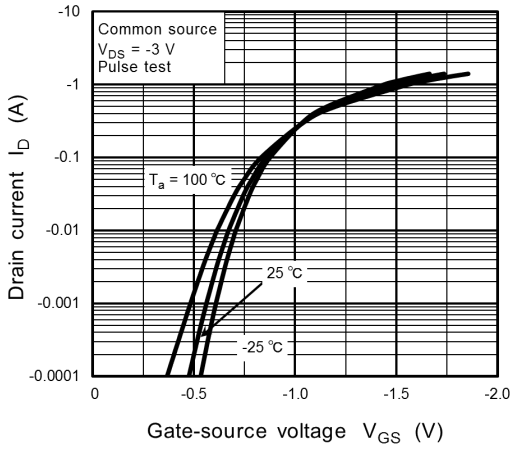


Fig. 8.2 I_D - V_{GS}

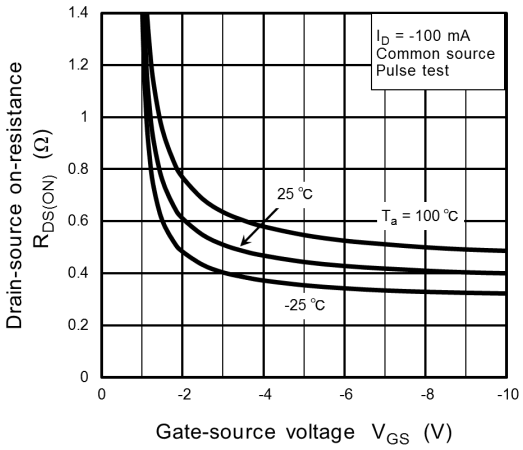


Fig. 8.3 $R_{DS(ON)}$ - V_{GS}

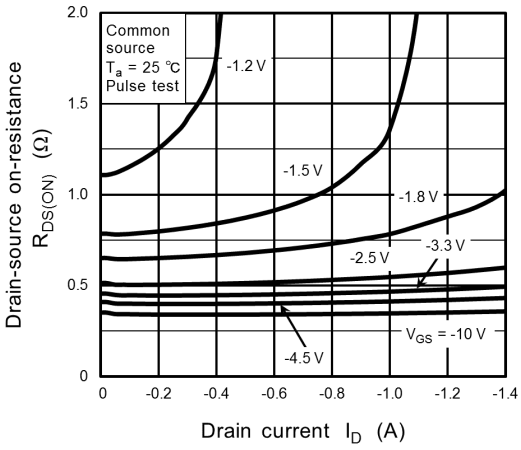


Fig. 8.4 $R_{DS(ON)}$ - I_D

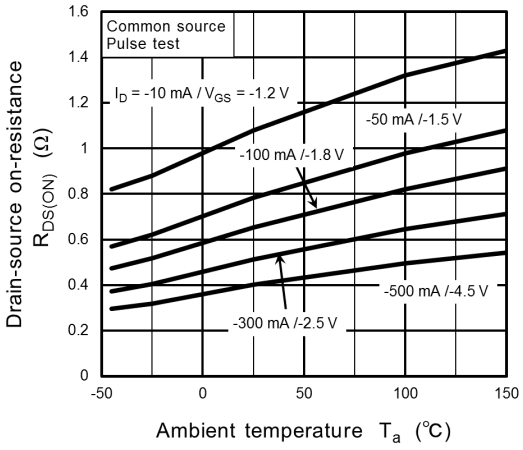


Fig. 8.5 $R_{DS(ON)}$ - T_a

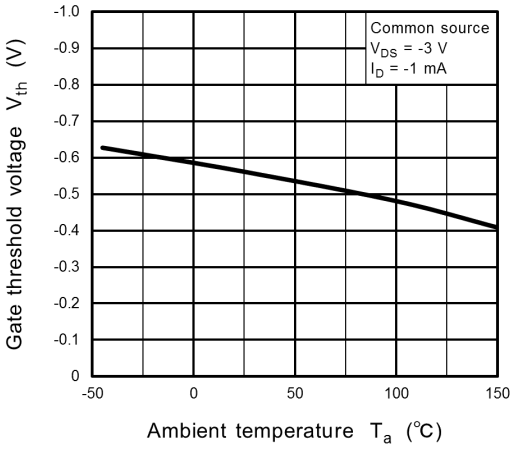


Fig. 8.6 V_{th} - T_a

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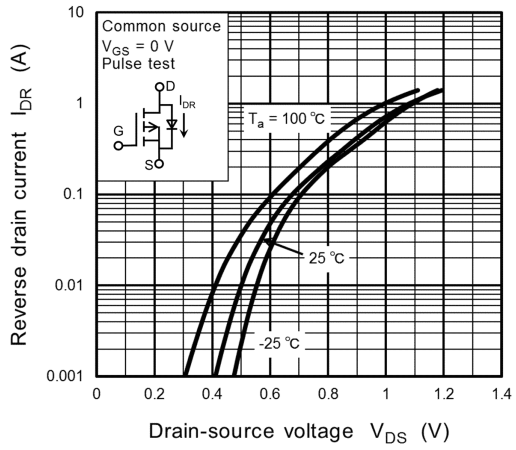


Fig. 8.7 I_{DR} - V_{DS}

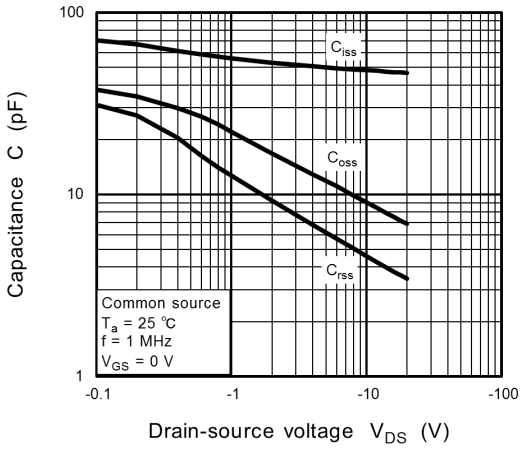


Fig. 8.8 C - V_{DS}

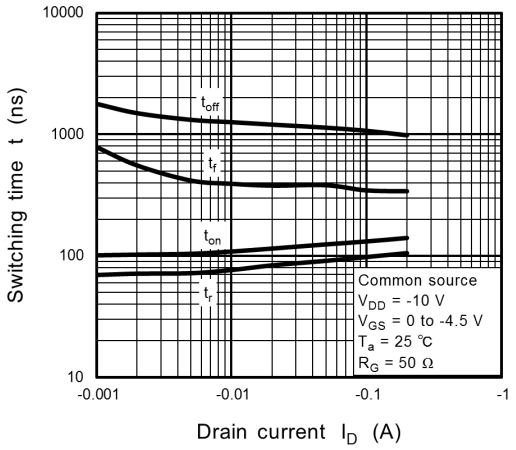


Fig. 8.9 t - I_D

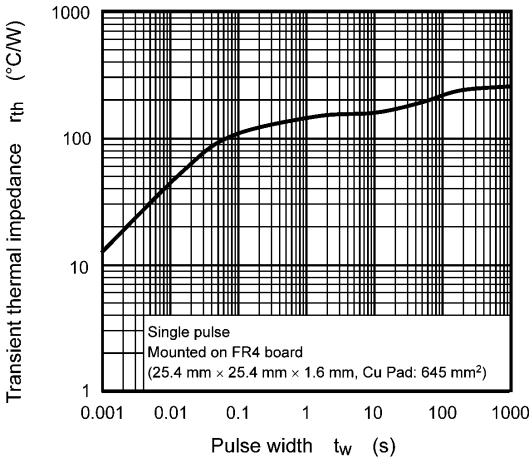


Fig. 8.10 r_{th} - t_w

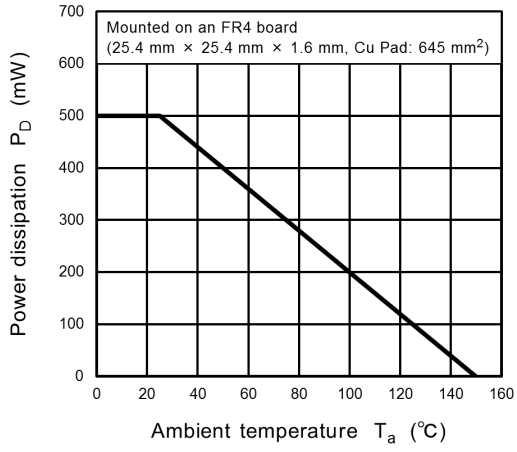
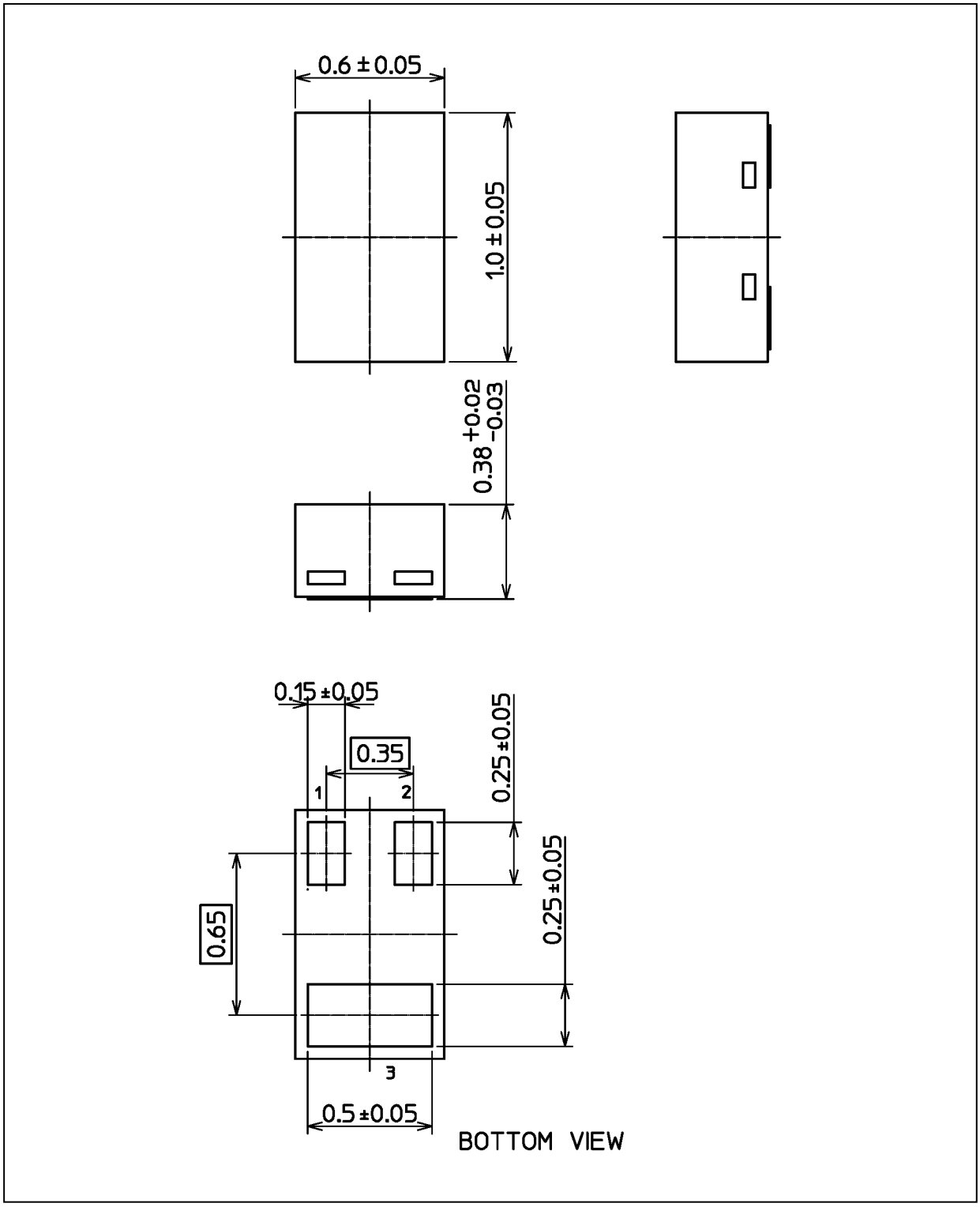


Fig. 8.11 P_D - T_a

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Package Dimensions

Unit: mm



Weight: 0.75 mg (typ.)

Package Name(s)
Nickname: CST3

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