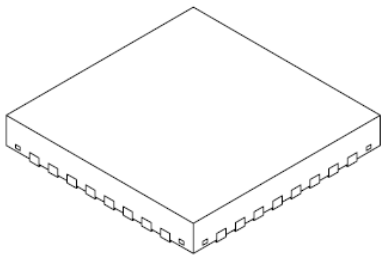
TOSHIBA CDMOS Integrated Circuit Silicon Monolithic

TC7735FTG

System power management IC for TFT / low-temperature polysilicon liquid crystal display



P-WQFN32-0505-0.50-001

Weight: 0.06 g (Typ.)

1. Summary

The TC7735FTG is a system power management IC for liquid crystal module of TFT and low-temperature polysilicon. It can generate each voltage level, which the liquid crystal display (LCD) driver requires. In addition, the TC7735FTG can generate the high-voltage power supply for source driver and gate driver and incorporates VCOM amplifier circuit. So, it can drive the LCD of TFT and low-temperature polysilicon easily by itself.

The TC7735FTG can also output the required voltage to connect various LCD drivers by incorporating the function of adjusting voltage. This optimizes the characteristics of whole LCD system. And the protection functions like the over current protection circuit and the under voltage lockout circuit are incorporated to improve safety in driving the IC.

2. Applications

TFT LCD module, low-temperature polysilicon LCD module, and so on

3. Features

- System power management IC for compound LCD module
  CH1: Buck/Boost DC-DC convertor
  CH2: Buck DC-DC convertor
  CH3: Positive regulated charge pump
  CH4: Negative regulated charge pump
  Op-Amp for VCOM
- Supporting input voltage in wide range: 4.5V to 16V
- Built-in power supply sequence generating circuit
- Built-in OSC circuit: 1MHz
- Capable of supplying external clocks of switching frequency
- Built-in monitor of internal state by Power Good (PG terminal.)
- Built-in input under voltage lockout circuit, input over voltage protection circuit, thermal shutdown, and output over voltage protection circuit.
- Serial communication for debug (I^2C bus)
- Power on reset function
- Operating temperature : -40 to 85°C
- Package : QFN32pin

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

4. Block diagram

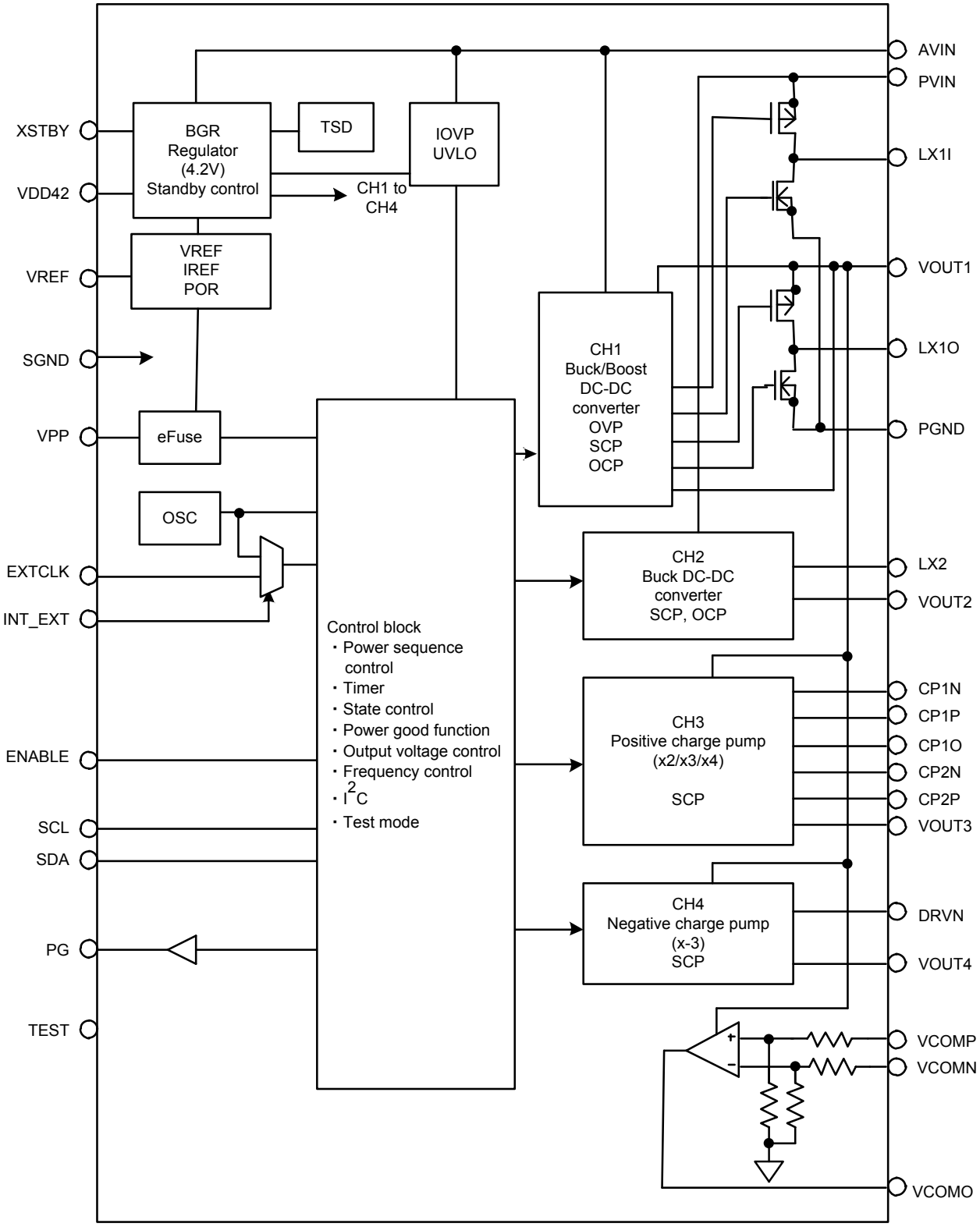


Figure 4.1 Block diagram

5. Pin assignment

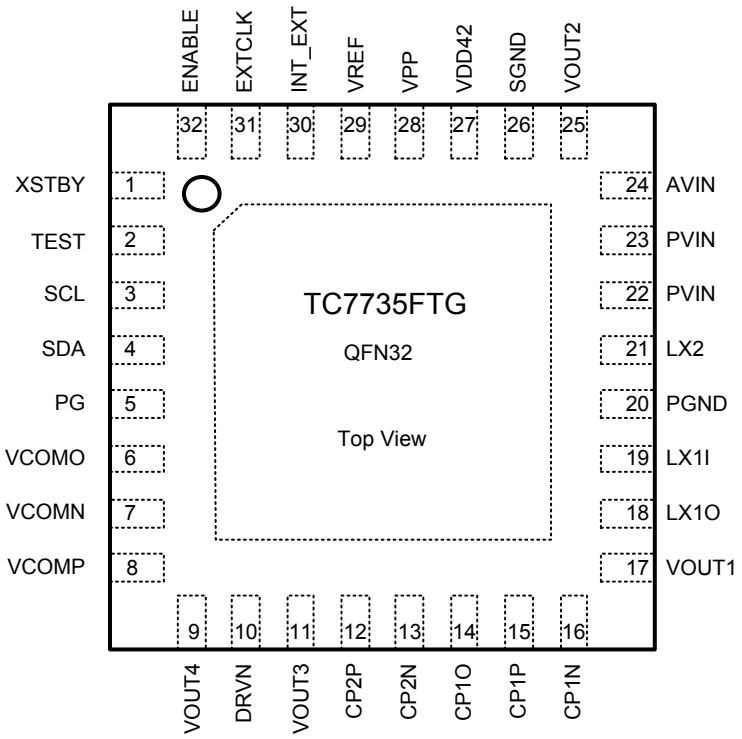


Figure 5.1 Pin assignment

Note: Package of QFN32 adopted to the TC7735FTG has a thermal pad for heat radiation on the back side of the package. Contact the back side of the package to the board by reflow and so on.

6. Pin description

Table 6.1 Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin description</th></tr>
<tr><td>PVIN</td><td>-</td><td>Power supply terminal (1)
Power supply terminal. Supply the same power supply as AVIN terminal. It is short circuited internally to AVIN terminal.</td></tr>
<tr><td>AVIN</td><td>-</td><td>Power supply terminal (2)
Analog power supply terminal. Supply the same power supply as PVIN terminal. It is short circuited internally to PVIN terminal.</td></tr>
<tr><td>PGND</td><td>-</td><td>Power GND terminal
Connect to the common ground (GND). It is short circuited internally to SGND terminal.</td></tr>
<tr><td>SGND</td><td>-</td><td>Analog GND terminal
Connect to the common ground (GND). It is short circuited internally to PGND terminal.</td></tr>
<tr><td>VDD42</td><td>O</td><td>Internal regulator output terminal
It generates the voltage of 4.2V for internal circuit. Connect the capacitor between VDD42 terminal and PGND terminal to stabilize the voltage. It cannot supply power to the external device.</td></tr>
<tr><td>VREF</td><td>O</td><td>Internal regulator output terminal
It generates the voltage of 1.5V for internal circuit. Connect the capacitor between VREF terminal and PGND terminal to stabilize the voltage. It cannot supply power to the external device.</td></tr>
<tr><td>XSTBY</td><td>I</td><td>Deep standby control terminal (with pull-down)
Deep standby terminal for the TC7735FTG. XSTBY=”L”: Operations of all circuits stop.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Enable control terminal
Enable terminal to control output voltage. Time of output voltage pattern, which is managed by control logic, can be controlled by ENABLE terminal.
Input should not be in floating state.
<table>
<tr><th>ENABLE</th><th>Functions</th></tr>
<tr><td>L</td><td>Power supplies for LCD modules (CH1 to CH4) and Op-amp for VCOM: All off</td></tr>
<tr><td>H</td><td>Power supplies for LCD modules (CH1 to CH4) and Op-amp for VCOM: All on
Each power supply starts up according to the sequence configured by the register.</td></tr>
</table></td></tr>
<tr><td>EXTCLK</td><td>I</td><td>Input terminal of external clock signal (with pull-down)
To control switching frequency of each power supply by inputting external clocks, input clocks by EXTCLK terminal. In supplying external clocks, set INT_EXT terminal high level. When external clocks are not used, configure the EXTCLK terminal open.</td></tr>
<tr><td>INT_EXT</td><td>I</td><td>Input terminal of clock select signal for each power supply.
It selects internal OSC clocks or external clocks for each power supply.
<table>
<tr><th>INT_EXT</th><th>Functions</th></tr>
<tr><td>L</td><td>Internal clock mode: Clocks for each power supply use internal OSC circuit.</td></tr>
<tr><td>H</td><td>External clock mode: Clocks for each power supply are supplied externally.
Input clock signal by EXTCLK terminal.</td></tr>
</table>
When INT_EXT is high level, short circuit to VDD42 terminal.</td></tr>
<tr><td>SCL</td><td>I</td><td>I^2C clock input terminal
In using I^2C communication, connect pull-up resistance. (Note 1)
When it is not used, connect it to GND.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>I^2C data input/output terminal
In using I^2C communication, connect pull-up resistance. (Note 1)
When it is not used, connect it to GND.</td></tr>
</table>

Note 1:ESD protection diode is connected to SDA and SCL terminals (VDD42 side). Pay attention that I^2C bus cannot be shared with the external IC.

Table 6.2 Pin description

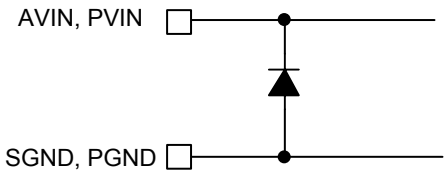
Pin name	I/O	Pin description
PG	O	Power Good output terminal PG signal outputs low level when channels of CH1 to CH4 operate normally. Connect pull-up resistance because this terminal is an open drain output terminal.
LX1I LX1O	O	Inductor connection terminal for CH1 (voltage buck/boost DC-DC convertor) Driver output terminal of voltage buck/boost DC-DC convertor. Voltage boost DC-DC convertor or buck DC-DC convertor can be constructed by connecting the inductor between LX1I terminal and LX1O terminal. Input voltage is switched to the boosting voltage or bucking voltage automatically.
VOUT1	O	Output terminal for CH1 (voltage buck/boost DC-DC convertor) Output terminal of voltage buck/boost DC-DC convertor. The voltage of LDO circuit and charge pump circuit is generated referring to the configured voltage which is outputted from VOUT1 terminal. Connect the capacitor between VOUT1 terminal and PGND terminal to stabilize the voltage.
LX2	O	Inductor connection terminal for CH2 (voltage buck DC-DC convertor) It generates the system power supply for LCD module. Available voltage range is 3V to 5V. Connect the inductor to LX2 terminal.
VOUT2	I	Feedback terminal for CH2 (voltage buck DC-DC convertor) It is a feedback input terminal to stabilize the output voltage of the voltage buck DC-DC convertor. Connect the capacitor between VOUT2 terminal and PGND terminal to stabilize the voltage.
CP1P CP1N CP2P CP2N	I/O	Capacitor connection terminal for CH3 (positive charge pump) Positive charge pump circuit can be used by connecting capacitors between CP1P terminal and CP1N terminal, and between CP2P terminal and CP2N terminal. When double charge pumps are used, terminals of CP1P and CP1N should be open.
CP1O	O	Output terminal of middle point for CH3 (positive regulated charge pump) It outputs the middle voltage of the voltage boost generated by the charge pump. Connect the capacitor between CP1O terminal and PGND terminal to stabilize the voltage. When double charge pumps are used, terminals of CP1O should be open.
VOUT3	O	Output terminal for CH3 (positive regulated charge pump) It outputs high voltage required by gate driver of LCD module. Connect the capacitor between VOUT3 terminal and PGND terminal to stabilize the voltage.
DRVN	O	Drive output terminal for CH4 (negative regulated charge pump) It outputs high voltage of negative-side required by gate driver of LCD module. Charge pump circuit is constructed by connecting the capacitor and the diode. And inverted voltage of VOUT1 is outputted.
VOUT4	I	Feedback terminal for CH4 (negative regulated charge pump) Feedback input terminal stabilizes the output voltage of the negative charge pump. Feedback the output voltage of the constructed charge-pump circuit externally.
VCOMP	I	Non-inverted input terminal of Op-amp for VCOM
VCOMN	I	Inverted input terminal of Op-amp for VCOM
VCOMO	O	Output terminal of Op-amp for VCOM
VPP	I	Voltage input terminal for eFuse Short circuit to VDD42 terminal.
TEST	I	Test terminal (with pull-down) Toshiba test terminal for shipping investigation. Connect it to the common ground (GND).

7. Equivalent circuit of input/output terminal

7.1 Power supply terminal

Table 7.1 Equivalent circuit of power supply terminal

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin name	Equivalent circuit
AVIN,PVIN PGND, SGND	

7.2 Logic input/output terminal

Table 7.2 Equivalent circuit of logic input/output terminal

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

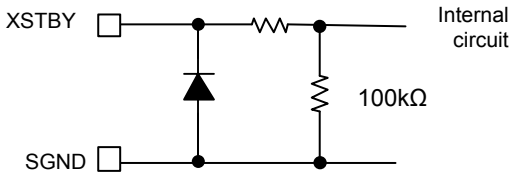
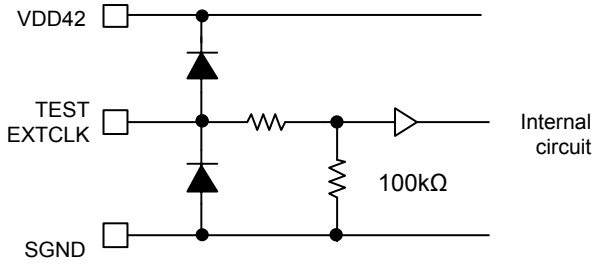
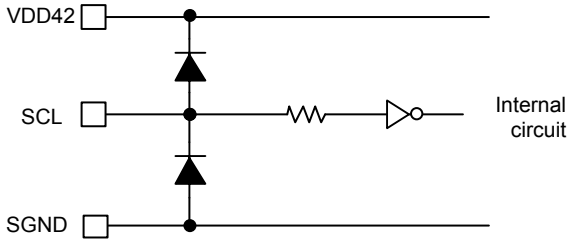
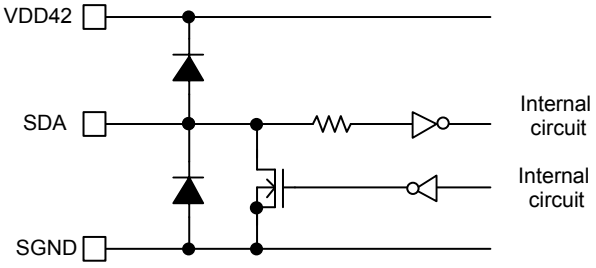
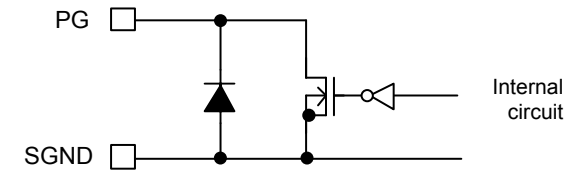
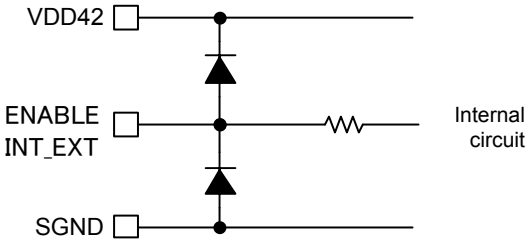
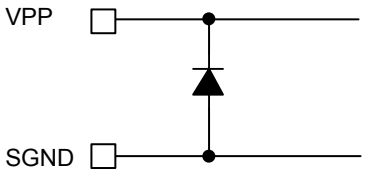
Pin name	Equivalent circuit
XSTBY	
TEST EXTCLK	
SCL	
SDA	

Table 7.3 Equivalent circuit of logic input/output terminal

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin name	Equivalent circuit
PG	
ENABLE INT_EXT	
VPP	

7.3 Analog input/output terminal

Table 7.4 Equivalent circuit of analog input/output terminal

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

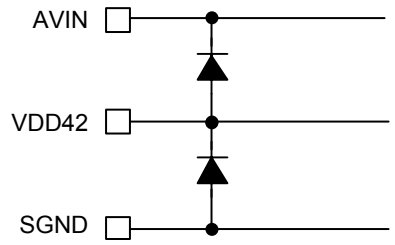
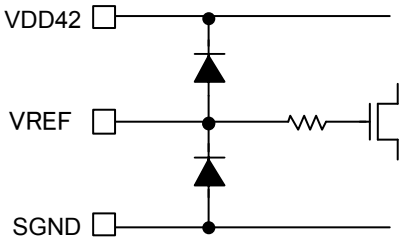
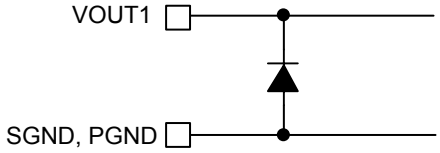
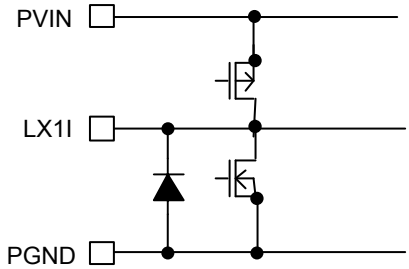
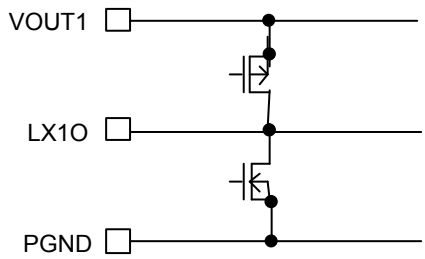
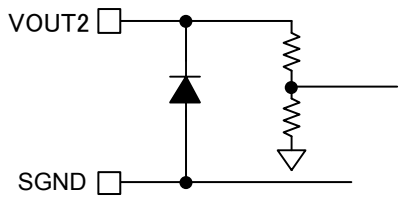
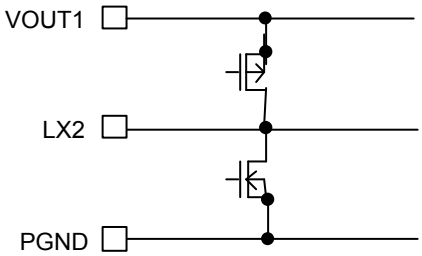
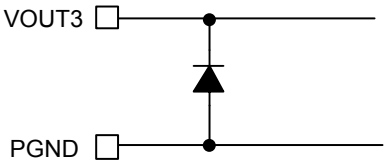
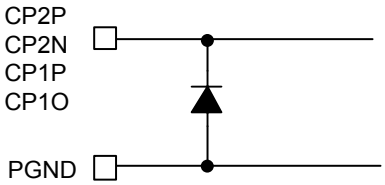
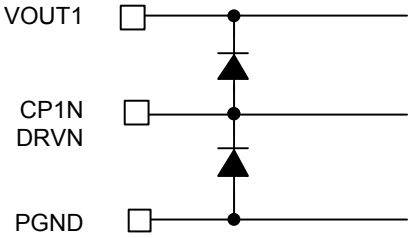
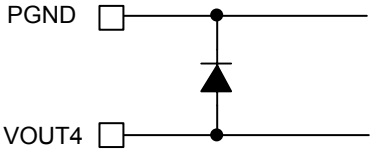
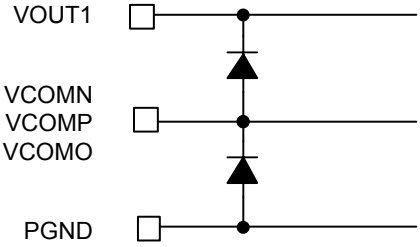
Pin name	Equivalent circuit
VDD42	
VREF	
VOUT1	
LX1I	
LX1O	

Table 7.5 Equivalent circuit of analog input/output terminal

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin name	Equivalent circuit
VOUT2	
LX2	
VOUT3	
CP2N CP2P CP1P CP1O	
CP1N DRVN	
VOUT4	
VCOMN VCOMP VCOMO	

8. Function / Operation description

The TC7735FTG can generate high voltage that LCD driver requires. It can generate the power supply for system logic (VCC) and following four kinds of power supplies. High-voltage power supply (AVDD) for source driver, high-voltage power supply (VGH) and low-voltage power supply (VGL) for gate driver, and power supply for VCOM.

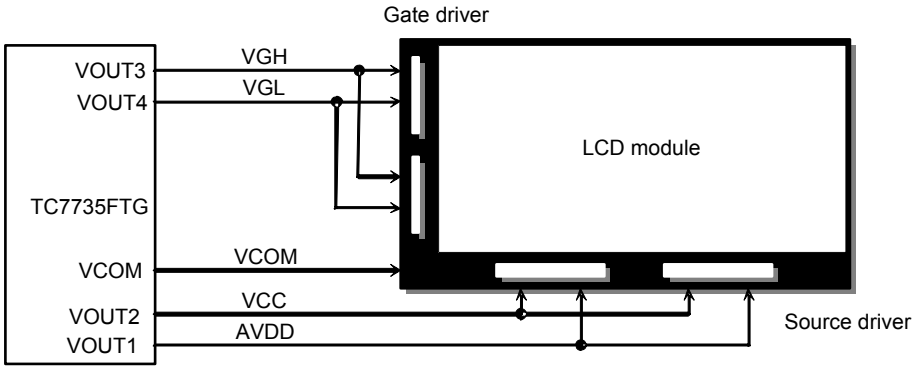


Figure 8.1 System diagram

The TC7735FTG can adjust the output voltage level of each power supply and the timing of ON/OFF sequence because it incorporates serial communication function for debug. The voltage environment can be optimized by writing these data to the internal eFuse.

Table 8.1 Setting output

Output	Standard setting product	Setting range (Note)
VOUT1	9.2V	5 to 15V (0.2V step)
VOUT2	3.3V	3 to 5V (0.1V step)
VOUT3	18.0V	14 to 22V (0.2V step)
VOUT4	-6.0V	-5 to -15V (0.2V step)

Note: Standard setting product cannot be used to change the voltage setting. Product sample for debug is required in order to change the output settings using the serial communication function.

8.1 Operation description

Operation mode of the TC7735FTG transits by the setting of XSTBY and ENABLE terminals shown in the Figure 8.2.

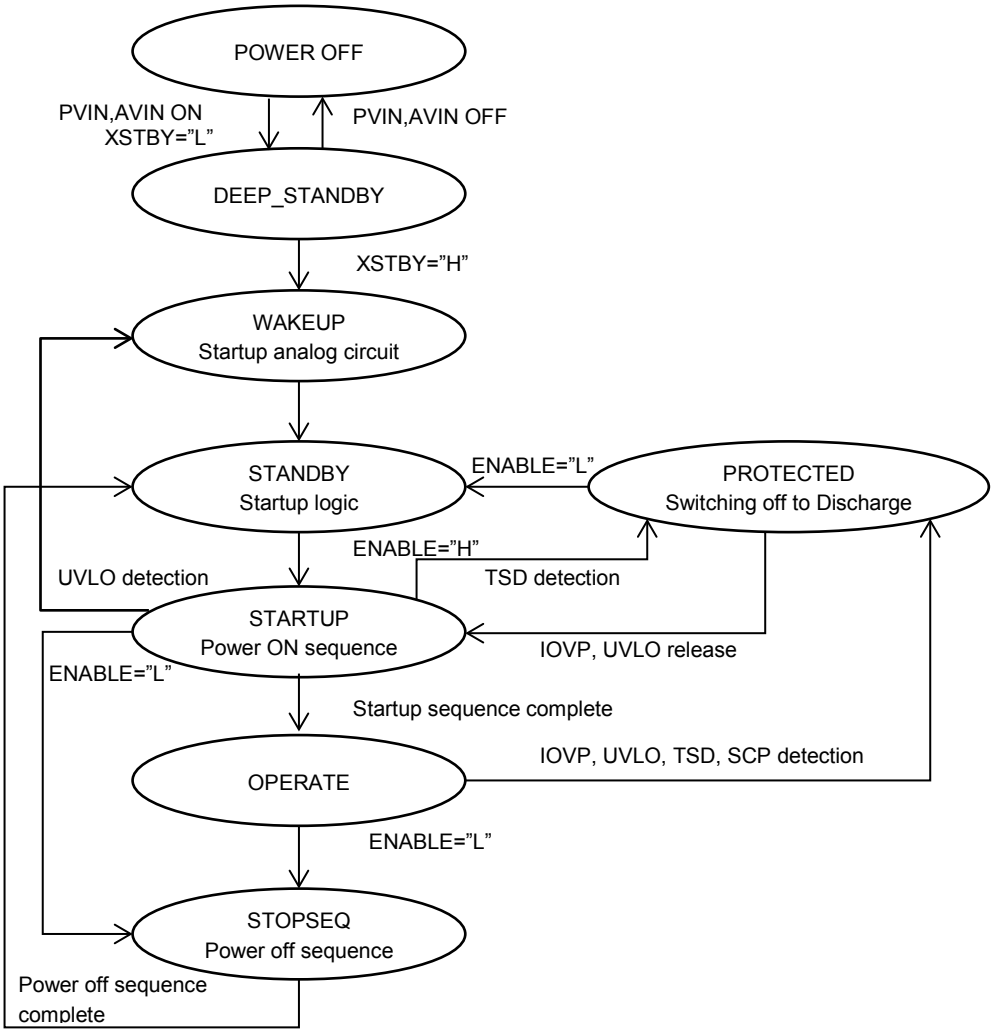


Figure 8.2 Mode transition diagram

8.1.1 DEEP STANDBY

DEEP STANDBY supplies the power supply to PVIN and AVIN. XSTBY="L" input. All of OSC circuit, internal regulator, and each power supply circuit are turned off. Low-current consumption drive can be kept even in applying voltage to the power supply of PVIN and AVIN.

8.1.2 WAKEUP

It indicates the starting up of OSC circuit and the internal regulator after inputting high level to XSTBY. Register setting value is read out from eFuse.

8.1.3 STANDBY

In STANDBY mode, all internal regulators are operating under the condition that XSTBY is "H" and ENABLE is "L". I^2C can be controlled and register setting value is kept. Each power supply circuit for driving LCD is turned off.

8.1.4 STARTUP

Channel of each power supply and Op-Amp for VCOM start soft start according to the power ON sequence by inputting high level to ENABLE from STANDBY. Power ON sequence depends on the register setting value. When soft start of all power channels and of Op-Amp for VCOM have been completed, the operation moves to the OPERATE mode. In STARTUP, all protection circuits except SCP and OVP are valid.

8.1.5 OPERATE

All power channels and Op-Amp for VCOM operate and all protection functions are enabled. PG terminal outputs low level. The operation moves to PROTECTED mode after abnormality is detected by protection functions except OCP under the following conditions; abnormality is detected continuously during delay time counted by each function.

8.1.6 STOPSEQ

After OPERATE mode, each power supply is turned off according to the power OFF sequence by inputting low level to ENABLE. Power OFF sequence depends on the register setting value. When all power supplies are turned off, the operation moves to STANDBY mode.

8.1.7 PROTECTED

PROTECTED mode is moved from STARTUP or OPERATE mode when the outputs of power channels are turned off by the protection function of IOVP, SCP, TSD, or UVLO. PG terminal is Hi-Z. When IOVP or UVLO is released, the operation moves to STARTUP mode.
When low level is inputted to ENABLE, the operation moves to STANDBY mode.

8.2 Description of register (for debug)

The TC7735FTG incorporates I^2C bus for debug to control the registers.
As shown in the Figure 8.3, pull up SCL and SDA terminals and connect them to the external MCU.

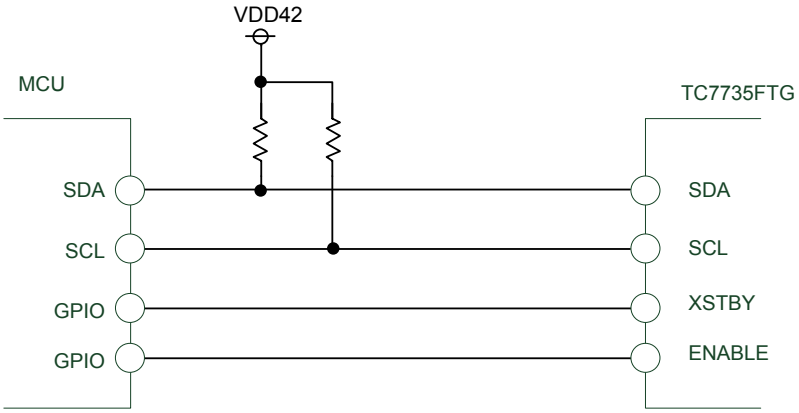


Figure 8.3 Example of connecting to MCU

Note: Register should be changed in STANDBY mode (XSTBY="H", ENABLE="L").

8.3 Register map

Refer to the below table of the register map.
Register No. 03h to 06h are enabled in product sample for debug.

Table 8.2 Register map

Register No.	D7	D6	D5	D4	D3	D2	D1	D0	R/W
00h	Reserved	SEL_REGI	SLP_SEL[1:0]		-	PWIDE_SEL[2:0]			R/W
01h	CH3TIM_SEL[1:0]		CH3DIV_SEL[1:0]		CH4DIV_SEL[1:0]		Reserved		R/W
02h	CH1_DLY[1:0]		CH4_DLY	CH1_FDLY	FSQ_SEL	-	-	-	R/W
03h	Reserved	Reserved	CH1_VSET[5:0]						R/W
04h	-	Reserved	-	CH2_VSET[4:0]					R/W
05h	-	Reserved	CH3_VSET[5:0]						R/W
06h	-	Reserved	CH4_VSET[5:0]						R/W
07h	-	TSD	UVLO	OVP	SCP_CH1	SCP_CH2	SCP_CH3	SCP_CH4	R

8.3.1 Setting (00h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	Reserved	SEL_REGI	SLP_SEL[1:0]		-	PWIDE_SEL[2:0]		
Initial value	0	0	0	1	0	0	0	1

SEL_REGI : Select eFuse or register.
To enable the register, set SEL_REGI=”1”.

Table 8.3 SEL_REGI

SEL_REGI	Function
0	eFuse: Enable
1	Register: Enable

SLP_SEL [1:0] : Adjustment register in inputting external clocks (Refer to Table 8.4)

PWIDE_SEL [2:0] : Adjustment register in inputting external clocks (Refer to Table 8.4)

Table 8.4 SLP_SEL, PWIDE_SEL

External clock frequency	SLP_SEL[1:0]	PWIDE_SEL [2:0]
400kHz to 800kHz	11	100
800kHz to 1.2MHz	01	001

Note: bit7: Fix to ”0”.

8.3.2 Setting (01h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01h	CH3TIM_SEL[1:0]		CH3DIV_SEL[1:0]		CH4DIV_SEL[1:0]		Reserved	
Initial value	0	0	1	0	1	0	1	0

CH3TIM_SEL [1:0] : CH3: Setting the number of multiple steps of the positive charge pump.

Table 8.5 CH3TIM_SEL

CH3TIM_SEL [1:0]	Number of multiple steps
00	×4
01	×3
10	×2
11	Setting forbidden

CH3DIV_SEL [1:0] : CH3: Setting the ratio of frequency dividing of the positive charge pump.
Switching frequency recommended value is 125kHz.

Table 8.6 CH3DIV_SEL

CH3DIV_SEL[1:0]	Ratio of dividing frequency
00	1/2
01	1/4
10	1/8
11	Setting forbidden

CH4DIV_SEL [1:0] : CH4: Setting the ratio of frequency dividing of the negative charge pump.
Switching frequency recommended value is 125kHz.

Table 8.7 CH4DIV_SEL

CH4DIV_SEL[1:0]	Ratio of dividing frequency
00	1/2
01	1/4
10	1/8
11	Setting forbidden

Note: bit1-0: Fix to ”10”.

8.3.3 Setting (02h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02h	CH1_DLY[1:0]		CH4_DLY	CH1_FDLY	FSQ_SEL	-	-	-
Initial value	0	0	0	0	0	0	0	0

CH1_DLY [1:0] : Setting the rising delay time of CH1 output.

Table 8.8 CH1_DLY

CH1_DLY[1:0]	Delay time
00	40ms
01	20ms
10	10ms
11	CH2 rising (90% is reached)

CH4_DLY : Setting the rising delay time of CH4 output.

Table 8.9 CH4_DLY

CH4_DLY	Delay time
0	20ms
1	10ms

CH1_FDLY : Setting the falling delay time of CH1 output.

Table 8.10 CH1_FDLY

CH1_FDLY	Delay time
0	4ms
1	2ms

FSQ_SEL : Setting the rising order of CH3 and CH4 output.

Table 8.11 FSQ_SEL

FSQ_SEL	Falling order
0	CH3⇒CH4
1	CH4⇒CH3

8.3.4 Setting VOUT1 (03h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03h	Reserved		CH1_VSET[5:0]					
Initial value	0	0	0	1	0	1	0	1

CH1_VSET [5:0] : Setting VOUT1.

Table 8.12 CH1_VSET

CH1_VSET [5:0]	VOUT1[V]	CH1_VSET [5:0]	VOUT1[V]	CH1_VSET [5:0]	VOUT1[V]	CH1_VSET [5:0]	VOUT1[V]
000000	5.0	010000	8.2	100000	11.4	110000	14.6
000001	5.2	010001	8.4	100001	11.6	110001	14.8
000010	5.4	010010	8.6	100010	11.8	110010	15.0
000011	5.6	010011	8.8	100011	12.0	110011	Setting forbidden
000100	5.8	010100	9.0	100100	12.2	110100	
000101	6.0	010101	9.2	100101	12.4	110101	
000110	6.2	010110	9.4	100110	12.6	110110	
000111	6.4	010111	9.6	100111	12.8	110111	
001000	6.6	011000	9.8	101000	13.0	111000	
001001	6.8	011001	10.0	101001	13.2	111001	
001010	7.0	011010	10.2	101010	13.4	111010	
001011	7.2	011011	10.4	101011	13.6	111011	
001100	7.4	011100	10.6	101100	13.8	111100	
001101	7.6	011101	10.8	101101	14.0	111101	
001110	7.8	011110	11.0	101110	14.2	111110	
001111	8.0	011111	11.2	101111	14.4	111111	

Note: bit7,bit6: Fix to ”0”.

Note: To change the voltage for debug, set ENABLE=”L”.

8.3.5 Setting VOUT2 (04h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04h	-	Reserved	-	CH2_VSET[4:0]				
Initial value	0	0	0	0	0	0	1	1

CH2_VSET [4:0] : Setting VOUT2. (Note1)

Table 8.13 CH2_VSET

CH2_VSET[4:0]	VOUT2[V]	CH2_VSET[4:0]	VOUT2[V]
00000	3.0	10000	4.6
00001	3.1	10001	4.7
00010	3.2	10010	4.8
00011	3.3	10011	4.9
00100	3.4	10100	5.0
00101	3.5	10101	Setting forbidden
00110	3.6	10110	
00111	3.7	10111	
01000	3.8	11000	
01001	3.9	11001	
01010	4.0	11010	
01011	4.1	11011	
01100	4.2	11100	
01101	4.3	11101	
01110	4.4	11110	
01111	4.5	11111	

Note 1: Setting range of VOUT2: VOUT2 < V_{IN} × 0.75
(It is the reference value because it depends on the conditions and external parts. Please confirm the operation in the actual operation conditions.)

Note: bit6: Fix to ”0”.

Note: To change the voltage for debug, set ENABLE=”L”.

8.3.6 Setting VOUT3 (05h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05h	-	Reserved	CH3_VSET[5:0]					
Initial value	0	0	0	1	1	1	1	0

CH3_VSET [5:0] : Setting VOUT3. (Note1)

Table 8.14 CH3_VSET

CH3_VSET [5:0]	VOUT3[V]	CH3_VSET [5:0]	VOUT3[V]	CH3_VSET [5:0]	VOUT3[V]	CH3_VSET [5:0]	VOUT3[V]
000000	Setting forbidden	010000	15.2	100000	18.4	110000	21.6
000001		010001	15.4	100001	18.6	110001	21.8
000010		010010	15.6	100010	18.8	110010	22.0
000011		010011	15.8	100011	19.0	110011	Setting forbidden
000100		010100	16.0	100100	19.2	110100	
000101		010101	16.2	100101	19.4	110101	
000110		010110	16.4	100110	19.6	110110	
000111		010111	16.6	100111	19.8	110111	
001000		011000	16.8	101000	20.0	111000	
001001		011001	17.0	101001	20.2	111001	
001010	14.0	011010	17.2	101010	20.4	111010	
001011	14.2	011011	17.4	101011	20.6	111011	
001100	14.4	011100	17.6	101100	20.8	111100	
001101	14.6	011101	17.8	101101	21.0	111101	
001110	14.8	011110	18.0	101110	21.2	111110	
001111	15.0	011111	18.2	101111	21.4	111111	

Note 1: Setting range of VOUT3: VOUT3 < VOUT1 × 2- 0.97V
or VOUT3 < VOUT1 × 3 - 1.33V
or VOUT3 < VOUT1 × 4 - 2.82V
(It is the reference value because it depends on the conditions and external parts. Please confirm the operation in the actual operation conditions.)

Note: bit6: Fix to ”0”.

Note: To change the voltage for debug, set ENABLE=”L”.

8.3.7 Setting VOUT4 (06h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06h	-	Reserved	CH4_VSET[5:0]					
Initial value	0	0	0	0	0	1	0	1

CH4_VSET [5:0] : Setting VOUT4. (Note1)

Table 8.15 CH4_VSET

CH4_VSET [5:0]	VOUT4[V]	CH4_VSET [5:0]	VOUT4[V]	CH4_VSET [5:0]	VOUT4[V]	CH4_VSET [5:0]	VOUT4[V]
000000	-5.0	010000	-8.2	100000	-11.4	110000	-14.6
000001	-5.2	010001	-8.4	100001	-11.6	110001	-14.8
000010	-5.4	010010	-8.6	100010	-11.8	110010	-15.0
000011	-5.6	010011	-8.8	100011	-12.0	110011	Setting forbidden
000100	-5.8	010100	-9.0	100100	-12.2	110100	
000101	-6.0	010101	-9.2	100101	-12.4	110101	
000110	-6.2	010110	-9.4	100110	-12.6	110110	
000111	-6.4	010111	-9.6	100111	-12.8	110111	
001000	-6.6	011000	-9.8	101000	-13.0	111000	
001001	-6.8	011001	-10.0	101001	-13.2	111001	
001010	-7.0	011010	-10.2	101010	-13.4	111010	
001011	-7.2	011011	-10.4	101011	-13.6	111011	
001100	-7.4	011100	-10.6	101100	-13.8	111100	
001101	-7.6	011101	-10.8	101101	-14.0	111101	
001110	-7.8	011110	-11.0	101110	-14.2	111110	
001111	-8.0	011111	-11.2	101111	-14.4	111111	

Note 1: Setting range of VOUT4: VOUT4 > VOUT1×(-3) + 5.97V
(It is the reference value because it depends on the conditions and external parts. Please confirm the operation in the actual operation conditions.)

Note: bit6: Fix to ”0”.

Note: To change the voltage for debug, set ENABLE=”L”.

8.3.8 Status read (07h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	-	TSD	UVLO	OVP	SCP_CH1	SCP_CH2	SCP_CH3	SCP_CH4
Initial value	-	-	-	-	-	-	-	-

Bit6-1: Outputting detection result of each protection.

Table 8.16 Status read

Bit	Register	Function	Data=”0”	Data=”1”
6	TSD	Read out detection result of TSD (Thermal shutdown) error.	Non detection	Detection
5	UVLO	Read out detection result of UVLO (Under voltage lockout) error.	Non detection	Detection
4	OVP	Read out detection result of OVP (Over voltage protection) error.	Non detection	Detection
3	SCP_CH1	Read out detection result of SCP (Short circuit protection) error of CH1.	Non detection	Detection
2	SCP_CH2	Read out detection result of SCP (Short circuit protection) error of CH2.	Non detection	Detection
1	SCP_CH3	Read out detection result of SCP (Short circuit protection) error of CH3.	Non detection	Detection
0	SCP_CH4	Read out detection result of SCP (Short circuit protection) error of CH4.	Non detection	Detection

8.4 Power supply sequence

8.4.1 Power ON sequence

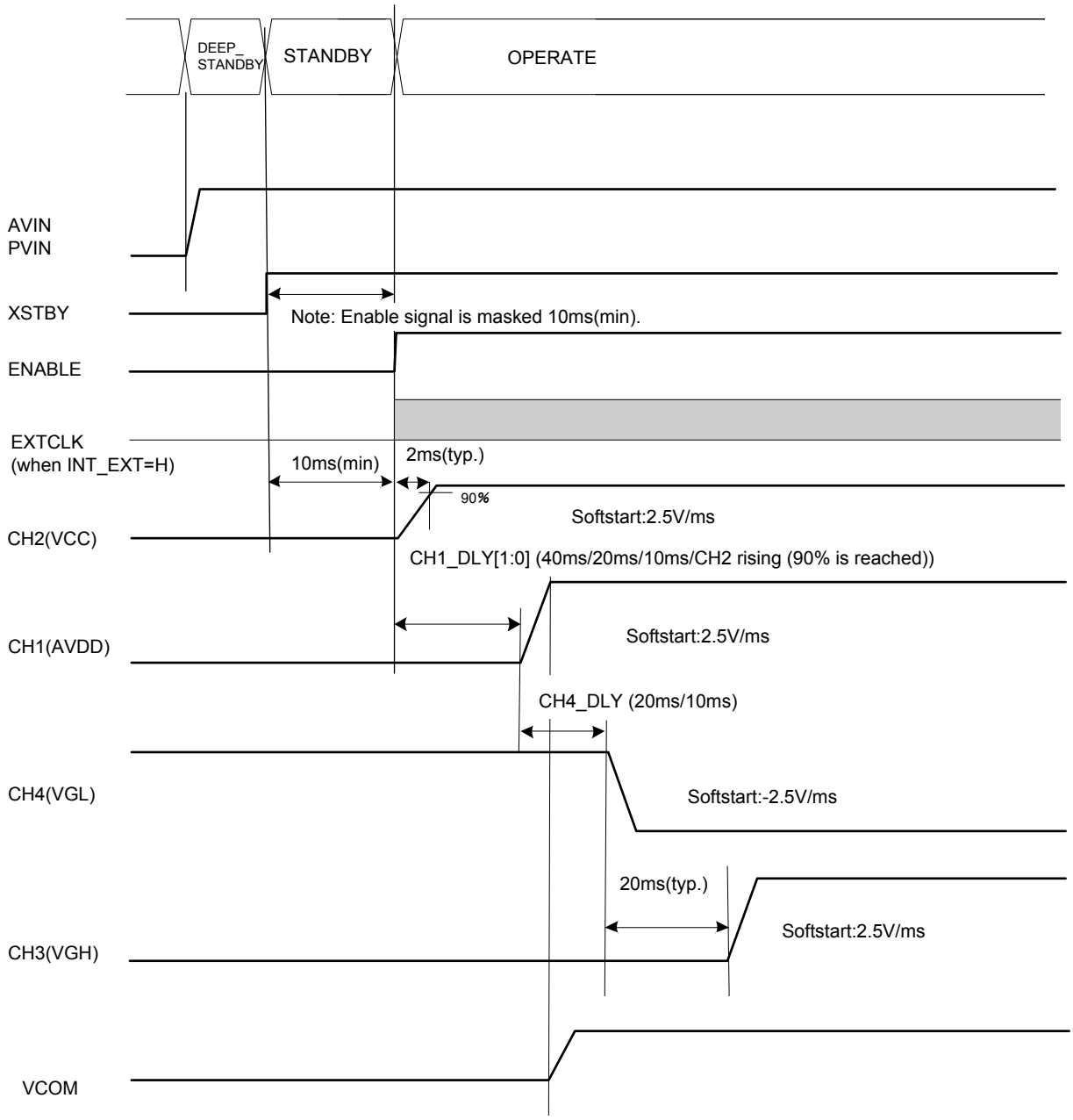


Figure 8.4 Power ON sequence

8.4.2 Power OFF sequence

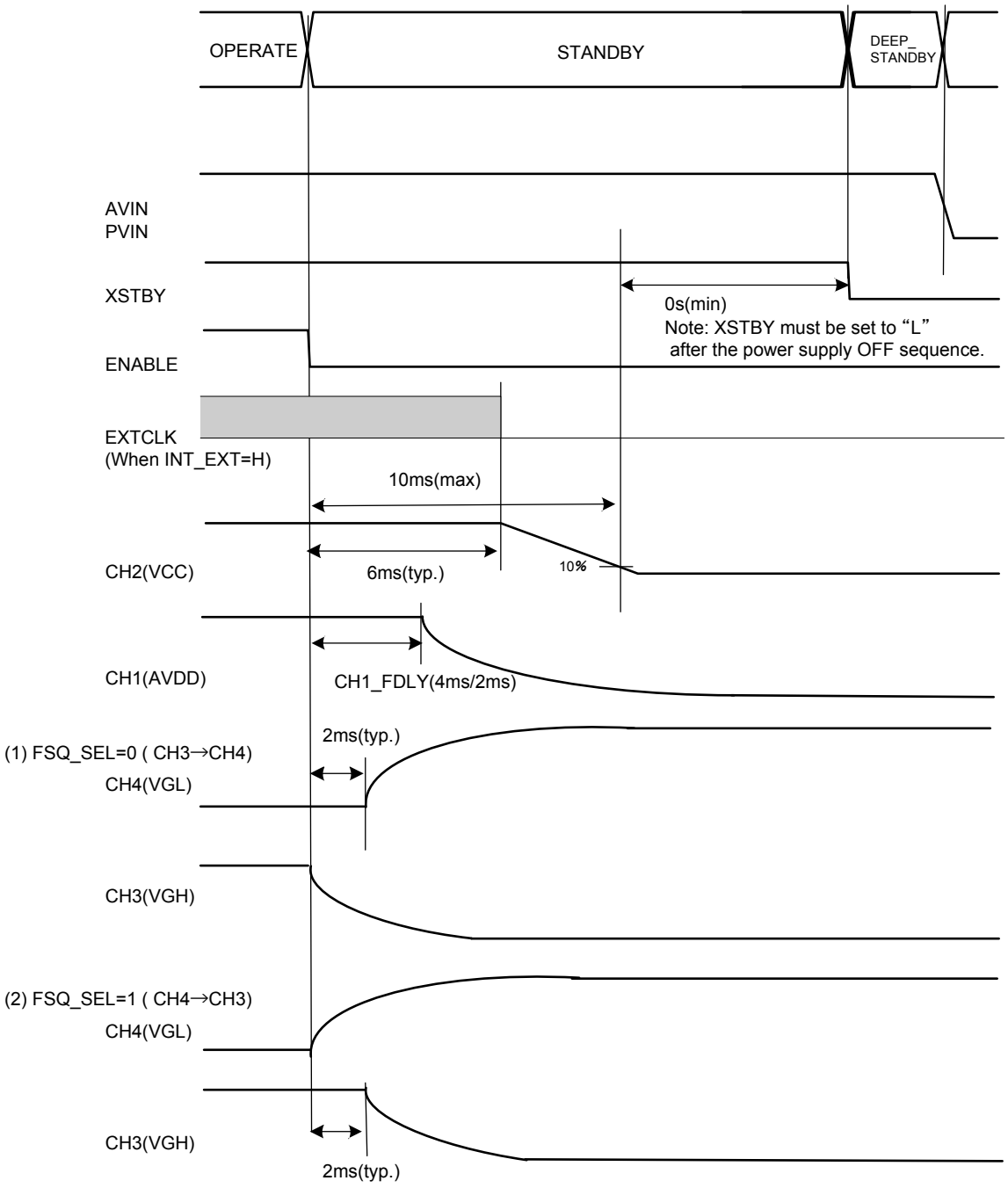


Figure 8.5 Power OFF sequence

8.5 Protection functions

8.5.1 Under voltage lockout (UVLO) function

Under voltage lockout (UVLO) function reduces the malfunction caused by low voltage of AVIN terminal. UVLO function works when the voltage of AVIN terminal is 4.0V (typ.) or less. When the voltage does not exceed 4.2 V (typ.) for 5μs (typ.), the operation moves to PROTECTED state and set 06h [5] (UVLO) to "1".

8.5.2 Over current detection (OCP) function

Over current detection (OCP) function prevents the IC from being destructed by over current of DC-DC convertor of CH1 or CH2. OCP function works when the current flowing in high-side MOSFET of the DC-DC convertor reaches the specified value. OCP detection current is as follows; driver current of CH1 > 0.8A (typ.), driver current of CH2 > 1A (typ.) When OCP is detected, high-side MOSFET of DC-DC convertor is turned off and low-side MOSFET is turned on. OCP function works by the switching cycle. So, OCP is released automatically at the next switching cycle and the normal operation recovers.

8.5.3 Short circuit protection (SCP) function

SCP function prevents the IC from being destructed by over current and over heat caused by short circuit of each power channel. SCP function works when the voltage of the feedback terminal of each power channel falls to less than the threshold voltage (80% of configured output voltage). When it does not exceed the threshold voltage within 1ms (typ.), the operation moves to PROTECTED state and sets 06h [3:0] (SCP_CHx) to "1".

8.5.4 Thermal shutdown (TSD) function

Thermal shutdown (TSD) function prevents the IC from being destructed by internal over heat. When internal temperature exceeds 150°C (typ.), TSD function works. In the case the temperature does not fall to 130°C (typ.) or less within 1ms (typ.), the operation moves to PROTECTED state and set 06h[6](TSD) to "1".

8.5.5 Input over voltage protection (IOVP)

Input over voltage protection prevents the IC from being destructed by over voltage of AVIN terminal. When the voltage of AVIN terminal becomes 22V (typ.) or more, switching operations of the power supplies of CH1 and CH2 are turned off. When the voltage of AVIN terminal falls below 17.0V (min), the operation recovers automatically to the OPERATE state.

8.5.6 Output over voltage protection (OVP)

Output over voltage protection prevents the IC from being destructed by over voltage of DC-DC convertor of CH1. In case the voltage of VOUT1 terminal exceeds the threshold value (120% of configured output voltage), OVP works. And in case the voltage does not fall below the threshold value within 5μs (typ.), the operation moves to PROTECTED state and 06h [4] (OVP) is set to "1".

8.6 Interface

The TC7735FTG sets each function by I²C interface. It supports the slave operation and the fast mode (400kHz) of I²C standard. Single write, continuous write, single read, and continuous read are possible. The slave address of the TC7735FTG is fixed to 0b1001101. As for descriptions of writing and reading, refer to Figure8.6 to Figure8.9.

Table 8.17 Description of I^2C interface

Symbol	Description
S	Start condition
Sr	Repeat start condition
Slave Address	Slave address (7bit)
R	Read mode (R/W=1)
W	Write mode (R/W=0)
A	Acknowledge signal (output L level)
NA	Non- acknowledge signal (output HiZ)
P	Stop condition

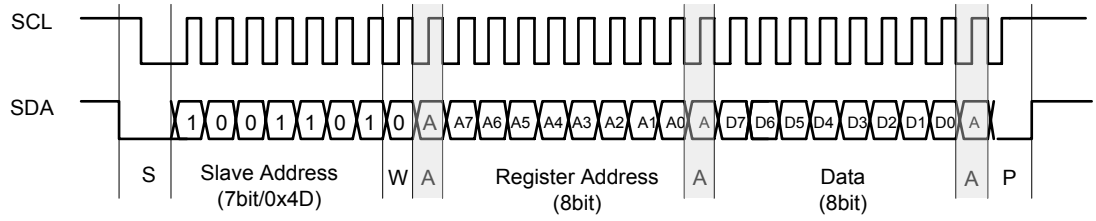


Figure8.6 Single write mode

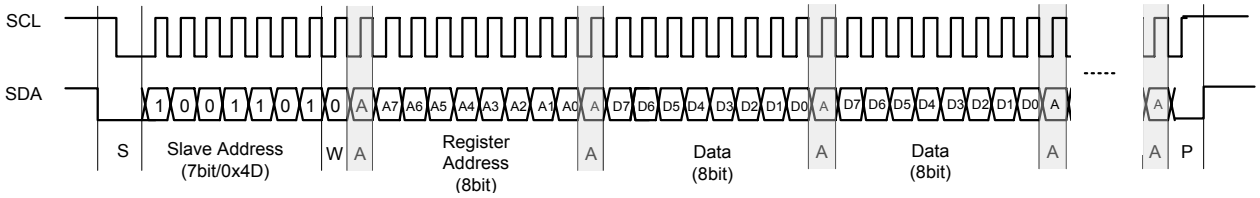


Figure8.7 Continuous write mode

Note: In continuous write mode, data is not written to the register 07h and the signal of ACK is returned.

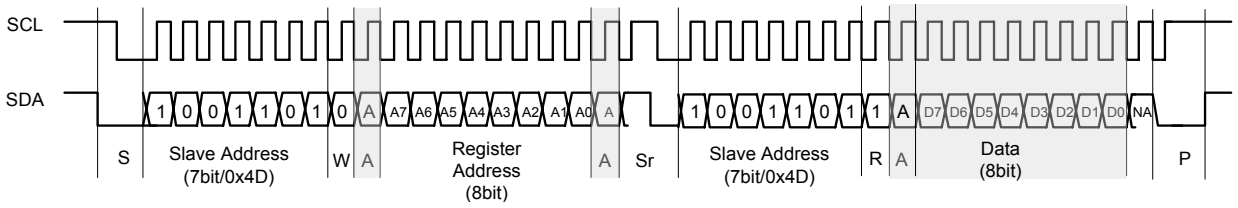


Figure8.8 Single read mode

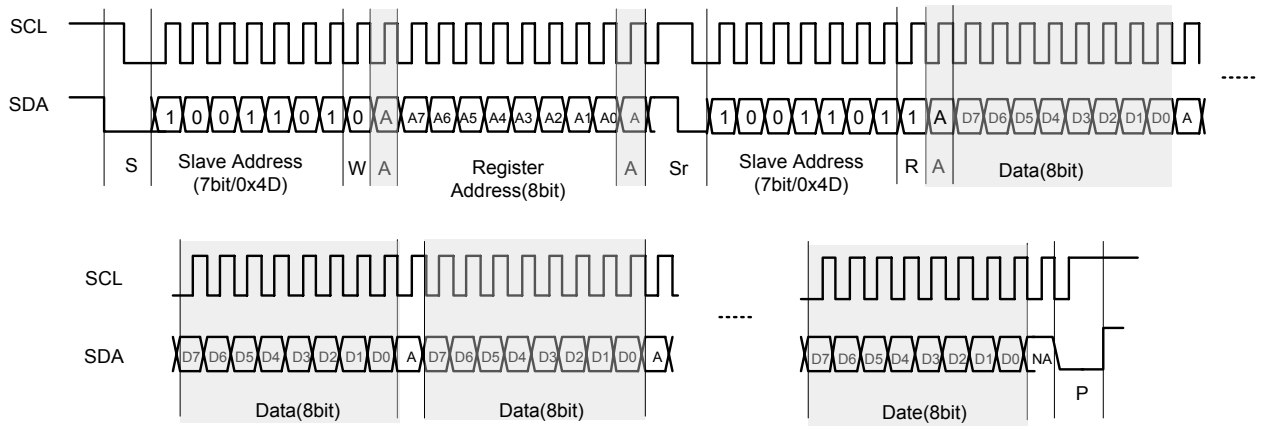


Figure8.9 Continuous read mode

Note: When ACK is set to "1", configure MCU to stop condition.

Note: When stop condition is recognized, the TC7735FTG opens SDA and waits for start condition. In case it is under accessed in this time, transfer data is canceled and the clock count is initialized.

Note: When the command is interrupted on the way of operation, the command before it is interrupted is reflected. The interrupted command is not executed. To reflect the command, configure the command again.

9. Absolute maximum ratings (Ta=25°C)

Table 9.1 Absolute maximum rating

Characteristic	Symbol	Rating	Unit
Supply voltage	AVIN,PVIN	− 0.3 to 18	V
		40 (1s)	
Supply voltage	SGND, PGND	+ 0.3	V
Terminal voltage (Note 1)	V_{IN1},	− 0.3 to 40.0	V
Terminal voltage (Note 2)	V_{IN2}	− 0.3 to 30.0	V
Terminal voltage (Note 3)	V_{IN3}	− 0.3 to 18.0	V
Terminal voltage (Note 4)	V_{IN4},	− 18.0 to 0.3	V
Terminal voltage (Note 5)	V_{IN5},	− 0.3 to 7.8	V
Terminal voltage (Note 6)	V_{IN6},	− 0.3 to 5.5	V
Terminal voltage (Note 7)	V_{IN7}	− 0.3 to 8.0	V
Power dissipation	PD	4.2 (Note 8)	W
Operating temperature	Topr	− 40 to 85	°C
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	− 55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant. If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions. Before using, creating and/or producing design, refer to and comply with the precautions and conditions set forth in this document.

Note 1: LX1I and LX2 terminals

Note 2: VOUT3, CP1P, CP1O, CP2N, and CP2P terminals

Note 3: VOUT1, LX1O, DRVN, CP1N, and VCOMP terminals

Note 4: VOUT4 terminal

Note 5: VCOMN and VCOMO terminal

Note 6: XSTBY, SDA, SCL, ENABLE, EXTCLK, INT_EXT, PG, TEST, VDD42, VOUT2 and VREF terminals

Note 7: VPP terminal

Note 8: Thermal simulation value. Conditions: Still air, standard four-layer JEDEC board

10. Electrical characteristics

10.1 DC characteristics (1)

10.1.1 Common characteristics

Table 10.1 DC characteristics (1)

(Unless otherwise specified, V_{IN}=14.0V, PGND =SGND = 0V, and Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Operation voltage	V_{IN}	Ta = −40 to 85°C	4.5	—	16	V	AVIN PVIN
IOVP detection voltage	V_{IOVP}		21	22	23	V	AVIN
IOVP hysteresis	$V_{IOVP\ Hys}$		—	5	—	V	AVIN
UVLO operation voltage	V_{UVLO}	AVIN falling	3.8	4.0	4.2	V	AVIN
UVLO hysteresis	$V_{UVLO\ Hys}$		—	0.2	—	V	AVIN
VDD42 voltage	V_{REG42}		—	4.2	—	V	VDD42
VREF voltage	V_{REF}		—	1.5	—	V	VREF
Consumption current	IQ1	XSTBY="L" (DEEP_STANDBY)	—	—	12	μA	AVIN PVIN
	ICC1	XSTBY="H", ENABLE="L" (STANDBY, PROTECTED)	—	—	4.5	mA	AVIN PVIN
	ICC2	ENABLE="H"(OPERATE) Non Switching	—	—	10	mA	AVIN PVIN
Oscillator frequency	f_{OSCINT}		850	—	1150	kHz	
Input range of external clock	f_{OSCEX}		400	—	1,200	kHz	EXTCLK
External clock DUTY	f_{OSC_duty}		40	—	60	%	EXTCLK
Input voltage	VIH1		1.8	—	—	V	ENABLE XSTBY EXTCLK INT_EXT SDA, SCL
	VIL1		—	—	0.5		
TSD detection temperature	T_{TSD}	Temp. rising	—	150	—	°C	
	T_{TSDHys}	Hysteresis	—	20	—		
Output voltage	VOL	I_{SINK}=4mA	GND	—	0.5	V	PG

10.1.2 CH1 automatic buck/boost DC-DC convertor

Table 10.2 DC characteristics (2)

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, and Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Output voltage	V_{O1}	Standard setting product (Note)	—	9.2	—	V	VOUT1
Accuracy of output voltage	ΔV_{O1}		−1.5	—	1.5	%	VOUT1
Peak current of OCP detection	I_{OCP1}	In Buck mode	—	0.8	—	A	
SCP detection voltage	V_{SCP1}		—	V_{O1} × 0.8	—	V	VOUT1
Through rate of output voltage	V_{SR1}	In startup, In using internal clocks	—	2.5	—	V/ms	VOUT1
Maximum of drive capability	$I_{OUT1max}$		100	—	—	mA	VOUT1

Note: The output voltage can be changed by the eFuse writing.

10.1.3 CH2 buck DC-DC convertor

Table 10.3 DC characteristics (3)

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Output voltage	V_{O2}	Standard setting product (Note)	—	3.3	—	V	VOUT2
Accuracy of output voltage	ΔV_{O2}		−2.0	—	2.0	%	VOUT2
Peak current of OCP detection	I_{OCP2}		—	1.0	—	A	
SCP detection voltage	V_{SCP2}		—	V_{O2} × 0.8	—	V	VOUT2
Through rate of output voltage	V_{SR2}	In startup, In using internal clocks	—	2.5	—	V/ms	
Maximum of drive capability	$I_{OUT2max}$		500	—	—	mA	

Note: The output voltage can be changed by the eFuse writing.

10.1.4 CH3 positive charge pump

Table 10.4 DC characteristics (4)

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, and Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Output voltage	V_{O3}	Standard setting product (Note)	—	18.0	—	V	VOUT3
Accuracy of output voltage	ΔV_{O3}		−2.0	—	2.0	%	VOUT3
SCP detection voltage	V_{SCP3}		—	V_{O3} × 0.8	—	V	VOUT3
Switching frequency	f_{SW3}	In using external clocks (Setting range of frequency dividing ratio) Recommended value:125kHz	100	—	200	kHz	
Through rate of output voltage	V_{SR3}	In using internal clocks	—	2.5	—	V/ms	VOUT3
Maximum of drive capability	$I_{OUT3max}$		2	—	—	mA	

Note: The output voltage can be changed by the eFuse writing.

10.1.5 CH4 negative charge pump

Table 10.5 DC characteristics (5)

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Output voltage	V_{O4}	Standard setting product (Note)	—	−6.0	—	V	VOUT4
Accuracy of output voltage	ΔV_{O4}		−5.0	—	5.0	%	VOUT4
SCP detection voltage	V_{SCP4}		—	V_{O3} × 0.8	—	V	VOUT4
Switching frequency	f_{SW4}	In using external clocks (Setting range of frequency dividing ratio) Recommended value:125kHz	100	—	200	kHz	
Through rate of output voltage	V_{SR4}	In using internal clocks	—	−2.5	—	V/ms	VOUT4
Maximum of drive capability	$I_{OUT4max}$		2	—	—	mA	

Note: The output voltage can be changed by the eFuse writing.

10.1.6 VCOM amplifier

Table 10.6 DC characteristics (6)

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Pin
Output voltage range	V_{VCOMO}	0.5 ≥ VCOMP ≥ 7.5V VO1 ≥ VVCOMO+0.6V	0.5	—	7.5	V	VCOMO
Off set between terminals	$V_{p\text{-}pOS}$	In following voltage (short circuit VCOMN and VCOMO terminals)	−25	—	25	mV	VCOMO
Maximum of drive capability	I_{COMmax}	,	2	—	—	mA	

10.2 AC characteristics

10.2.1 I^2C bus

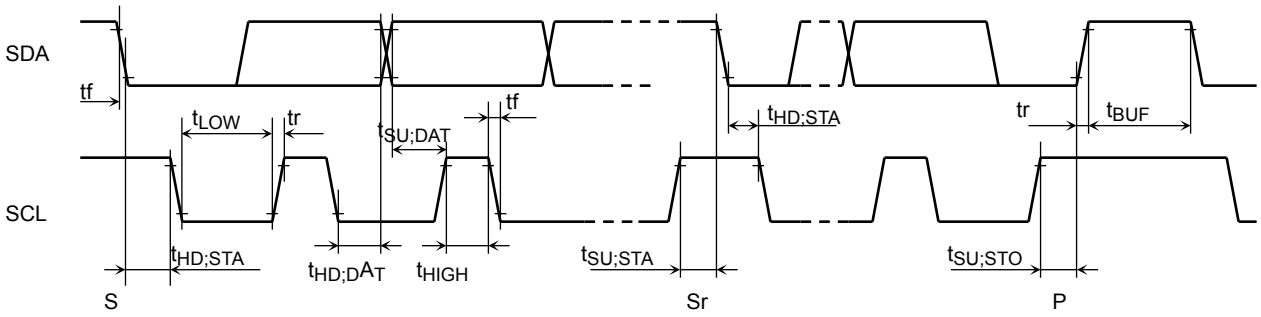
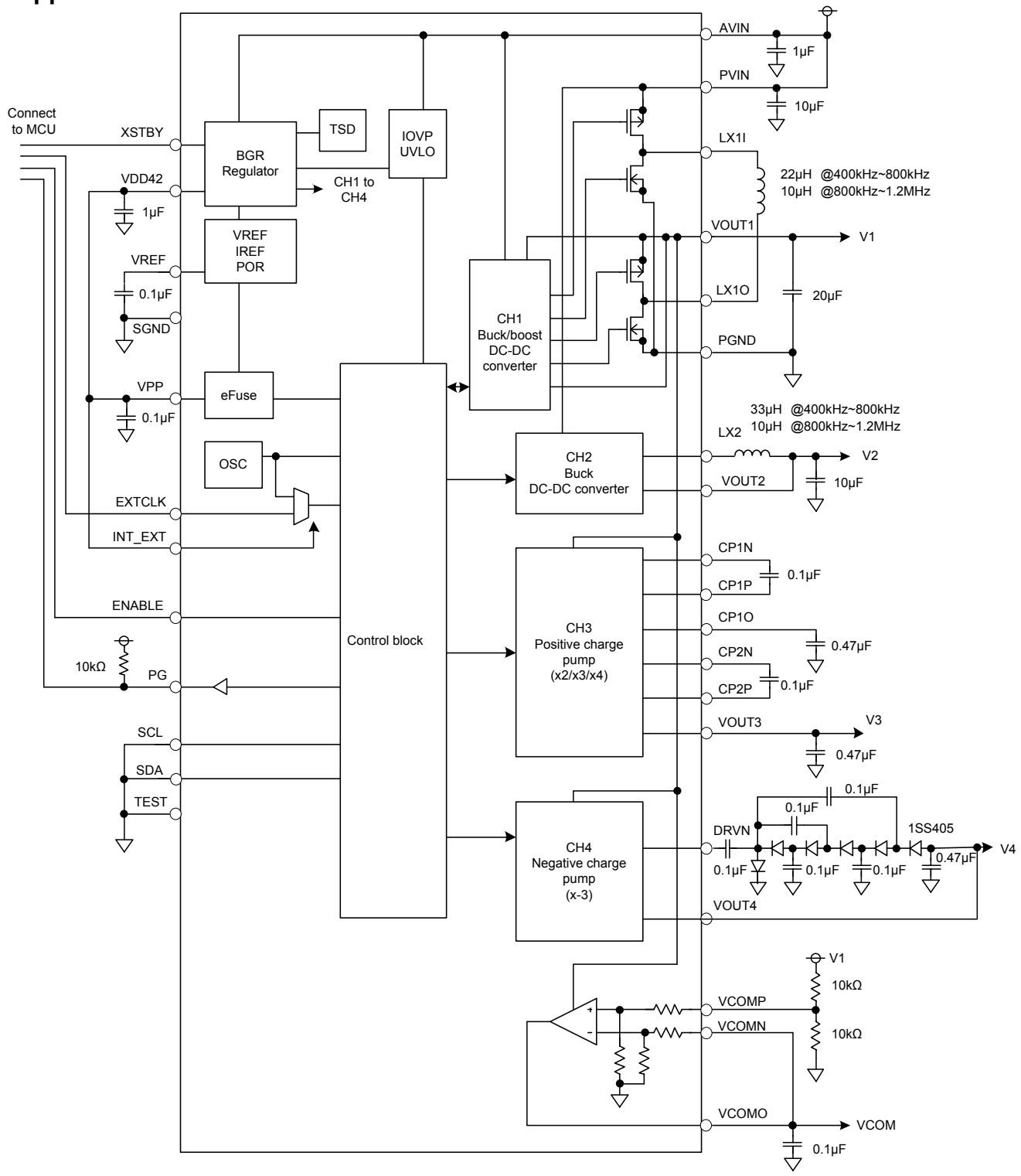


Table 10.7 AC characteristics

(Unless otherwise specified, V_{IN} =14.0V, PGND =SGND = 0V, and Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Operation clock frequency	f_{SCL}		—	—	400	kHz
Hold time of repeat start condition	$t_{HD:STA}$		0.6	—	—	μs
Setup time of repeat start condition	$t_{SU:STA}$		0.6	—	—	μs
Data hold time	$t_{HD;DAT}$		0	—	0.9	μs
Data setup time	$t_{SU;DAT}$		100	—	—	ns
Low term of SCL signal	t_{LOW}		1.3	—	—	μs
High term of SCL signal	t_{HIGH}		0.6	—	—	μs

11. Application circuit



Note: When CH3TIM_SEL [1:0] is set to ”10”(×2), terminals of CP1P, CP1N and CP1O should be open.

Note: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

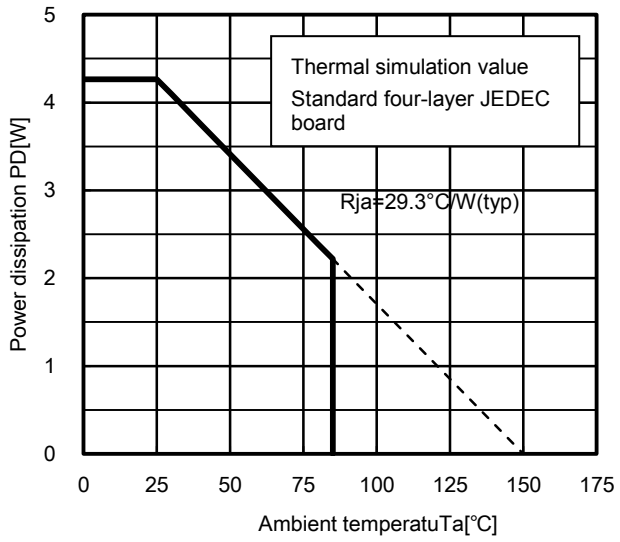
Usage Considerations

A large current might abruptly flow through the IC in case of a short-circuit across its outputs, a short-circuit to power supply or a short-circuit to ground, leading to a damage of the IC. Also, the IC or peripheral parts may be permanently damaged or emit smoke or fire resulting in injury especially if a power supply pin (PVIN,AVIN) or an output pin is short-circuited to adjacent or any other pins. These possibilities should be fully considered in the design of the output, PVIN, AVIN, and ground lines.

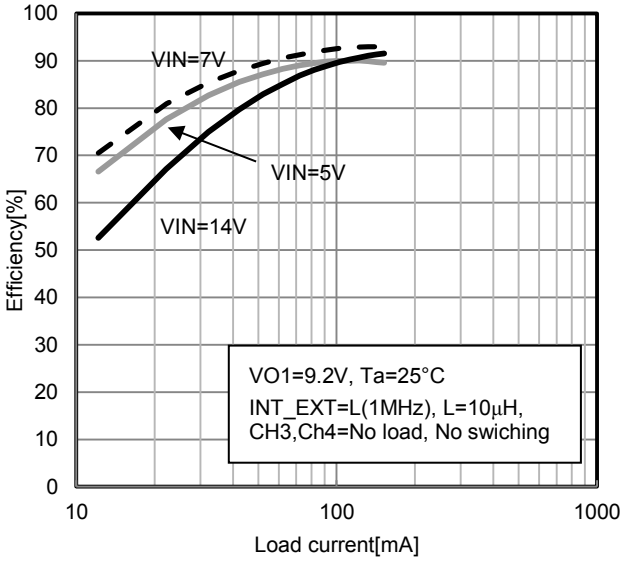
A fuse should be connected to the power supply line.

12. Characteristics (Reference data)

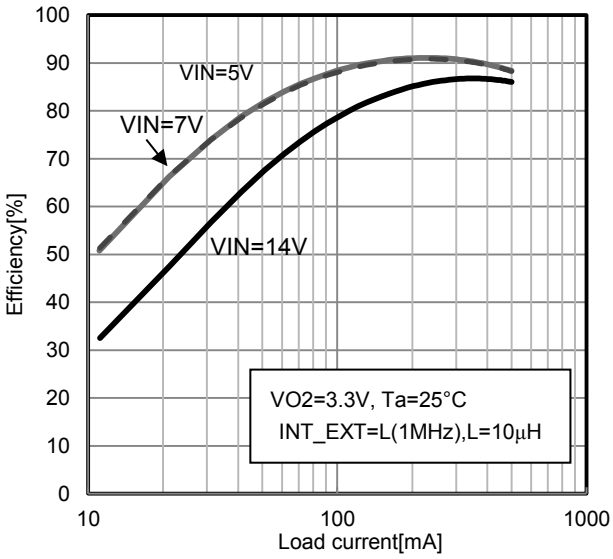
PD-Ta



CH1 Efficiency

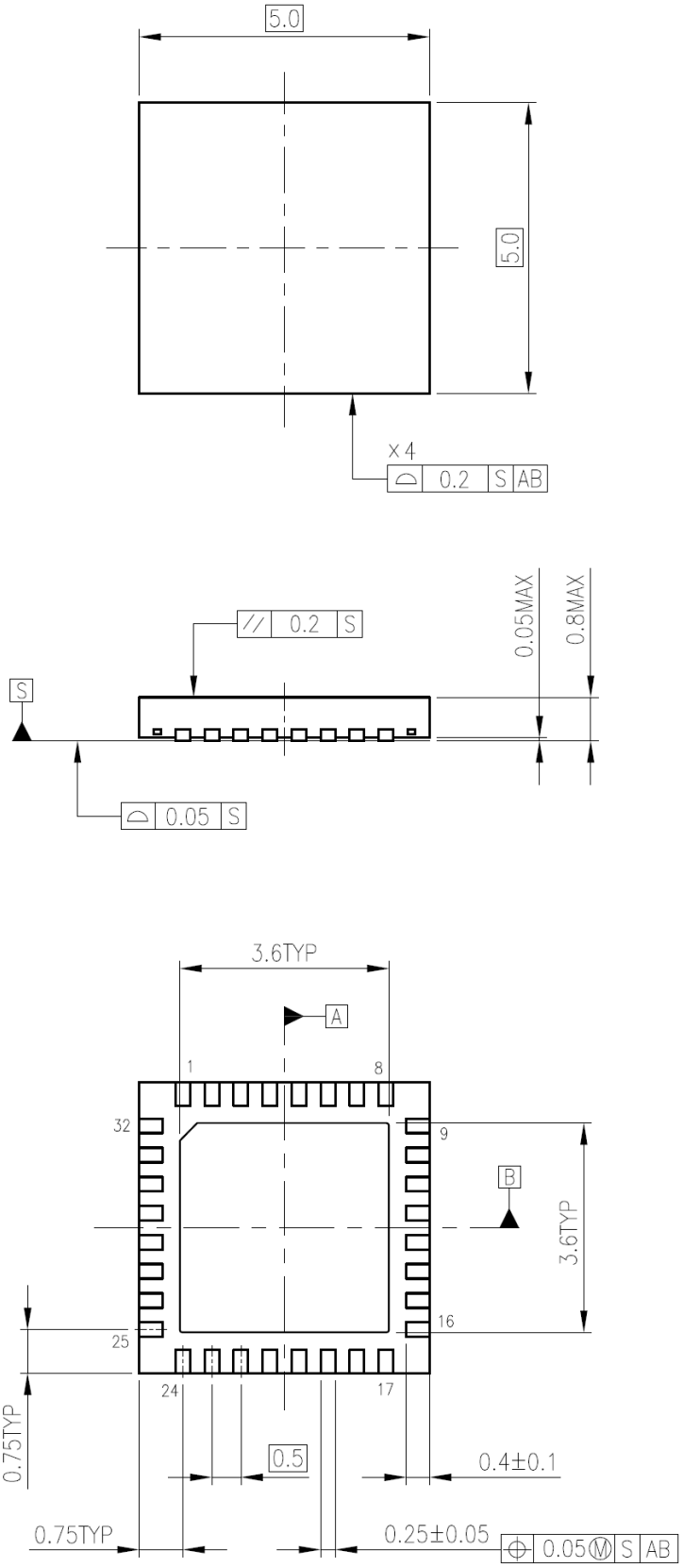


CH2 Efficiency



13. Package dimensions

P-WQFN32-0505-0.50-001 Unit: mm



Weight: 0.06 g (Typ.)

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