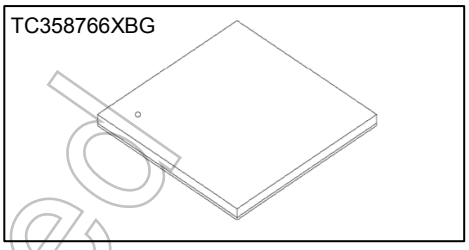
CMOS Digital Integrated Circuit Silicon Monolithic

TC358766XBG

Mobile Peripheral Devices



P-VFBGA120-0606-0.50AZ
Weight: 62mg (Typ.)

Overview

The DSI/DPI to DisplayPort™ converter TC358766XBG is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI® DSI or DPI link to drive DisplayPort™ display panels.

Features

- Translates MIPI® DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, upto1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration: From DSI link, SPI or I²C interface (only one of the SPI and I²C interfaces can be active at any time).
- Internally generated H/VSync in DSI mode can be muxed out to Host.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP o/p testing without any video (DSI/DPI) i/p.
- Debug/Test Port: I²C Slave

- **DSI Receiver:** Supports one DSI Interface between TC358766XBG and Host.
  - ✧ MIPI® DSI: v1.01 / MIPI® D-PHY: v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per Hsync period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats:
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support: 16-bit YCbCr 422

      Interlaced video mode is not supported.

- **DPI Receiver:** Supports one DPI Interface between TC358766XBG and Host.
  - ✧ Up to 16 / 18 / 24 bit parallel data interface.
  - ✧ Maximum speed at 154 MPs (MPixel per sec).
  - ✧ Video input data formats: RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
  - ✧ Shutdown support (can be used in non-DPI mode also).

- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC358766XBG to display panels.
  - ✧ High speed serial bridge chip using VESA DisplayPort™ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications
  - ✧ Supports up to two (2) single-lane ports for connection to two DisplayPort™ panels.
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2V
  - ✧ Support of pre-emphasis levels of 0, 3.5dB and 6dB.
  - ✧ Supports Audio related Secondary Data Packets
  - ✧ AUX channel supported at 1 Mbps.
  - ✧ HPD support through GPIO[1:0] based interrupts
  - ✧ Enhanced mode supported for HDCP content protection.

    Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1. (on DisplayPort™0 in case two port configuration is used)
  - ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
    - Start Link training in response to HPD & read final Link training status
    - Configure DP link for actual video streaming & start video streaming

- ✧ Link Policy maker is assumed shared between the Host and TC358766XBG chip.
  - In auto_correction = 0 mode, control link training
  - Initiate Display device capabilities read and configure TC358766XBG accordingly.
- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with up to 30 kHz modulation to reduce EMI.
- ✧ Toshiba Magic Square algorithm – RGB666 18b produces RGB888 24b like quality (with up to 16-million colors).
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

● **RGB Parallel Output Interface:**
- ✧ RGB888 output mode (DisplayPort™ disabled) with only DSI input supported in this mode
- ✧ PCLK max = 100 MHz
- ✧ Polarity control for PCLK, VSYNC, HSYNC & DE.

● **I²C Interface:**
- ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
- ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).

● **SPI Interface:**
- ✧ SPI slave interface for chip register set access enabled using a boot-strap option.
- ✧ SPI interface support for up to 30 MHz operation.

● **GPIO Interface:**
- ✧ 2 bits of GPIO (shared with other digital logic).
- ✧ Direction controllable by Host I²C accesses.

● **Clock Source:**
- ✧ DisplayPort™ clock source is from an external clock input or clock from DSI interface (13, 26, 19.2 or 38.4 MHz) – generates all internal & output clocks to interfacing display devices.
- ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.

● Clock and power management support to achieve low power states.

● **Possible modes of Operation:** Supports six (6) modes of operation:
- ✧ MODE S21: TC358766XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DSI Host.
- ✧ MODE S22: TC358766XBG uses DisplayPort™ Tx port as two independent 1-lane DisplayPort™ links to interface to two (2) DisplayPort™ display devices. Video stream source is from MIPI® DSI Host. Same video stream can be displayed on two display devices.
- ✧ MODE P21: TC358766XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DPI Host.
- ✧ MODE P22: TC358766XBG uses DisplayPort™ Tx port as two independent 1-lane DisplayPort™ links to interface to two (2) DisplayPort™ display devices. Video stream source is from MIPI® DPI Host. Same video stream is displayed on two display devices.
- ✧ MODE SP22: TC358766XBG uses DisplayPort™ Tx as two independent DisplayPort™ output links (each single lane). TC358766XBG routes the DSI input to one DisplayPort™ Tx link and routes the DPI input to the second DisplayPort™ Tx link.
- ✧ MODE S2P: TC358766XBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI® DSI Host.

● **Power supply inputs**
- ✧ Core and MIPI® D-PHY: 1.2V ±0.06V
- ✧ Digital I/O: 1.8V ±0.09V
- ✧ DisplayPort™: 1.8V ±0.09V
- ✧ DisplayPort™: 1.2V ±0.06V

● **Power Consumptions (based on estimations)**
- ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
  - DSI Rx: 0.01 mW
  - DP PHY: 2.34 mW
  - PLL9: 0.01 mW
  - Core: 0.96 mW
  - Rest: 0.01 mW
- ✧ Normal operation (1920 x 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
  - DSI Rx: 21.79 mW
  - DP PHY: 142.70 mW
  - PLL9: 2.42 mW
  - Core: 87.64 mW
  - IOs: 1.68 mW

Table of contents

List of Figures

List of Tables

- MIPI is a trademark of MIPI Alliance, Inc.
- DisplayPort is trademark owned by the Video Electronics Standards Association (VESA®) in the United States and other countries.
- All other company names, product names, and service names may be trademarks of their respective companies.

NOTICE OF DISCLAIMER

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI® hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI® Alliance. MIPI®, MIPI® Alliance and the dotted rainbow arch and all related trademarks, trade names, and other intellectual property are the exclusive property of MIPI® Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI® BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI®: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI®. MIPI® does not make any search or investigation for IPR, nor does MIPI® require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI® Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane
Piscataway, NJ 08854
Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

REFERENCES

1. MIPI® D-PHY, “MIPI® Alliance Specification for D-PHY Version 1.00.00 14-May-2009"
2. MIPI® Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. MIPI® DPI, “MIPI® Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00 – 15 September 2005”
4. VESA DisplayPort™ Standard (Version 1, Revision 1A January 11, 2008)
5. VESA Embedded DisplayPort™ (eDP) Standard (Version 1.1 October 23, 2009)
6. Digital Content Protection LLC, HDCP (Version 1.3 with DisplayPort™ amendment Revision 1.1, Jan. 15 2010)
7. I²C bus specification, version 2.1, January 2000, Philips Semiconductor
8. Digital audio interface – Part 1: General “CEI IEC 60958-1, First edition 1999-12”
9. Digital audio interface – Part 3: Consumer applications “IEC 60958-3, Second edition 2003-01”
10. Draft CEA-861-C, A DTV Profile for Uncompressed High Speed Digital Interfaces (Doc. Number: CEA-861rCv9.pdf (PNXXX)) Date: 05/04/2005
11. DisplayPort™ PHY DFT Strategy Specification Rev 1.3

1. Overview

The DSI/DPI to DisplayPort™ converter (TC358766XBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI® DSI or DPI link to drive DisplayPort™ display panels. TC358766XBG provides a low power bridge solution to efficiently translate MIPI® DSI or DPI transfers to DisplayPort™ transfers. As the DisplayPort™ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC358766XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort™ interface and also to connect to existing panels over longer distance using DisplayPort™ adaptors at far-end. TC358766XBG can interface to up to two independent devices.

The chip can be configured through the DSI link by sending write/read register commands through DSI Generic Long Write packets. It can also be configured through the I^2C Slave interface or the SPI interface. The selection between I^2C or SPI slave interface is done using a boot-strap option.

The DSI-RX receiver supports from 1 to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in continuous video streaming mode. Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only a small video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The DPI-Rx receiver supports 16, 18 or 24 bits parallel interface along with the required control signals for the Pixel clock and HSync/VSync/DE.

The TC358766XBG also supports content protection using HDCP copy protection.

The DisplayPort™ transmitter supports data throughput at 1.62 Gbps or 2.7 Gbps per lane of main link.

TC358766XBG supports five (6) configuration modes as briefed below. These modes mainly differ based on the source of input stream and number of display devices that TC358766XBG can be connected to.

- Mode_S21: A system configuration where TC358766XBG may typically be used is shown in Figure 1.1. In this system, TC358766XBG could be connected to a single display. In this configuration, the TC358766XBG can support displays with resolution up to WUXGA (1920x1200) at 24bit, 60 fps or WUXGA (1920x1200) at 18bit, 60 fps. Video stream source is from DSI Host.
- Mode_S22: An alternate system configuration where TC358766XBG may typically be used is shown in Figure 1.2. In this system, TC358766XBG could be connected to two independent displays. In this configuration, the TC358766XBG can support displays with resolution up to WXGA+, WSXGA (1440x900) at 24bit, 60 fps or WSXGA+ (1680x1050) at 18bit, 60 fps. Video stream source is from DSI Host. Both display devices are used to display the same video stream.
- Mode_P21: A system configuration where TC358766XBG may typically be used is shown in Figure 1.3. This is similar to the Mode_S21 except that the video stream source is from DPI Host. In this configuration, the TC358766XBG can support displays with resolution up to WUXGA (1920x1200) at 24bit, 60 fps.
- Mode_P22: An alternate system configuration where TC358766XBG may typically be used is shown in Figure 1.4. This is similar to the Mode_S22 except that the video stream source is from DPI Host. Same video stream is displayed on both display devices. In this configuration, the TC358766XBG can support displays with resolution up to WXGA+, WSXGA (1440x900) at 24bit, 60 fps or WSXGA+ (1680x1050) at 18bit, 60 fps.
- Mode_SP22: In this mode, the DisplayPort™ Tx Main links are used as two independent links (each one lane) as shown in Figure 1.5. One DisplayPort™ Tx Main link lane is used to receive the video stream from the DSI Rx port, while the second DisplayPort™ Tx Main link lane is used to receive the video stream from the DPI Rx port. In this configuration, the TC358766XBG can support displays with resolution up to WXGA+, WSXGA (1440x900) at 24bit, 60 fps or WSXGA+ (1680x1050) at 18bit, 60 fps.
- Mode_S2P: A system configuration where TC358766XBG may typically be used is shown in Figure 1.6. In this mode, DisplayPort™ output is not used and the chip rather behaves as a DSI to RGB convertor. In this system, TC358766XBG could be connected to a single display. In this configuration, the TC358766XBG can support displays with resolution up to WXGA (1280x800 or 1366x768). Max output PCLK is 80 MHz. Video stream source is from DSI Host.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link or the shutdown pin (SD) during DPI input mode.

The following figures show all these modes, where TC358766XBG, display panels and a Host are connected in target Reference system for mobile large display panel applications.

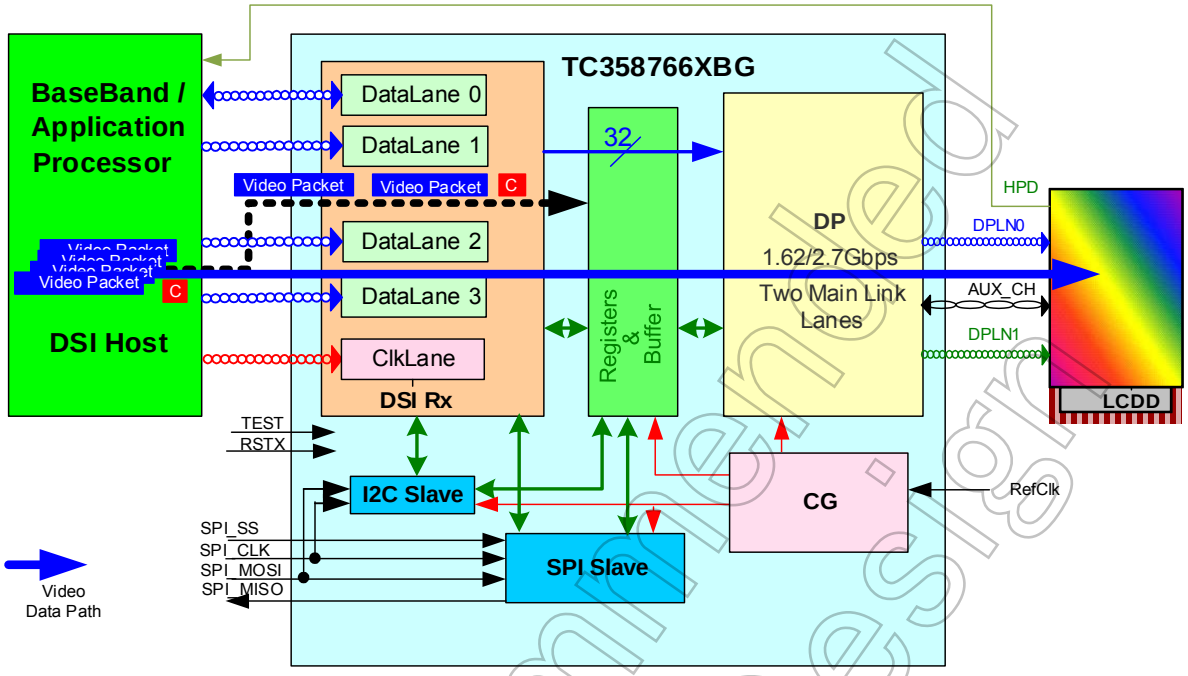


Figure 1.1 System Overview with TC358766XBG in MODE_S21 Configuration

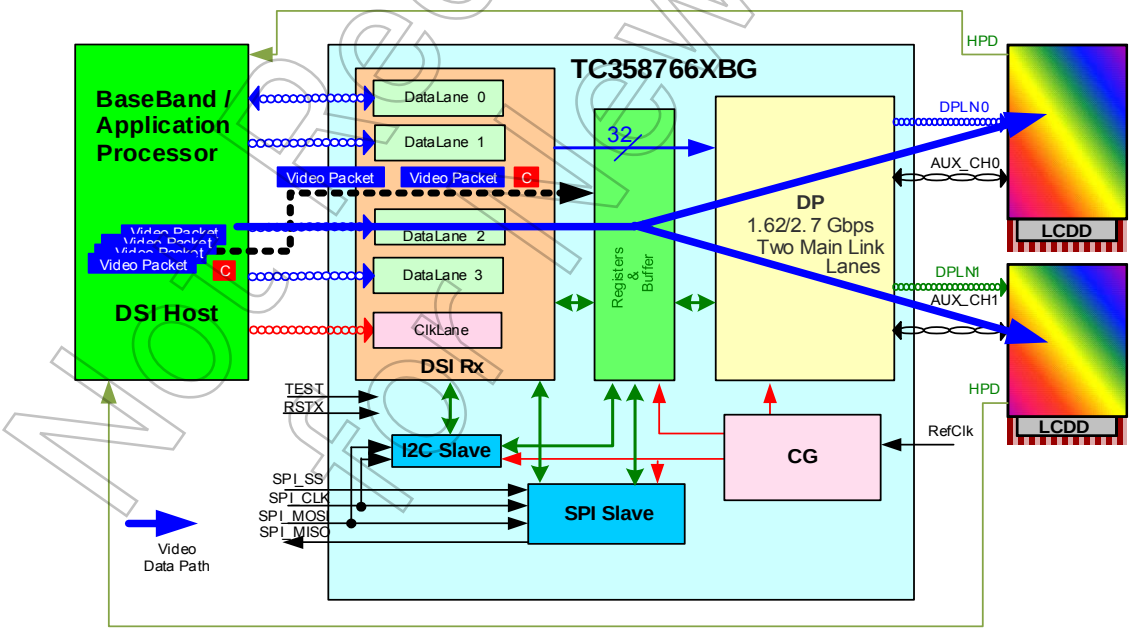


Figure 1.2 System Overview with TC358766XBG in MODE_S22 Configuration

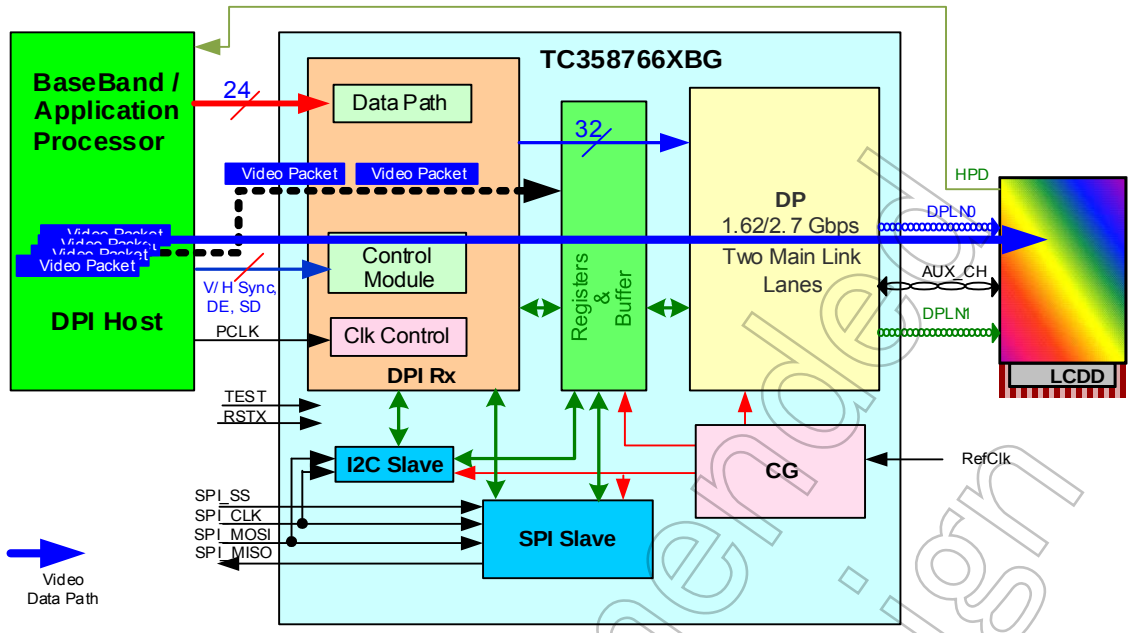


Figure 1.3 System Overview with TC358766XBG in MODE_P21 Configuration

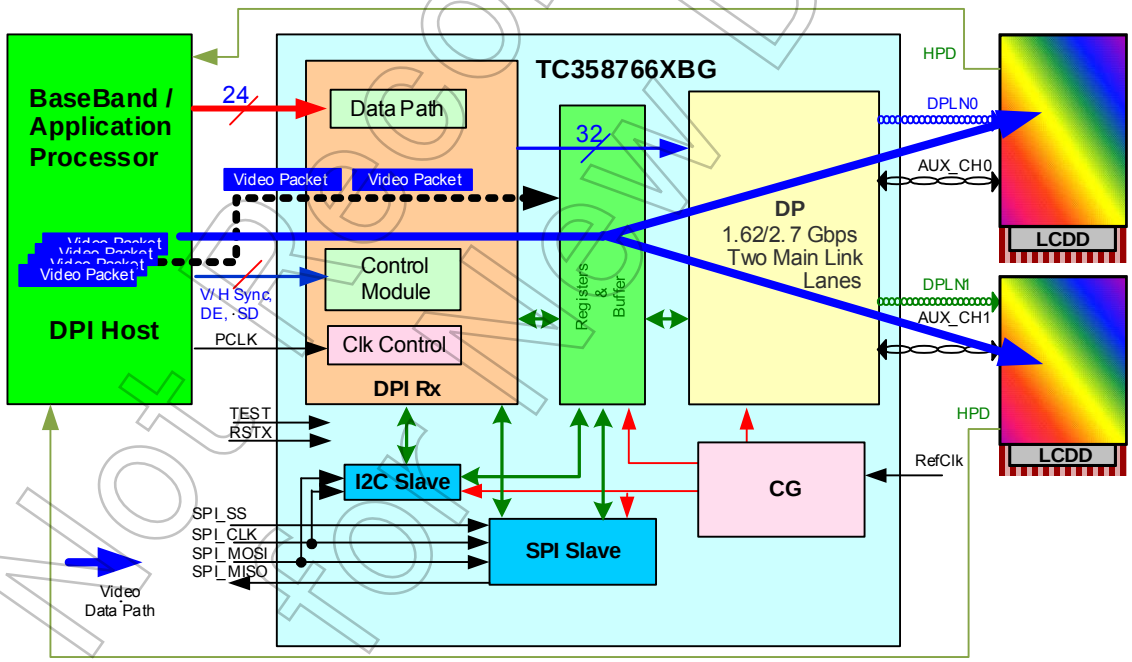


Figure 1.4 System Overview with TC358766XBG in MODE_P22 Configuration

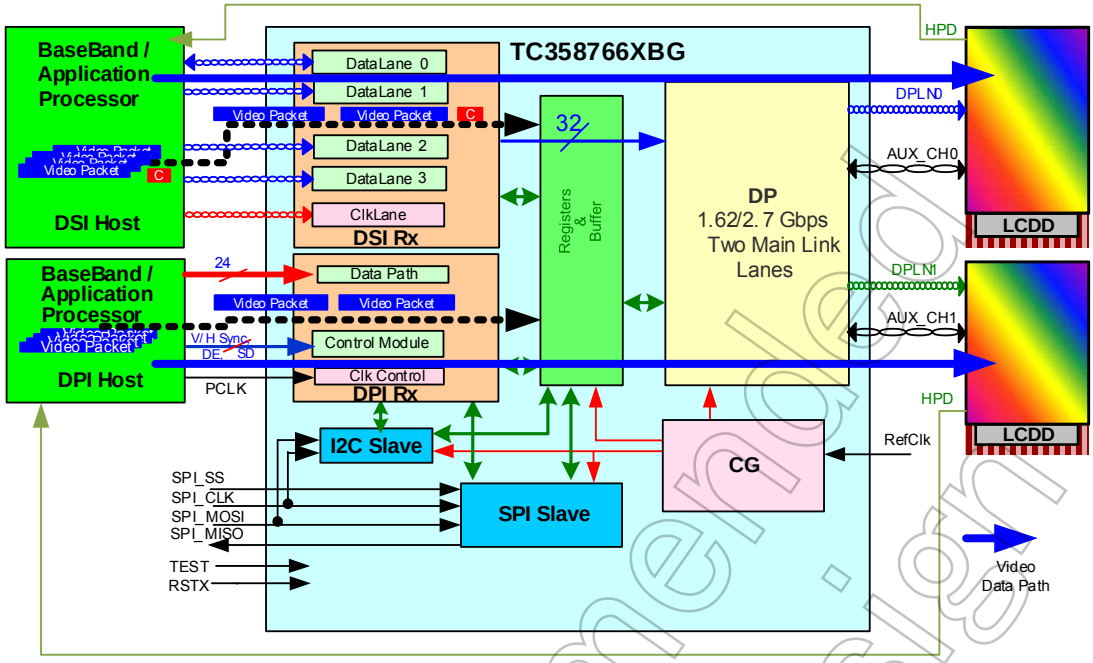


Figure 1.5 System Overview with TC358766XBG in MODE_SP22 Configuration

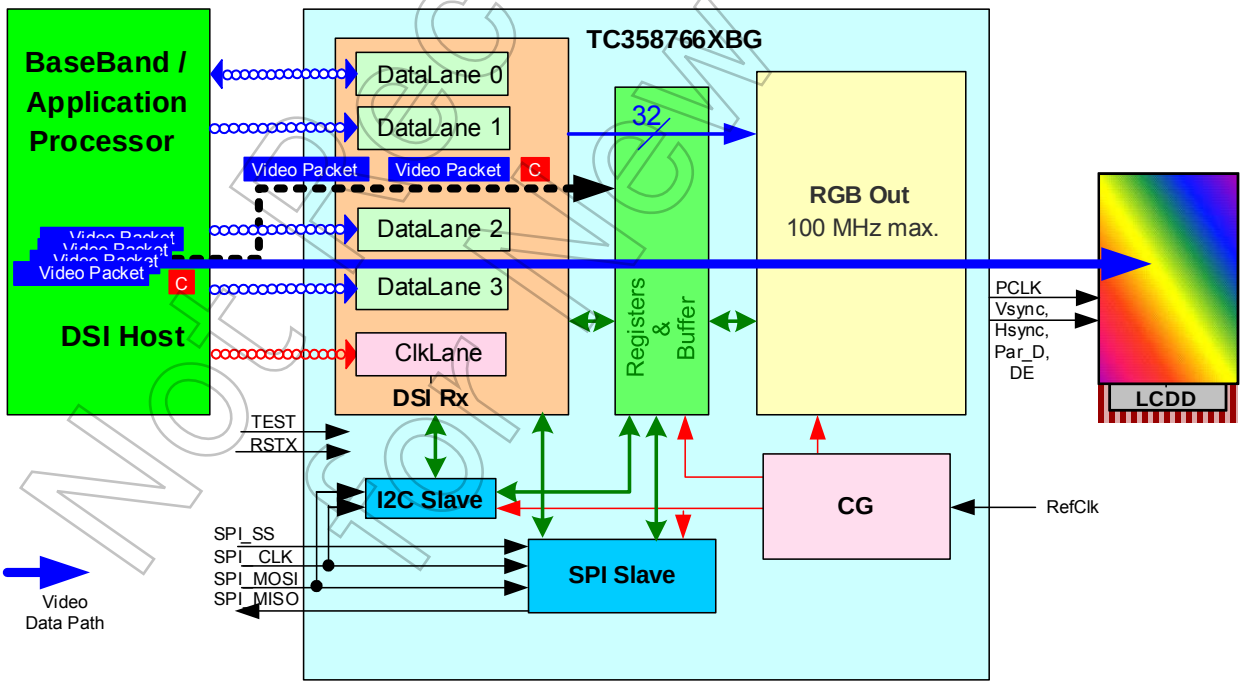


Figure 1.6 System Overview with TC358766XBG in MODE_S2P Configuration

2. Features

Below are the main features supported by TC358766XBG.

- Translates MIPI® DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, upto1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration: From DSI link, SPI or I²C interface (only one of the SPI and I²C interfaces can be active at any time).
- Internally generated H/VSync in DSI mode can be muxed out to Host.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP o/p testing without any video (DSI/DPI) i/p.
- Debug/Test Port: I²C Slave
- **DSI Receiver:** Supports one DSI Interface between TC358766XBG and Host.
  - ✧ MIPI® DSI: v1.01 / MIPI® D-PHY: v0.90 Compliant.
  - ✧ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Supports Burst as well as Non-Burst Mode Video Data.
    - Video data packets are limited to one row per Hsync period.
  - ✧ Supports video stream packets for video data transmission.
  - ✧ Supports generic long packets for accessing the chip's register set.
  - ✧ Video input data formats:
    - RGB-565, RGB-666 and RGB-888.
    - New DSI V1.02 Data Type Support: 16-bit YCbCr 422
  - ✧ Interlaced video mode is not supported.
- **DPI Receiver:** Supports one DPI Interface between TC358766XBG and Host.
  - ✧ Up to 16 / 18 / 24 bit parallel data interface.
  - ✧ Maximum speed at 154 MPs (MPixel per sec).
  - ✧ Video input data formats: RGB-565, RGB-666 and RGB-888.
  - ✧ Only Progressive mode supported.
  - ✧ Shutdown support (can be used in non-DPI mode also).
- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC358766XBG to display panels.
  - ✧ High speed serial bridge chip using VESA DisplayPort™ 1.1a Standard.
  - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications
  - ✧ Supports up to two (2) single-lane ports for connection to two DisplayPort™ panels.
  - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2V
  - ✧ Support of pre-emphasis levels of 0, 3.5dB and 6dB.
  - ✧ AUX channel supported at 1 Mbps.
  - ✧ HPD support through GPIO[1:0] based interrupts
  - ✧ Enhanced mode supported for HDCP content protection.
  - ✧ Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1. (on DisplayPort™0 in case two port configuration is used)

- ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
  - Start Link training in response to HPD & read final Link training status
  - Configure DP link for actual video streaming & start video streaming
- ✧ Link Policy maker is assumed shared between the Host and TC358766XBG chip.
  - In auto_correction = 0 mode, control link training
  - Initiate Display device capabilities read and configure TC358766XBG accordingly.
- ✧ Video timing generation as per panel requirement.
- ✧ SSCG with up to 30 kHz modulation to reduce EMI.
- ✧ Toshiba Magic Square algorithm – RGB666 18b produces RGB888 24b like quality (with up to 16-million colors).
- ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
  - ✧ RGB888 output mode (DisplayPort™ disabled) with only DSI input supported in this mode
  - ✧ PCLK max = 100 MHz
  - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE.
- **I²C Interface:**
  - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
  - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).
- **SPI Interface:**
  - ✧ SPI slave interface for chip register set access enabled using a boot-strap option.
  - ✧ SPI interface support for up to 30 MHz operation.
- **GPIO Interface:**
  - ✧ 2 bits of GPIO (shared with other digital logic).
  - ✧ Direction controllable by Host I²C accesses.
- **Clock Source:**
  - ✧ DisplayPort™ clock source is from an external clock input or clock from DSI interface (13, 26, 19.2 or 38.4 MHz) – generates all internal & output clocks to interfacing display devices.
  - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:** Supports six (6) modes of operation:
  - ✧ MODE S21: TC358766XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DSI Host.
  - ✧ MODE S22: TC358766XBG uses DisplayPort™ Tx port as two independent 1-lane DisplayPort™ links to interface to two (2) DisplayPort™ display devices. Video stream source is from MIPI® DSI Host. Same video stream can be displayed on two display devices.
  - ✧ MODE P21: TC358766XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI® DPI Host.
  - ✧ MODE P22: TC358766XBG uses DisplayPort™ Tx port as two independent 1-lane DisplayPort™ links to interface to two (2) DisplayPort™ display devices. Video stream source is from MIPI® DPI Host. Same video stream is displayed on two display devices.
  - ✧ MODE SP22: TC358766XBG uses DisplayPort™ Tx as two independent DisplayPort™ output links (each single lane). TC358766XBG routes the DSI input to one DisplayPort™ Tx link and routes the DPI input to the second DisplayPort™ Tx link.

- ✧ MODE S2P: TC358766XBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI® DSI Host.

- **Power supply inputs**
  - ✧ Core and MIPI® D-PHY: 1.2V ±0.06V
  - ✧ Digital I/O: 1.8V ±0.09V
  - ✧ DisplayPort™: 1.8V ±0.09V
  - ✧ DisplayPort™: 1.2V ±0.06V
- **Power Consumptions (based on estimations)**
  - ✧ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
    - DSI Rx: 0.01 mW
    - DP PHY: 2.34 mW
    - PLL9: 0.01 mW
    - Core: 0.96 mW
    - Rest: 0.01 mW
  - ✧ Normal operation (DSI-Rx in 4-lane @900 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
    - DSI Rx: 21.79 mW
    - DP PHY: 142.70 mW
    - PLL9: 2.42 mW
    - Core: 87.64 mW
    - IOs: 1.68 mW
- **Package**
  - 0.5mm ball pitch, 120 balls, 6 x 6 mm BGA package

Table 2.1 TC358766XBG operational modes summary with panel size support information

Mode	Input Configuration			Register Access Method	Output Configuration	
	# of input streams	DSI input	DPI input		# of output panels	Max Panel size example
S21	1	Active	X	DSI or DSI+I²C or DSI+SPI	1	WUXGA 18bpp @ 60fps WUXGA 24bpp @ 60fps
S22	1	Active	X	DSI or DSI+I²C or DSI+SPI	2	WSXGA+ 18bpp @ 60fps WXGA+ 24bpp @ 60fps WSXGA 24bpp @ 60fps
P21	1	X	Active	I²C or SPI	1	WUXGA 24bpp @ 60fps
P22	1	X	Active	I²C or SPI	2	WSXGA+ 18bpp @ 60fps WXGA+ 24bpp @ 60fps WSXGA 24bpp @ 60fps
SP2	2	Active	Active	DSI or DSI+I²C or DSI+SPI	2	WSXGA+ 18bpp @ 60fps WXGA+ 24bpp @ 60fps WSXGA 24bpp @ 60fps

Tables below provide an idea of different panel sizes that can be supported by using different data link lane configurations.

Table 2.2 Panel Size v/s Data link required by TC358766XBG in DSI input case

Frame Size			FPS	Pixel Clock (MHz)	RGB666				RGB888			
-	-	With OverHead			Bit Rate (Gbps)	# DSI Data lanes	# DP Main links		Bit Rate (Gbps)	# DSI Data lanes	# DP Main links	
							1.62G	2.7G			1.62G	2.7G
XGA	1024x768	1184x790	60	56	1.01	2	1	1	1.34	2	2	1
WXGA+ / WSXGA	1440x900	1600x926	60	89	1.60	2	2	1	2.13	3	2	1
SXGA+	1400x1050	1560x1080	60	89	1.82	2	2	1	2.43	3	2	2
WSXGA+	1680x1050	1840x1080	60	119	2.15	3	2	1	2.86	3	-	2
UXGA	1600x1200	1760x1235	60	130	2.35	3	2	2	3.13	-	-	2
WUXGA	1920x1200	2080x1235	60	154	2.77	3	-	2	3.70	-	-	2

Table 2.3 Panel Size v/s Data link required by TC358766XBG in DPI input case

Frame Size			FPS	Pixel Clock (MHz)	DPI Support 154 MHz PCLK	RGB666			RGB888		
-	-	With OverHead				Bit Rate (Gbps)	# DP Main links		Bit Rate (Gbps)	# DP Main links	
							1.62G	2.7G		1.62G	2.7G
XGA	1024x768	1184x790	60	56	Yes	1.01	1	1	1.34	2	1
WXGA+ / WSXGA	1440x900	1600x926	60	89	Yes	1.60	2	1	2.13	2	1
SXGA+	1400x1050	1560x1080	60	89	Yes	1.82	2	1	2.43	2	2
WSXGA+	1680x1050	1840x1080	60	119	Yes	2.15	2	1	2.86	-	2
UXGA	1600x1200	1760x1235	60	130	Yes	2.35	2	2	3.13	-	2
WUXGA	1920x1200	2080x1235	60	154	Yes	2.77	-	2	3.70	-	2

Note: These are the formats commonly used by displays. Support for other sizes is possible as long as they satisfy the maximum data rate constraints on the DSI and DisplayPort™ link interfaces.

NOTE: Throughout the rest of the document, "DP" is used to denote "DisplayPort™". Both these words have been used interchangeably and refer to the VESA DisplayPort™ specification as mentioned in the references.

3. External Pins

TC358766XBG chip uses a 120pin package. Following table gives the signals of TC358766XBG and their function.

Table 3.1 TC358766XBG Functional Signal List for 120-pin Package

Group	Pin Name	I/O	Type	Initial	Function	Note
System: Reset & Clock (14)	RESX	I	Sch	-	System Reset – active Low	-
	REFCLK	I	Sch	-	13, 26, 19.2 or 38.4 MHz 50ps phase jitter p2p/ WC duty cycle 40-60%	-
	TEST	I	N	Low	Test Pin, active high	-
	TEST[6:4]	I	N	-	Test Pins, connect to GND	-
	INT	O	N	-	Interrupt to Host	4mA
	SD	I	N	-	Shutdown Input/ Audio Over Sampling Clock *Note1	-
	SYNC	O	N	-	Internal H/V Sync o/p to Host	4mA
	MODE[4:0]	I	N	Low	Mode Selection pins	-
DSI Rx (10)	DSICP	I	MIPI®-PHY	-	MIPI®-DSI Rx Clock Lane Pos	-
	DSICM	I	MIPI®-PHY	-	MIPI®-DSI Rx Clock Lane Neg	-
	DSIDP[3:0]	I/O	MIPI®-PHY	-	MIPI®-DSI Rx Data Lane Pos	-
	DSIDM[3:0]	I/O	MIPI®-PHY	-	MIPI®-DSI Rx Data Lane Neg	-
DP Out (12)	DPLNP[1:0]	O	DP-PHY	-	eDP Output Main Link Pos	-
	DPLNM[1:0]	O	DP-PHY	-	eDP Output Main Link Neg	-
	DPAUXP[1:0]	I/O	DP-PHY	-	eDP Output AUX Channel Pos	-
	DPAUXM[1:0]	I/O	DP-PHY	-	eDP Output AUX Channel Neg	-
	ATB[1:0]	I/O	DP-PHY	-	Analog Test Bus output *Note1	-
	PREC_RES[1:0]	I	DP-PHY	-	Precision Resistance (3K @ 1%) connection	-
DPI Rx (28)	DPI_PCLK	I/O	N	-	DPI Pixel Clock (max 154 MHz) (default: Input) *Note1	4mA
	DPI_VSYNC	I/O	N	-	DPI Vertical Sync (default: Input) *Note1	4mA
	DPI_HSYNC	I/O	N	-	DPI Horizontal Sync (default: Input) *Note1	4mA
	DPI_DE	I/O	N	-	DPI Data Enable (default: Input) *Note1	4mA
	DPI_D [23:0]	I/O	N	-	DPI Parallel Data (default: Input) *Note1	4mA
SPI / I²C (4)	SPI_SCLK / I2C_SCL	OD	FS/Sch	-	SPI Clock / I²C Clock *Note1	-
	SPI_MOSI / I2C_SDA	OD	FS/Sch	-	SPI Input data from Host *Note1	4mA
	SPI_MISO	O	N	-	SPI Output data to Host	4mA
	SPI_SS/ I2C_ADR_SEL	I	N	-	SPI Slave Select / I²C Slave Address Select *Note1	-
GPIO (2)	GPIO[1:0]	OD	5T-OD	-	GPIO or Test Control *Note1 GPIO[1:0] can be used for HPD support	4mA
POWER (27)	VDDC (*VDD12*)	NA	-	-	VDD for Internal Core (8)	-
	VDDS (1.8V)	NA	-	-	VDDS for IO Ring power supply (5)	-
	VDD_PLL18 (1.8V)	NA	-	-	VDD for DP PHY PLLs (2)	-
	VDD_PLL12 (1.2V)	NA	-	-	VDD for DP PHY PLLs (2)	-
	VDD_DP18 (1.8V)	NA	-	-	VDD for DP PHY Main Channels (2)	-
	VDD_DPA18 (1.8V)	NA	-	-	VDD for DP PHY Aux Channels	-
	VDD_DP12 (1.2V)	NA	-	-	VDD for DP PHY (2)	-
	VDD_DSI12 (1.2V)	NA	-	-	VDD for the MIPI® DSI PHY (2)	-
	VDD_PLL912 (1.2V)	NA	-	-	VDD for the PLL9	-
	VPGM	NA	-	-	eFUSE programming voltage (2)	-
GROUND (23)	VSS	NA	-	-	Ground (including VSSC (core), VSS_IO (IO), VSS_DSI (MIPI®), VSS_DP (DP), VSS_DPA, VSS_PLL (PLL))	-

Total 120 pins BGA package.

Note 1: Pins with multiplexed Functional mode functions

N: Normal IO
PHY: Either DP analog front end or MIPI® D-PHY
OD: Open drain
Pd: Pull Down
FS: Fail safe IO - gated
Sch: Schmitt trigger input
5T-OD: 5V tolerant bi-direction buffer with Open drain

3.1. Pin Mapping

The mapping of TC358766XBG signals to the external pins is given in the following figure. (BGA array)

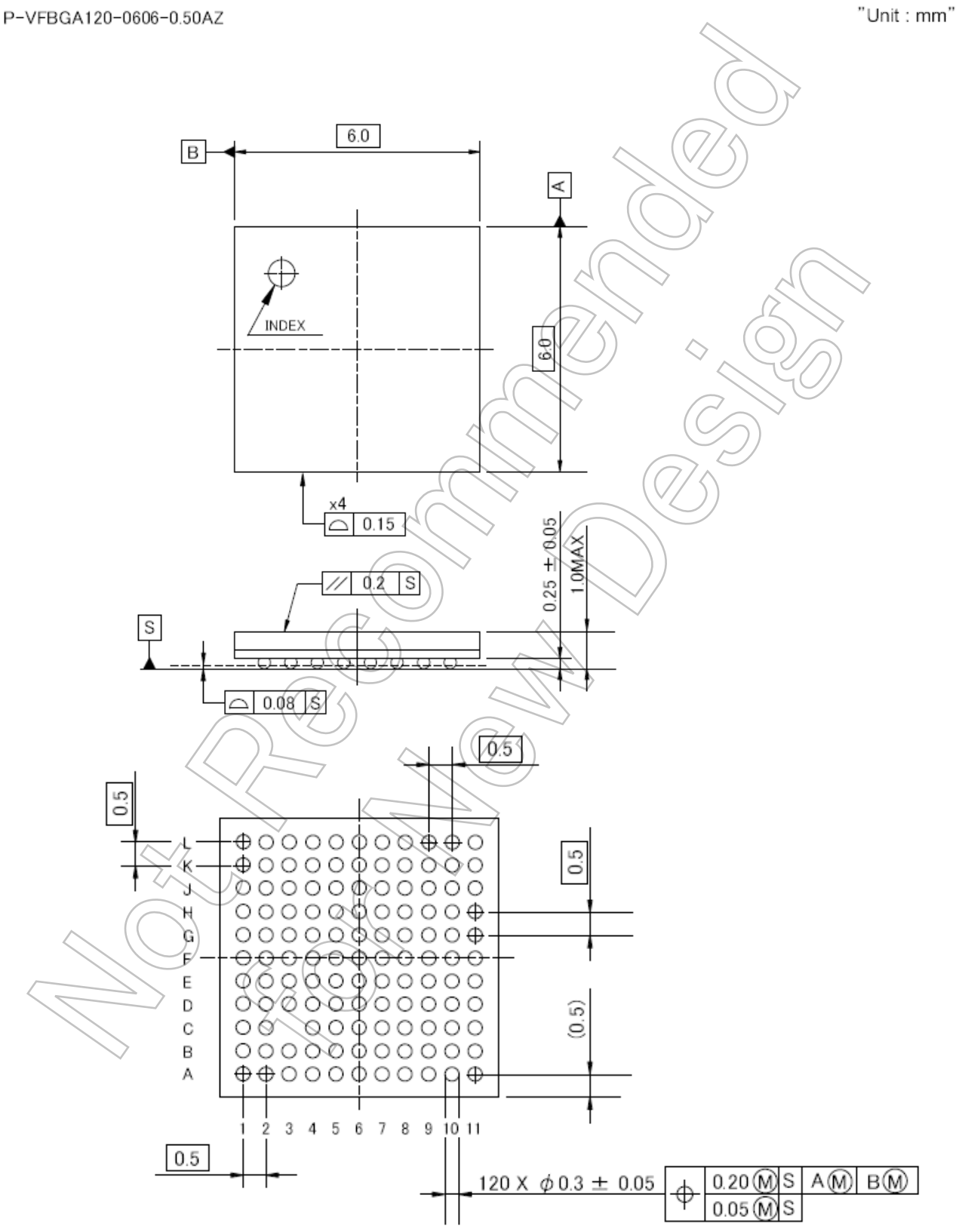
Top View (through the die)

A1 MODE_2	A2 MODE_3	A3 DPI_VSYNC	A4 DPI_DE	A5 DPI_D_0	A6 DPI_D_2	A7 DPI_D_3	A8 DPI_D_5	A9 DPI_D_7	A10 DPI_D_9	A11 DPI_D_11
B1 DSIDM_0	B2 DSIDP_0	B3 MODE_0	B4 VDDC	B5 DPI_D_1	B6 SD	B7 DPI_D_4	B8 DPI_D_6	B9 DPI_D_8	B10 DPI_D_10	B11 DPI_D_12
C1 DSIDM_1	C2 DSIDP_1	C3	C4 VSS	C5 TEST_4	C6 TEST_6	C7 DPI_HSYNC	C8 SPI_MISO	C9 VDDC	C10 DPI_D_14	C11 DPI_D_13
D1 VSS_DSI	D2 VDD_DSI12	D3 MODE_1	D4 INT	D5 TEST_5	D6 SPI_SS	D7 VDDC	D8 VSS	D9 VPGM_1	D10 SPI_SCLK	D11 DPI_D_15
E1 DSICM	E2 DSICP	E3 TEST	E4 SYNC	E5 VSS	E6 VSS	E7 VSS	E8 VDDS	E9 SPI_MOSI	E10 DPI_D_17	E11 DPI_D_16
F1 VDD_DSI12	F2 VSS_DSI	F3 MODE_4	F4 GPIO_0	F5 VSS_E	F6 VSS_E	F7 VSS_E	F8 RESX	F9 GPIO_1	F10 VPGM_0	F11 DPI_D_18
G1 DSIDM_2	G2 DSIDP_2	G3 PREC_RES_0	G4 VDDC12	G5 VSS_E	G6 VSS_E	G7 VSS_E	G8 VSS_PLL9	G9 VDDS	G10 VDDC	G11 DPI_PCLK
H1 DSIDM_3	H2 DSIDP_3	H3 PREC_RES_1	H4 VDD18	H5 VDDC	H6 VDD18	H7 VDD18	H8 VDDC	H9 VSSC	H10 DPI_D_19	H11 VDD_PLL912
J1 ATB_1	J2 VDD_PLL18	J3 VDD_PLL12	J4 VSS_PLL	J5 VSS_PLL	J6 VDD_PLL12	J7 VDD_PLL18	J8 VSS	J9 VDDC	J10 DPI_D_21	J11 DPI_D_20
K1 REFCLK	K2 VDD_DP12	K3 DPLNP_0	K4 VSS_DP	K5 VDD_DP12	K6 DPLNP_1	K7 VSS_DP	K8 DPAUXP_0	K9 VSS_DPA	K10 DPAUXP_1	K11 DPI_D_22
L1 ATB_0	L2 VSS_DP	L3 DPLNM_0	L4 VDD_DP18	L5 VSS_DP	L6 DPLNM_1	L7 VDD_DP18	L8 DPAUXM_0	L9 VDD_DPA18	L10 DPAUXM_1	L11 DPI_D_23

Figure 3.1 TC358766XBG 120-Pin Layout

4. Package

The package for TC358766XBG is described in the figure below.



Weight : 62mg (Typ.)

Figure 4.1 120 pin TC358766XBG package

The mechanical dimension of BGA120 package is listed below.

Table 4.1 Mechanical Dimension of P-VFBGA120-0606-0.50AZ

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height	Note
120-Pin	0.50 mm	0.25 mm	6.0 x 6.0 mm^2	1.0 mm	—

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

VDD18 used for VDDS as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V)	VDD18	-0.3 to +3.5	V
Supply voltage (1.2V)	VDD12	-0.3 to +2.0	V
Supply voltage (IO)	VDD18	-0.3 to +3.5	V
	VREF	-0.3 to +3.5	V
Input voltage	VIN	-0.3 to VDDS+0.3	V
Output voltage	VOUT	-0.3 to VDDS+0.3	V
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS = 0 V reference

VDD18 used for VDDS as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V)	VDD18	1.71	1.8	1.89	V
Supply voltage (1.2V)	VDD12	1.14	1.2	1.26	V
Operating frequency (internal)	Fopr	-	-	200	MHz
Operating temperature	Ta	-20	-	+70	°C

5.3. DC Electrical Specification

VSS = VSS_C = VSS_IO = VSS_DSI = VSS_DP = VSS_PLL = VSS_REG = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input Note1	VIH	0.7 VDDS	-	VDDS	V
Input voltage Low level CMOS input Note1	VIL	0	-	0.3 VDDS	V
Input voltage High level CMOS Schmitt Trigger Note1	VIHS	0.7 VDDS	-	VDDS	V
Input voltage Low level CMOS Schmitt Trigger Note1	VILS	0	-	0.3 VDDS	V
Output voltage High level Note1, Note2	VOH	0.8 VDDS	-	VDDS	V
Output voltage Low level Note1, Note2	VOL	0	-	0.2 VDDS	V
Input leak current High level	IIH1 (Note3)	-10	-	10	μA
Input leak current Low level	IIL1 (Note4)	-10	-	10	μA
	IIL2 (Note5)	-200	-	-10	μA

Note1: VDDS within recommended operating condition.

Note2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note3: Normal pin, or Pull-up I/O pin applied VDD18_IO supply voltage to input pin

Note4: Normal pin applied VSS (0V) to input pin

Note5: Pull-up I/O pin applied VSS (0V) to input pin

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.1	2014-07-23	Newly released
0.12	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.0	2017-11-07	Modified descriptions in Features. Deleted I2S descriptions. Modified Figure 1.1 to Figure 1.6, Figure 3.1 and Table 3.1. Deleted Table 3.2. (It is the same as Table 4.1.) Added section 5 Electrical Characteristics. Changed header, footer and the last page. Changed corporate name.
1.01	2017-12-27	Modified Figure 1.1 to Figure 1.6. Changed frequency to 100MHz in Figure 1.6. Added description, trademarks and modified registered trademarks.
1.1	2018-05-28	Modified Table 2.2 and Table 2.3.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**