HIGH SPEED QUAD CHANNEL DIGITAL ISOLATORS

DCL541x01,DCL542x01

DCL541L01/DCL541H01/DCL542L01/DCL542H01

1. Applications

- Industrial automation systems
- Motor control
- Inverter
- Switching power supply

2. Description

DCL541L01 / DCL541H01 / DCL542L01 / DCL542H01 are high-speed quad-channel digital isolators. Outstanding performance characteristics are achieved by Toshiba CMOS technology and the magnetic coupling structure. In addition, they comply with UL 1577 and has a 5000V_{rms} rating as an isolation voltage. These products can operate with a temperature range of -40 to 110 °C and a wide supply voltage of 2.25 to 5.5 V.

3. Features

Data rate	: Up to 150 Mbps
Supply voltage	: 2.25V to 5.5 V
Temperature Range	: -40°C to 110 °C
Propagation Delay	:10.9 ns Typ. (5.0 V operation)
Default Output	: High and Low Options
CMTI(min)	: 100 kV/μs
Withstand Voltage	: 5 kV_{rms}
Package	: 16pin SOIC Wide body
Safety-Related Certification	:

UL	: UL 1577, File No. E519997
cUL	: CSA Component Acceptance Service Notice No. 5A, File No. E519997
VDE	: DIN EN IEC 60747-17 (VDE V 0884-17) Certificate No.40055132 (Note 1)
CQC	: GB 4943.1-2022 Certificate No. CQC22001345018

Note 1:When a VDE approved type is needed, please contact your Toshiba sales representative.

Start of commercial production
2023-11

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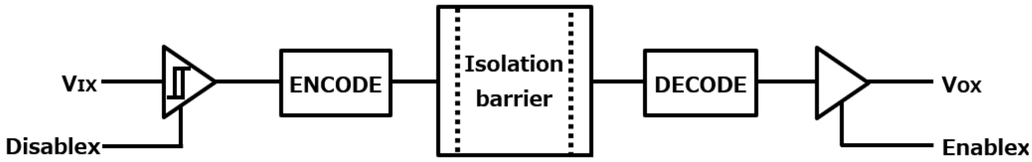
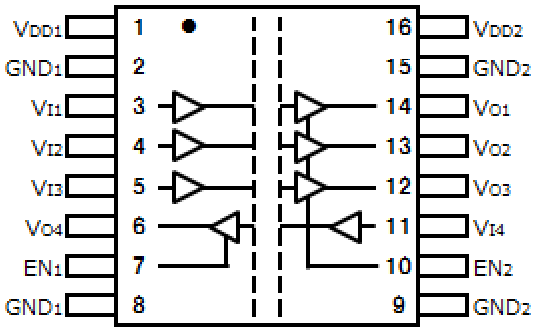
4. Internal Circuit

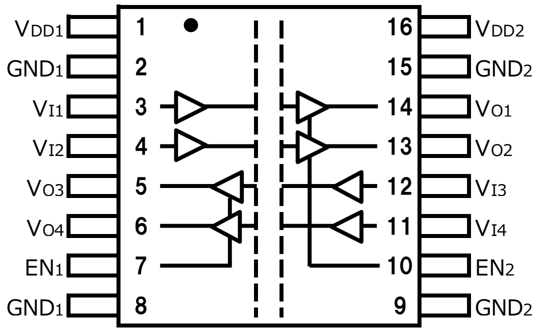


5. Pin configuration and Functions

DCL541L01 / DCL541H01



DCL542L01 / DCL542H01



5.1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DCL541L01 DCL541H01	DCL542L01 DCL542H01		
V_{DD1}	1	1	-	Power Supply, side 1
GND_1	2, 8	2, 8	-	GND connection for V_{DD1} , side 1
V_{I1}	3	3	I	Input, Channel1
V_{I2}	4	4	I	Input, Channel2
V_{I3}	5	12	I	Input, Channel3
V_{I4}	11	11	I	Input, Channel4
EN_1	7	7	I	Output enable 1. Input pins on side 1 are enabled when EN_1 is high or open, and in high impedance state when EN_1 is low.
GND_2	9, 15	9, 15	-	GND connection for V_{DD2}, side 2
EN_2	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN_2 is high or open, and in high impedance state when EN_2 is low.
V_{o4}	6	6	O	Output, Channel4
V_{o3}	12	5	O	Output, Channel3
V_{o2}	13	13	O	Output, Channel2
V_{o1}	14	14	O	Output, Channel1
V_{DD2}	16	16	-	Power Supply, side 2

6. Functional Description

(1) DCL541L01/DCL541H01 / DCL542L01/DCL542H01

V_{DDI}	V_{DDO}	OUTPUT ENABLE (ENx)	INPUT (V_{IX})	OUTPUT (V_{OX})	DESCRIPTION
PU	PU	H or OPEN	L	L	Normal Operation
			H	H	
			OPEN	Default	Default mode DCL54xL01=L , DCL54xH01=H
		L	*	Z	Output Disable mode
PU	PD	*	*	Undetermined	When V_{DDO} is unpowered, a channel output is undetermined.
PD	PU	H or OPEN	*	Default	Default mode DCL54xL01=L , DCL54xH01=H
		L		Z	Output Disable mode
PD	PD	*	*	Undetermined	When V_{DDO} is unpowered, a channel output is undetermined.

PU= Powered up (V_{DD}≥2.25 V), PD= Powered down (V_{DD}≤1.7 V), H= High level, L= Low level, * = Don't care
V_{DDI}, V_{DDO} : Supply voltages on the input and output sides of each channel.
ENx : Output enable signal on the same side as the VOX output.
V_{IX}, V_{OX} : Input and output signals of each channel.
When the input pin on the power-off side is set to "H", power is supplied to the device via the ESD circuit, so use is prohibited.

7. Absolute Maximum Ratings (Ta = 25 °C)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Input Voltage	V_I	-0.5	V_{DDX}+0.5(1)	V
Output Voltage	V_O	-0.5	V_{DDX}+0.5(1)	V
Output Current	I_O	-15	15	mA
Storage Temperature	T_{stg}	-65	150	°C
Operating Temperature	T_{opr}	-40	110	°C
Soldering Temperature (10 s)	T_{sol}	-	260	°C
Maximum Withstanding Isolation Voltage (1 min.)	BV_S	-	5000	V_{rms}

Note(1) : Maximum voltage must not exceed 6 V. X = 1 or 2.

8. Recommended Operating Conditions (Note)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power supply voltage	V_{DD1}, V_{DD2}	2.25	5.5	V
Junction Temperature	T_J	-40	150	°C
Operating Temperature	T_{opr}	-40	110	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND2) for V_{DD2}, and should be the layout on the IC as close as possible (less than 10 mm). Otherwise, the IC may not switch properly.

9. Electrical Characteristics

9.1. Electrical Characteristics – 5 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V≤V_{DD1}≤5.5 V, 4.5 V≤V_{DD2}≤5.5 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1 12.3	V_{DDXUV+}	-	2.10	2.25	V
	Threshold when supply voltage is falling		V_{DDXUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDXUVH}	0.1	0.2	-	
Output Voltage Logic High	V_{Ix} = H , I_{OH} = -20 μA	12.5	V_{OH}	V_{DDO}(1)-0.1	V_{DDO}(1)	-	V
	V_{Ix} = H , I_{OH} = -4 mA			V_{DDO}(1)-0.4	V_{DDO}(1)-0.2	-	
Output Voltage Logic Low	V_{Ix} = L , I_{OL} = 20 μA	12.5	V_{OL}	-	0.0	0.1	V
	V_{Ix} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	12.5	Z_O	-	50	-	Ω
High-level input voltage	-	12.7	V_{IH}	0.7*V_{DDI}(1)	-	-	V
Low-level input voltage	-	12.7	V_{IL}	-	-	0.3*V_{DDI}(1)	V
Input Voltage Hysteresis	-	12.7	V_{HYS}	-	0.37	-	V
Input Current	V_I= V_{DDI}(1) or 0 V	-	I_I	-	-	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12.9	t_{PHL} , t_{PLH}	-	10.9	18.3	ns
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	12.9	PWD	-	0.8	2.8	ns
Propagation Delay Skew(2) (Between any two units)	-	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.9	t_{skCD}	-	-	3.2	ns
	Opposing Direction	12.9	t_{skOD}	-	-	3.6	
Output Rise Time	10 % - 90 %	12.9	t_r	-	0.9	-	ns
Output Fall Time	90 % - 10 %	12.9	t_f	-	0.9	-	ns
Enable 3-state output enable time(3)	50 kHz, Duty=50 %, tr=tf=2 ns,C_L=15 pF	12.12	t_{pZL} , t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time		12.12	t_{pLZ} , t_{pHZ}	-	-	18.0	ns
Common mode transient immunity	V_I= V_{DDI} or 0 V , VCM=1500 V , T_a=25 °C	12.15	| CMTI |	100	-	-	kV/μs

Note(1): V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}

Note(2): Propagation delay difference (between parts) is applied under the same operating conditions. (Power supply voltage. input current, temperature conditions, etc.).

Note(3):When EN_X signal is changed from Low to High or OPEN, the output signal (V_{Ox}) is valid after the output enable time. The output signal (V_{Ox}) within the output enable time is undefined.

9.2. Electrical Characteristics – 3.3 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V≤V_{DD1}≤3.6 V, 3.0 V≤V_{DD2}≤3.6 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1 12.3	V_{DDXUV+}	-	2.10	2.25	V
	Threshold when supply voltage is falling		V_{DDXUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDXUVH}	0.1	0.2	-	
Output Voltage Logic High	V_{Ix} = H , I_{OH} = -20 μA	12.5	V_{OH}	V_{DDO}(1)-0.1	V_{DDO}(1)	-	V
	V_{Ix} = H , I_{OH} = -4 mA			V_{DDO}(1)-0.4	V_{DDO}(1)-0.2	-	
Output Voltage Logic Low	V_{Ix} = L , I_{OL} = 20 μA	12.5	V_{OL}	-	0.0	0.1	V
	V_{Ix} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	12.5	Z_O	-	50	-	Ω
High-level input voltage	-	12.7	V_{IH}	0.7*V_{DDI}(1)	-	-	V
Low-level input voltage	-	12.7	V_{IL}	-	-	0.3*V_{DDI}(1)	V
Input Voltage Hysteresis	-	12.7	V_{HYS}	-	0.32	-	V
Input Current	V_I= V_{DDI}(1) or 0 V	-	I_I	-	-	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12.9	t_{PHL} , t_{PLH}	-	11.6	19.1	ns
Pulse Width Distortion	$\|t_{PHL} – t_{PLH}\|$	12.9	PWD	-	0.8	2.8	ns
Propagation Delay Skew(2) (Between any two units)	-	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.9	t_{skCD}	-	-	3.3	ns
	Opposing Direction	12.9	t_{skOD}	-	-	3.7	
Output Rise Time	10 % - 90 %	12.9	t_r	-	0.8	-	ns
Output Fall Time	90 % - 10 %	12.9	t_f	-	0.8	-	ns
Enable 3-state output enable time(3)	50 kHz, Duty=50 %, tr=tf=2 ns,C_L=15 pF	12.12	t_{pZL} , t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time		12.12	t_{pLZ} , t_{pHZ}	-	-	18.0	ns
Common mode transient immunity	V_I= V_{DDI} or 0 V , VCM=1500 V , T_a=25 °C	12.15	| CMTI |	100	-	-	kV/μs

Note(1): V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}
Note(2): Propagation delay difference (between parts) is applied under the same operating conditions.
(Power supply voltage. input current, temperature conditions, etc.).
Note(3):When EN_X signal is changed from Low to High or OPEN, the output signal (V_{Ox}) is valid after the output enable time.
The output signal (V_{Ox}) within the output enable time is undefined.

9.3. Electrical Characteristics – 2.5 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V≤V_{DD1}≤2.75 V, 2.25 V≤V_{DD2}≤2.75 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	Fig.	SYMBOL	MIN	TYP.	MAX	UNIT
DC SPECIFICATIONS							
Under voltage Lockout	Threshold when supply voltage is rising	12.1 12.3	V_{DDXUV+}	-	2.10	2.25	V
	Threshold when supply voltage is falling		V_{DDXUV-}	1.7	1.9	-	
	Supply voltage hysteresis		V_{DDXUVH}	0.1	0.2	-	
Output Voltage Logic High	V_{Ix} = H , I_{OH} = -20 μA	12.5	V_{OH}	V_{DDO}(1)-0.1	V_{DDO}(1)	-	V
	V_{Ix} = H , I_{OH} = -4 mA			V_{DDO}(1)-0.4	V_{DDO}(1)-0.2	-	
Output Voltage Logic Low	V_{Ix} = L , I_{OL} = 20 μA	12.5	V_{OL}	-	0.0	0.1	V
	V_{Ix} = L , I_{OL} = 4 mA			-	0.2	0.4	
Output impedance	-	12.5	Z_O	-	50	-	Ω
High-level input voltage	-	12.7	V_{IH}	0.7*V_{DDI}(1)	-	-	V
Low-level input voltage	-	12.7	V_{IL}	-	-	0.3*V_{DDI}(1)	V
Input Voltage Hysteresis	-	12.7	V_{HYS}	-	0.32	-	V
Input Current	V_I= V_{DDI}(1) or 0 V	-	I_I	-	-	±10	μA
SWITCHING SPECIFICATIONS							
Data Rate	-	-	t_{bps}	DC	-	150	Mbps
Pulse Width	-	-	PW	6.6	-	-	ns
Propagation Delay	50 kHz,Duty=50 %, t_r=t_f=2 ns,C_L=15 pF	12.9	t_{PHL} , t_{PLH}	-	12.6	21.0	ns
Pulse Width Distortion	|t_{PHL} – t_{PLH}|	12.9	PWD	-	1.0	3.0	ns
Propagation Delay Skew(2) (Between any two units)	-	-	t_{PSK}	-	-	10	ns
Channel Matching	Same Direction	12.9	t_{skCD}	-	-	3.5	ns
	Opposing Direction	12.9	t_{skOD}	-	-	3.9	
Output Rise Time	10 % - 90 %	12.9	t_r	-	0.8	-	ns
Output Fall Time	90 % - 10 %	12.9	t_f	-	0.8	-	ns
Enable 3-state output enable time(3)	50 kHz, Duty=50 %, tr=tf=2 ns,C_L=15 pF	12.12	t_{pZL} , t_{pZH}	-	-	15.0	ns
Enable 3-state output disable time		12.12	t_{pLZ} , t_{pHZ}	-	-	18.0	ns
Common mode transient Immunity	V_I= V_{DDI} or 0 V , VCM=1500 V , T_a=25 °C	12.15	| CMTI |	100	-	-	kV/μs

Note(1): V_{DDI}=Input-side V_{DDx} , V_{DDO}=Output-side V_{DDx}
Note(2): Propagation delay difference (between parts) is applied under the same operating conditions.
(Power supply voltage. input current, temperature conditions, etc.).
Note(3):When EN_X signal is changed from Low to High or OPEN, the output signal (V_{Ox}) is valid after the output enable time.
The output signal (V_{Ox}) within the output enable time is undefined.

9.4. Supply Current Characteristics – 5 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=5 V. Minimum/maximum specifications apply over the entire recommended operating range of 4.5 V≤V_{DD1}≤5.5 V, 4.5 V≤V_{DD2}≤5.5 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

(1) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL541L01) V_I=1 (DCL541H01)	$I_{DD1(Q)}$	-	3.0	4.3	mA
		$I_{DD2(Q)}$	-	4.5	6.6	mA
	V_I=0 (DCL541H01) V_I=1 (DCL541L01)	$I_{DD1(Q)}$	-	16.6	22.5	mA
		$I_{DD2(Q)}$	-	10.2	14.1	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	10.0	15.5	mA
		$I_{DD2(1)}$	-	7.6	10.2	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	12.1	18.2	mA
		$I_{DD2(25)}$	-	10.6	15.4	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	17.4	24.5	mA
		$I_{DD2(100)}$	-	22.5	35.2	mA

(2) DCL542x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL542L01) V_I=1 (DCL541H01)	$I_{DD1(Q)}$	-	3.8	5.5	mA
		$I_{DD2(Q)}$	-	3.8	5.5	mA
	V_I=0 (DCL542H01) V_I=1 (DCL542L01)	$I_{DD1(Q)}$	-	13.4	18.3	mA
		$I_{DD2(Q)}$	-	13.4	18.3	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	8.8	12.9	mA
		$I_{DD2(1)}$	-	8.8	12.9	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	11.4	16.8	mA
		$I_{DD2(25)}$	-	11.4	16.8	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	20.0	29.9	mA
		$I_{DD2(100)}$	-	20.0	29.9	mA

9.5. Supply Current Characteristics – 3.3 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V≤V_{DD1}≤3.6 V, 3.0 V≤V_{DD2}≤3.6 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

(1) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL541L01) V_I=1 (DCL541H01)	$I_{DD1(Q)}$	-	2.9	4.1	mA
		$I_{DD2(Q)}$	-	4.4	6.5	mA
	V_I=0 (DCL541H01) V_I=1 (DCL541L01)	$I_{DD1(Q)}$	-	16.5	22.3	mA
		$I_{DD2(Q)}$	-	10.1	14.0	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	9.9	14.9	mA
		$I_{DD2(1)}$	-	7.5	9.5	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	10.8	16.6	mA
		$I_{DD2(25)}$	-	9.7	12.8	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	14.5	19.9	mA
		$I_{DD2(100)}$	-	16.6	26.0	mA

(2) DCL542x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL542L01) V_I=1 (DCL542H01)	$I_{DD1(Q)}$	-	3.7	5.3	mA
		$I_{DD2(Q)}$	-	3.7	5.3	mA
	V_I=0 (DCL542H01) V_I=1 (DCL542L01)	$I_{DD1(Q)}$	-	13.3	18.2	mA
		$I_{DD2(Q)}$	-	13.3	18.2	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	8.7	12.2	mA
		$I_{DD2(1)}$	-	8.7	12.2	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	10.3	14.7	mA
		$I_{DD2(25)}$	-	10.3	14.7	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	15.6	23.0	mA
		$I_{DD2(100)}$	-	15.6	23.0	mA

9.6. Supply Current Characteristics – 2.5 V Supply

All typical specifications are at T_a=25 °C, V_{DD1}=V_{DD2}=2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V≤V_{DD1}≤2.75 V, 2.25 V≤V_{DD2}≤2.75 V, and -40 °C≤T_a≤110 °C, unless otherwise noted.

(1) DCL541x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL541L01) V_I=1 (DCL541H01)	$I_{DD1(Q)}$	-	2.9	4.1	mA
		$I_{DD2(Q)}$	-	4.5	6.4	mA
	V_I=0 (DCL541H01) V_I=1 (DCL541L01)	$I_{DD1(Q)}$	-	16.4	22.2	mA
		$I_{DD2(Q)}$	-	10.0	13.9	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	9.8	14.8	mA
		$I_{DD2(1)}$	-	7.4	9.5	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	10.4	16.1	mA
		$I_{DD2(25)}$	-	9.2	12.2	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	13.1	18.2	mA
		$I_{DD2(100)}$	-	14.3	24.1	mA

(2) DCL542x01

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Current (DC Signal)	V_I=0 (DCL542L01) V_I=1 (DCL541H01)	$I_{DD1(Q)}$	-	3.7	5.3	mA
		$I_{DD2(Q)}$	-	3.7	5.3	mA
	V_I=0 (DCL542H01) V_I=1 (DCL542L01)	$I_{DD1(Q)}$	-	13.2	18.1	mA
		$I_{DD2(Q)}$	-	13.2	18.1	mA
1 Mbps	f_{CLK}=500 kHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(1)}$	-	8.6	12.2	mA
		$I_{DD2(1)}$	-	8.6	12.2	mA
25 Mbps	f_{CLK}=12.5 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(25)}$	-	9.8	14.2	mA
		$I_{DD2(25)}$	-	9.8	14.2	mA
100 Mbps	f_{CLK}=50 MHz, duty=50 % cycle square wave. C_L=15 pF	$I_{DD1(100)}$	-	13.7	21.2	mA
		$I_{DD2(100)}$	-	13.7	21.2	mA

10. Insulation Specifications

PARAMETER	Symbol	TEST CONDITIONS	VALUE	UNIT
Minimum External Clrearance	CLR	Shortest terminal-to-terminal distance through air	8	mm
Minimum External Creepage	CPG	Shortest terminal-to-terminal distance across the package surface	8	mm
Distance Through The Insulation	DTI	Minimum internal gap	17	μm
Comparative Tracking Index	CTI		600	V
Material Group	-	According to IEC 60664-1	I	-
Overvoltage Category Per IEC 60664-1	-	Related Mains Voltage ≤ 300 V_{rms}	I-IV	-
	-	Related Mains Voltage ≤ 600 V_{rms}	I-IV	-
	-	Related Mains Voltage ≤ 1000 V_{rms}	I-III	-
DIN EN IEC 60747-17; (VDE 0884-17)				
Maximum Repititive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	1414	V_{PK}
Maximum Transient Isolation Voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification) , V_{TEST}= 1.2 x V_{IOTM}, t = 1 s (100 % production)	8000	V_{PK}
Maximum Impulse Voltage	V_{IMP}	IEC 61000-4-5 1.2/50 μs waveform	8000	V_{PK}
Maximum surge isolation voltage	V_{IOSM}	Test method per IEC 61000-4-5, 1.2/50 μs waveform, V_{IOSM} ≥ 1.3 × V_{IMP} (qualification)	12800	V_{PK}
Apparent charge measuring voltage	$V_{pd(m)}$	Method A, After Input/Output safety test subgroup2&3, $V_{ini,a}$=V_{IOTM}, $V_{pd(m)}$=1.2 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	1697	V_{PK}
		Method A, After environmental tests subgroup 1, $V_{ini,a}$=V_{IOTM}, $V_{pd(m)}$=1.6 x V_{IORM} t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	2263	
		Method B1; At routine test (100 % production) and preconditioning (type test) $V_{ini,b}$ ≥ 1.2 x V_{IOTM}, $V_{pd(m)}$=1.875 x V_{IORM} $t_{ini,b}$ = 1 s, t_m = 1 s partial discharge < 5 pC	2652	
Barrier capacitance, input to output	C_{IO}	f = 1 MHz	1.5	pF
Input Capacitance	C_I	V_{IX}	1.8	pF
Isolation Resistance	R_{IO}	V_{IO} = 500 V, T_A = 25 °C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 °C ≤ T_A ≤ 110 °C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150 °C	$>10^{9}$	
Pollution Degree	-	-	2	-
Climaic Category	-	-	40/110/21	-
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	V_{TEST} = V_{ISO} , t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} , t = 1 s (100 % production)	5000	V_{rms}

11. Safety Limiting Values

PARAMETER	Symbol	TEST CONDITIONS	Value	Unit
Safety Input, Output Or Supply Current	I_S	V_{DD1}=V_{DD2}=5.5 V, Tj=150 °C,T_a=25 °C	284	mA
		V_{DD1}=V_{DD2}=3.6 V, Tj=150 °C,T_a=25 °C	434	mA
		V_{DD1}=V_{DD2}=2.75 V, Tj=150 °C,T_a=25 °C	568	mA
Safety Input, Output Or Total Power	P_S	Tj=150 °C, T_a=25 °C	1562	mW
Maximum Safety Temperature	T_S	-	150	°C

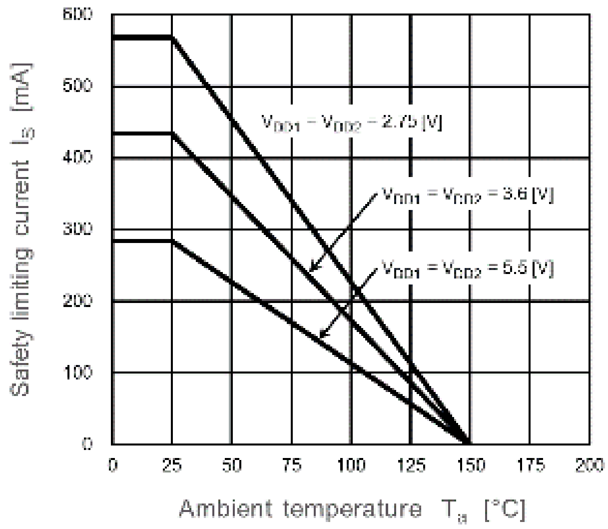
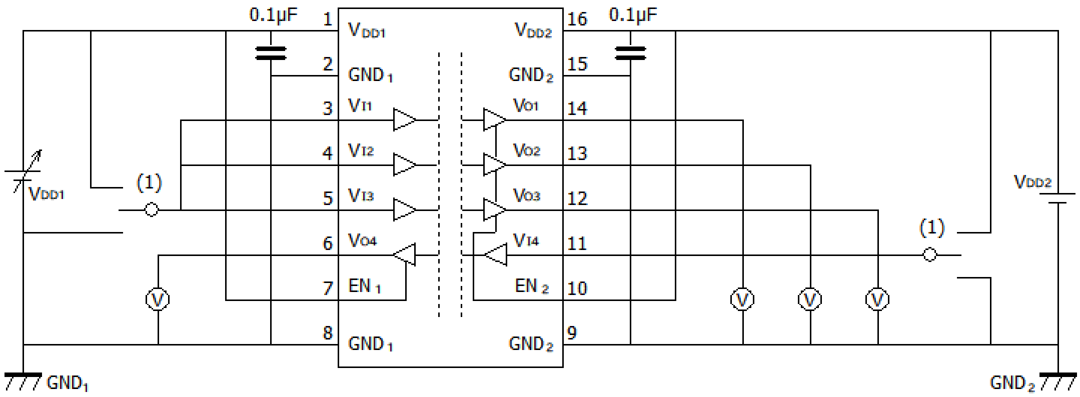


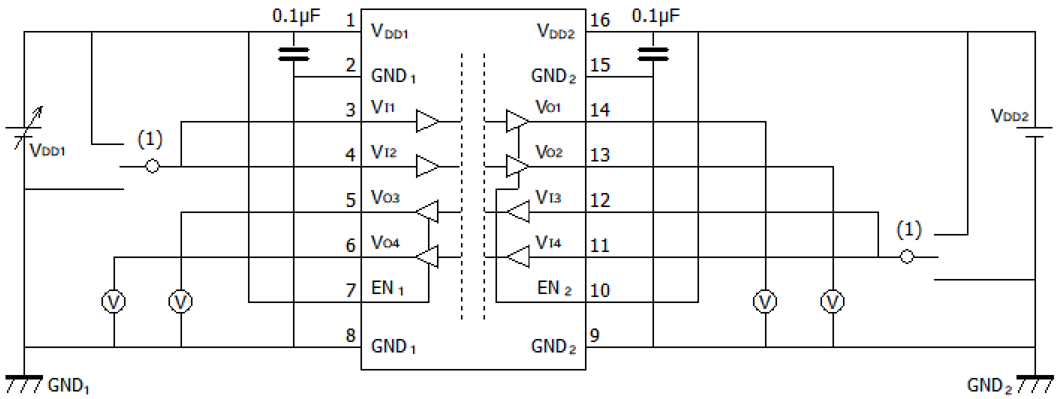
Fig. 11.1: Thermal Derating Curve for Safety Limiting Current - T_a

12. Test Circuit



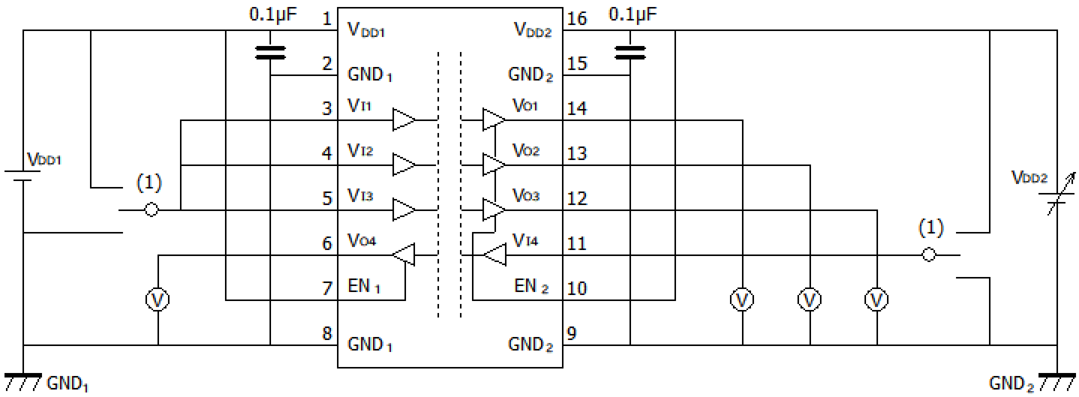
1: Default=L : V_{DDx} , Default=H : GND_x

Fig. 12.1: DCL541L01/DCL541H01 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



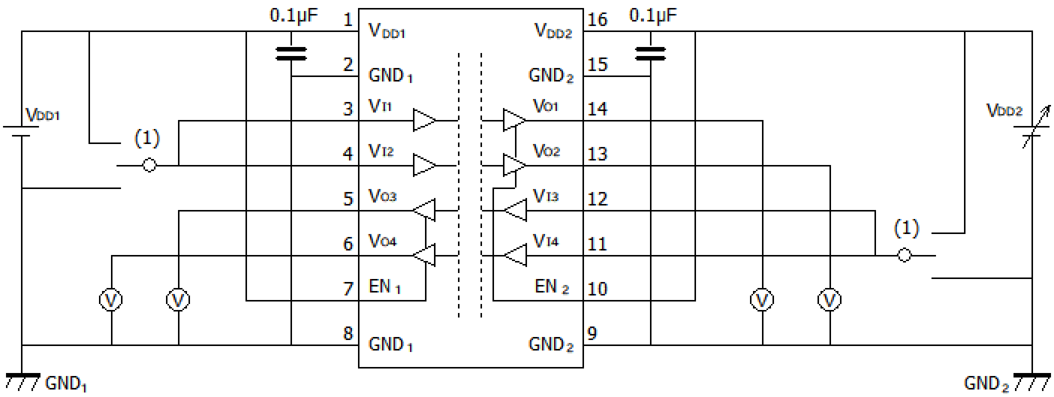
1: Default=L : V_{DDx} , Default=H : GND_x

Fig. 12.2: DCL542L01/DCL542H01 V_{DD1UV+}/ V_{DD1UV-} Test Circuit



1: Default=L : V_{DDx} , Default=H : GND_x

Fig. 12.3: DCL541L01/DCL541H01 V_{DD2UV+}/ V_{DD2UV-}Test Circuit



1: Default=L : V_{DDx} , Default=H : GND_x

Fig. 12.4: DCL542L01/DCL542H01 V_{DD2UV+}/ V_{DD2UV-}Test Circuit

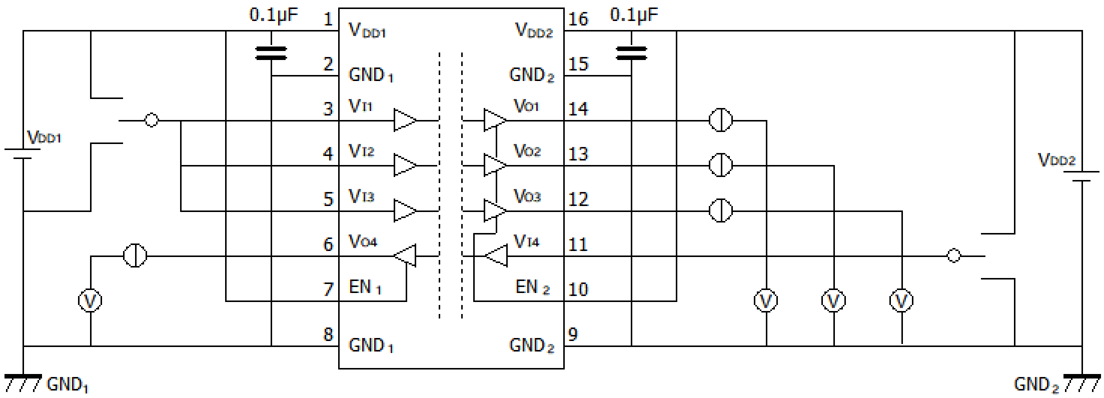


Fig. 12.5: DCL541L01/DCL541H01 V_{OH}/V_{OL} Test Circuit

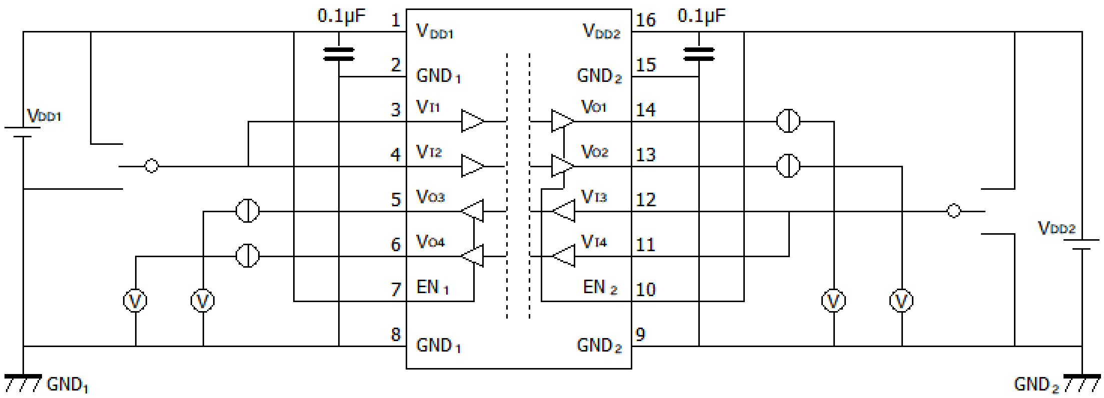


Fig. 12.6: DCL542L01/DCL542H01 V_{OH}/V_{OL} Test Circuit

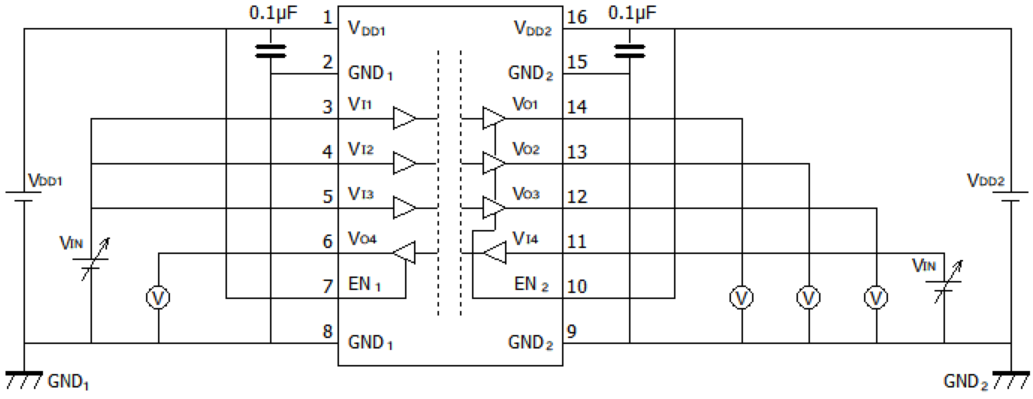


Fig. 12.7: DCL541L01/DCL541H01 V_{IH}/V_{IL} Test Circuit

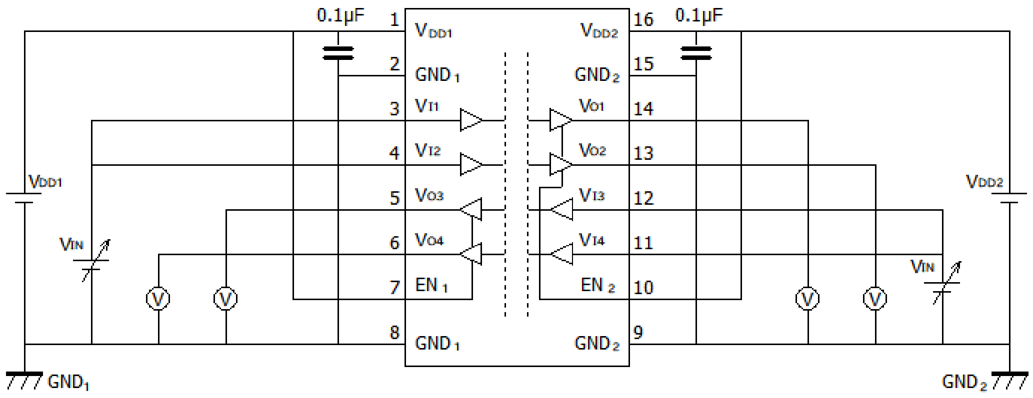
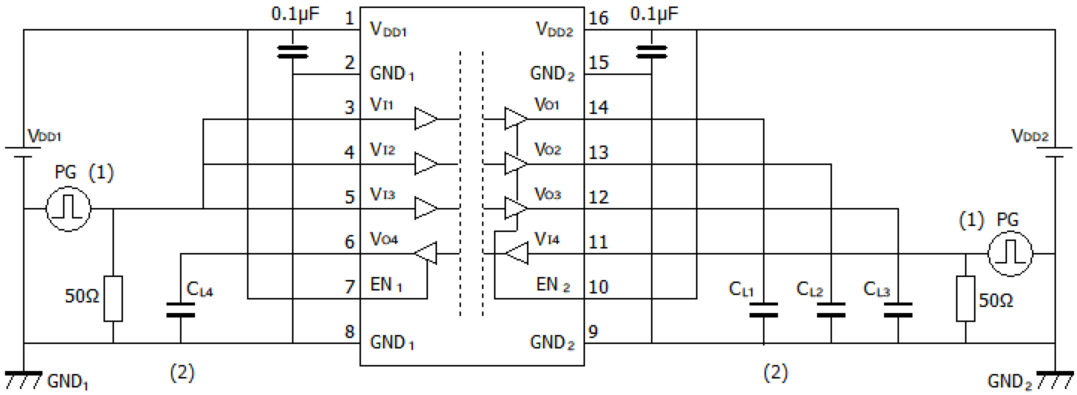


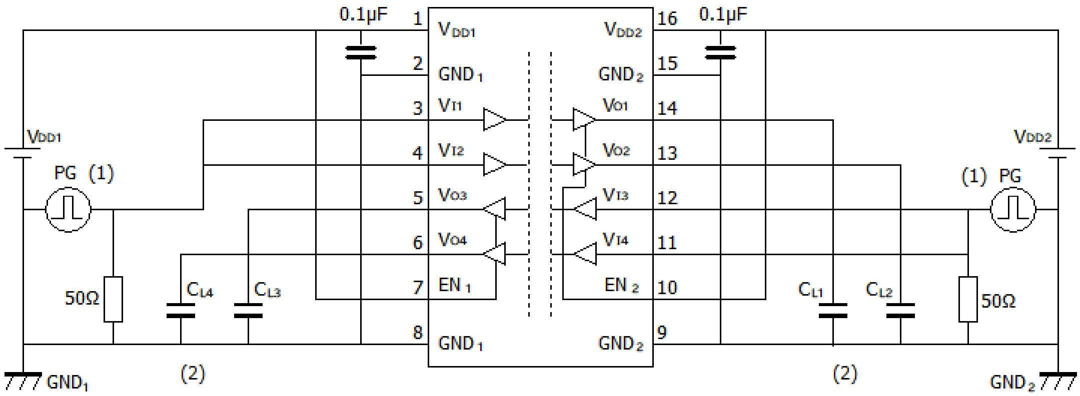
Fig. 12.8: DCL542L01/DCL542H01 V_{IH}/V_{IL} Test Circuit



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

2: C_{LX}=15 pF includes instrumentation and fixture capacitance.

Fig. 12.9: DCL541L01/DCL541H01 Switching Test Circuit



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.

2: C_{LX}=15 pF includes instrumentation and fixture capacitance.

Fig. 12.10: DCL542L01/DCL542H01 Switching Test Circuit

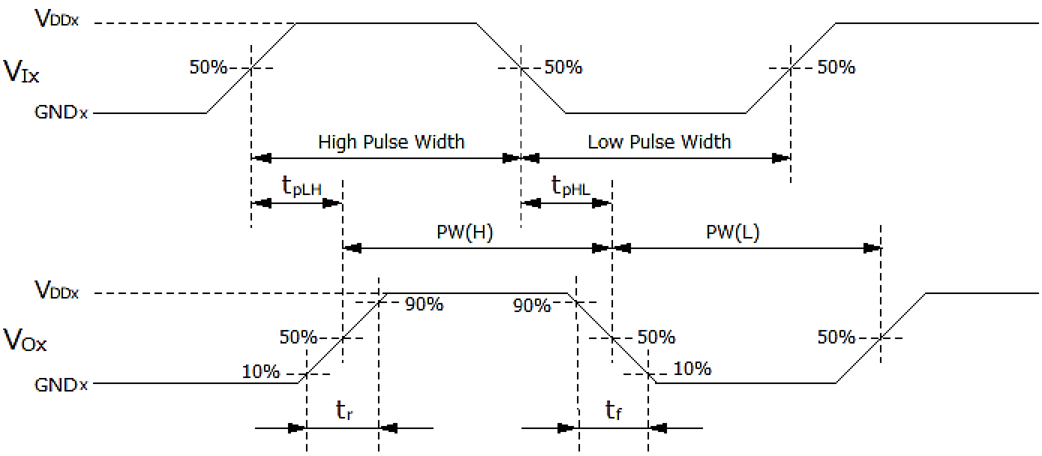
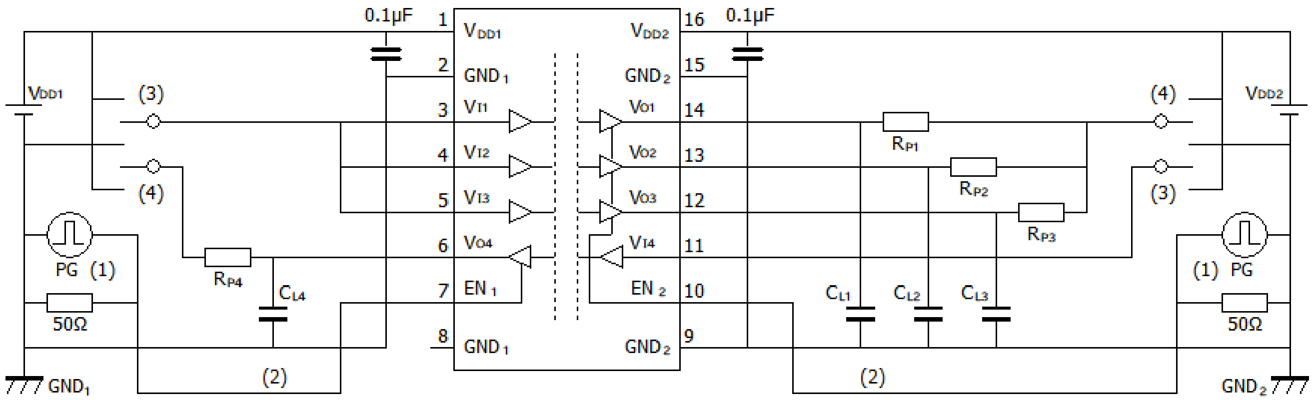
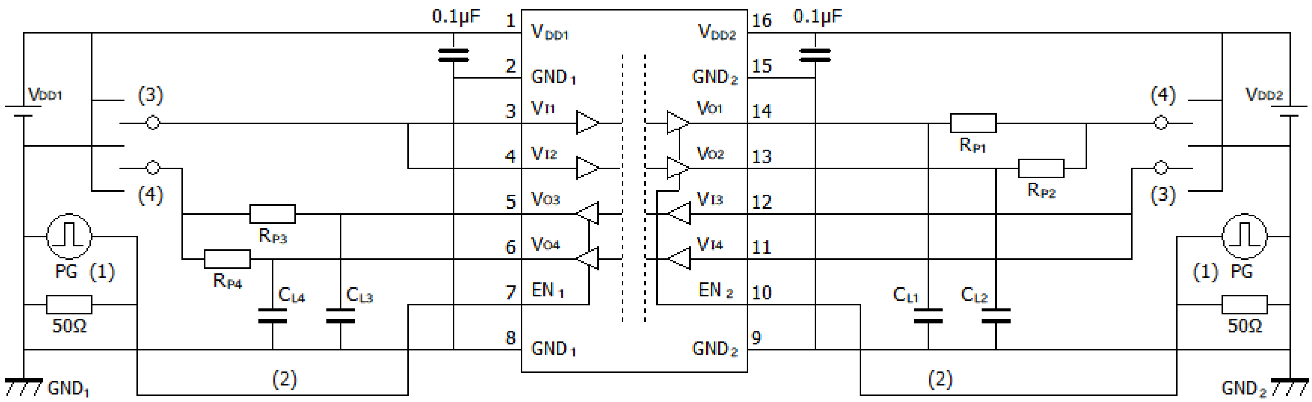


Fig. 12.11: DCL54xL01/DCL54xH01 Switching Waveforms



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.
2: C_{LX}=15 pF includes instrumentation and fixture capacitance.
3: GND for t_{pZL}, t_{pLZ}, V_{DD} for t_{pZH}, t_{pHZ}
4: V_{DD} for t_{pZL}, t_{pLZ}, GND for t_{pZH}, t_{pHZ}.

Fig. 12.12: DCL541L01/DCL541H01 Enable Propagation Delay Time Test Circuit



1: The input pulse is supplied by a generator having the following characteristics: PRR≤50 kHz, 50 % duty cycle, tr≤2 ns, tf≤2 ns, Z_O =50 Ω. At the input, 50 Ω resistor is required to terminate input generator signal. It is needed not in actual application.
2: C_{LX}=15 pF includes instrumentation and fixture capacitance.
3: GND for t_{pZL}, t_{pLZ}, V_{DD} for t_{pZH}, t_{pHZ}
4: V_{DD} for t_{pZL}, t_{pLZ}, GND for t_{pZH}, t_{pHZ}.

Fig. 12.13: DCL542L01/DCL542H01 Enable Propagation Delay Time Test Circuit

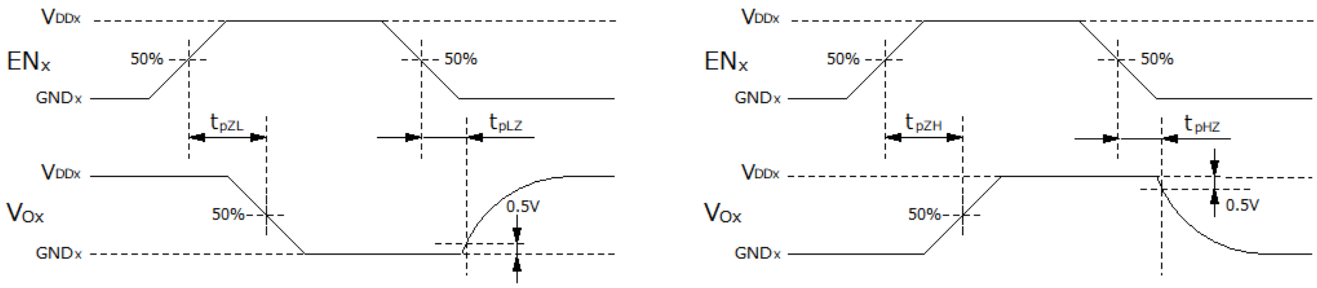
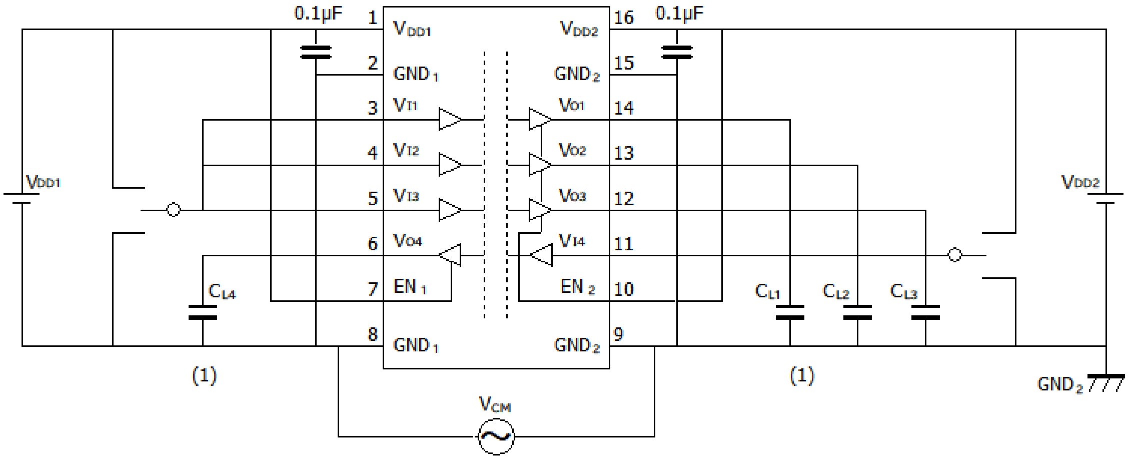


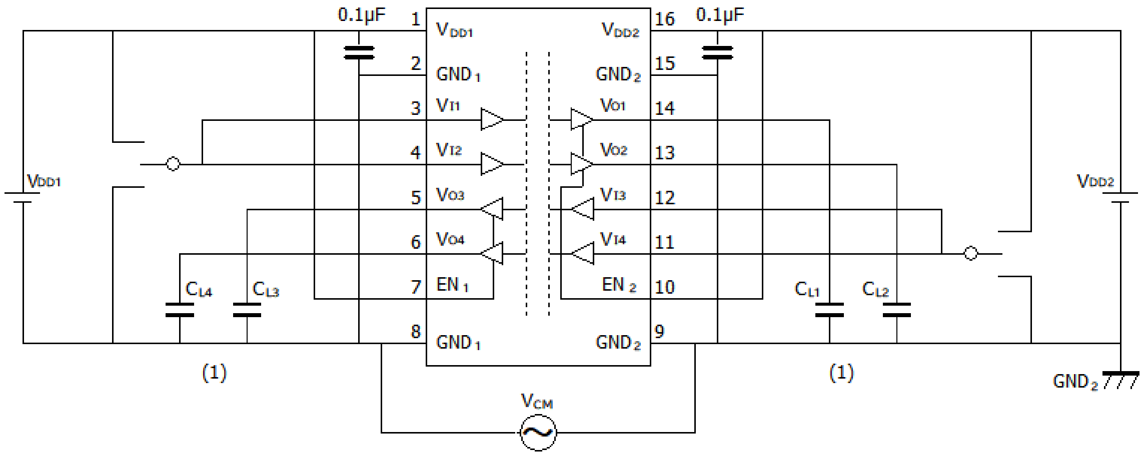
Fig. 12.14: DCL54xL01/DCL54xH01 Enable Propagation Delay Time Waveforms



1: C_{LX}=15 pF includes instrumentation and fixture capacitance.

2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND_1 or with reference to GND_2.

Fig. 12.15: DCL541L01/DCL541H01 Common-Mode Transient Immunity Test Circuit



1: C_{LX}=15 pF includes instrumentation and fixture capacitance.

2: Apply V_{CM} with reference to the GND terminal on the output terminal side of the IC. The GND on the IC input terminal side is isolated from the output terminal side. Depending on which channel is being measured, V_{CM} may be applied with reference to GND_1 or with reference to GND_2.

Fig. 12.16: DCL542L01/DCL542H01 Common-Mode Transient Immunity Test Circuit

13. Characteristics Curves (Note)

Note: The following characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

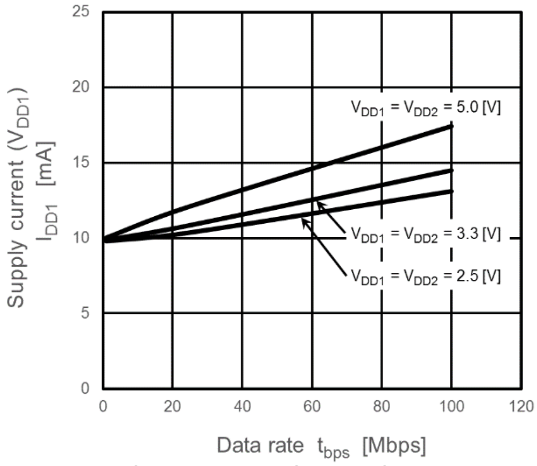


Fig. 13.1: DCL541x01 I_{DD1} Supply Current - Data rate

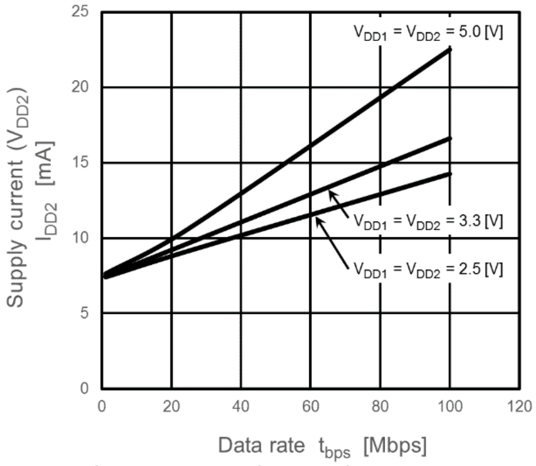


Fig. 13.2: DCL541x01 I_{DD2} Supply Current - Data rate

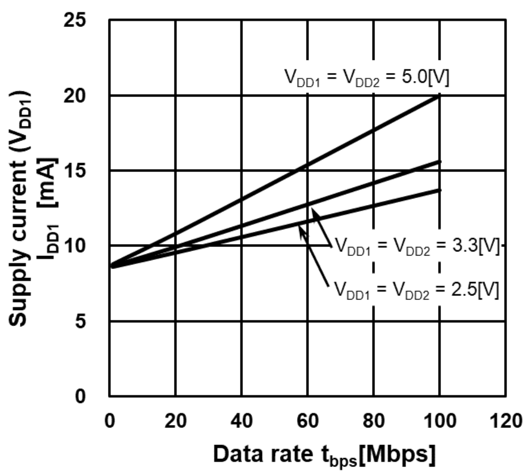


Fig. 13.3: DCL542x01 I_{DD1} Supply Current - Data rate

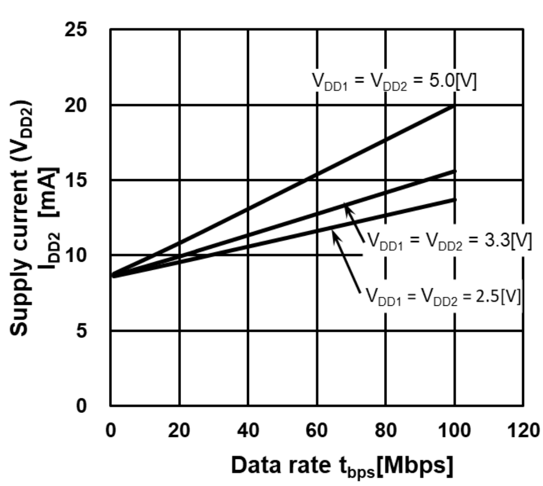


Fig. 13.4: DCL542x01 I_{DD2} Supply Current - Data rate

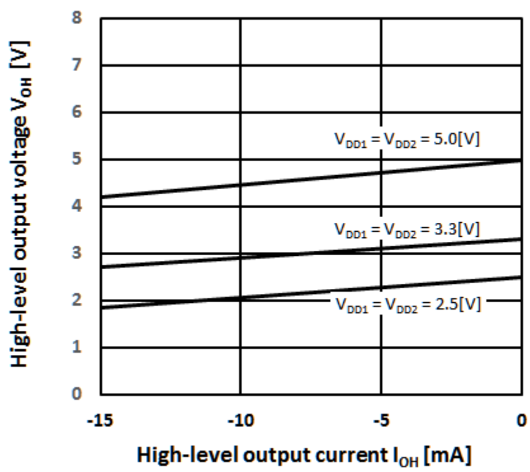


Fig. 13.5: V_{OH}-I_{OH}

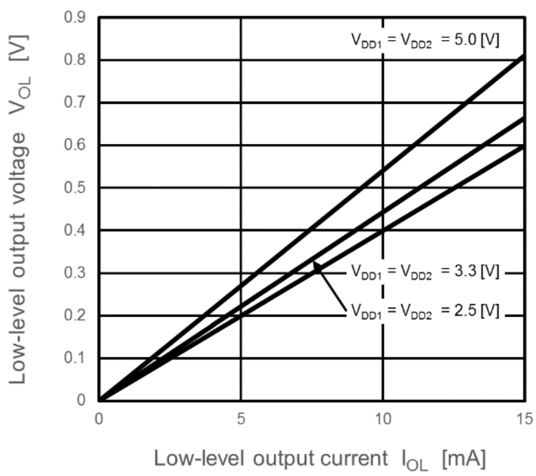


Fig. 13.6: V_{OL}-I_{OL}

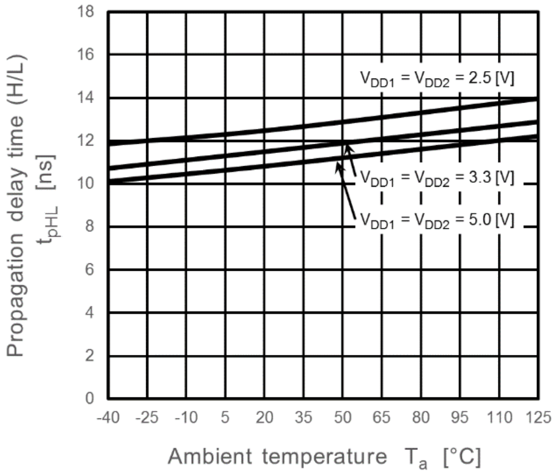


Fig. 13.7:Propagation Delay Time t_{PHL} -T_a

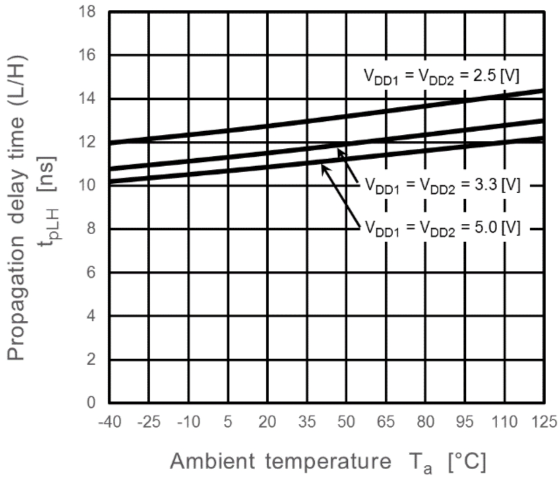


Fig. 13.8: Propagation Delay Time t_{PLH} -T_a

14. Application Note

14.1. Eye diagram

The following figure shows typical eye diagrams of DCL541x01 at the maximum data rate of 150Mbps with pseudorandom bit sequences (PRBS), supply voltage 3.3V for reference only.

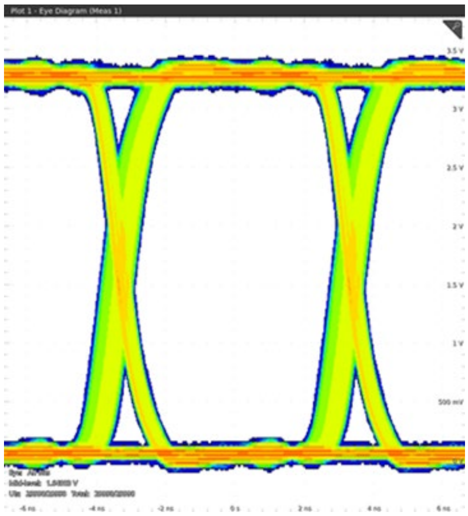


Fig. 14.1:DCL541L01 Eye diagram at 150Mbps

14.2. PCB layout

A ceramic capacitor (0.1 µF) should be connected between pin 1 (V_{DD1}) and pin 2 (GND_1) for V_{DD1} and between pin 16 (V_{DD2}) and pin 15 (GND_2) for V_{DD2}, and it should be the layout on the IC as close as possible (less than 10mm). Otherwise, the IC may not operate properly.

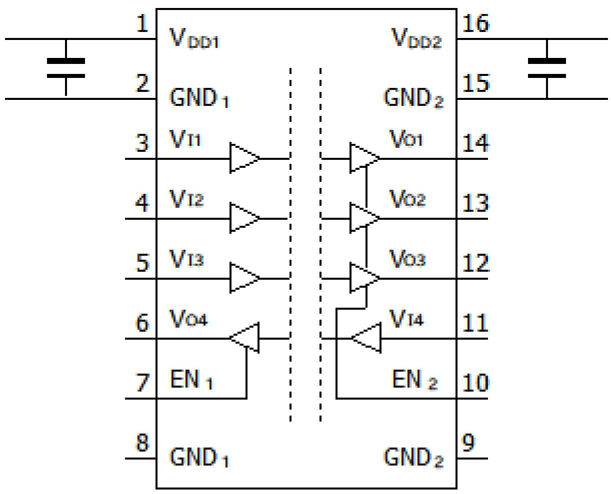
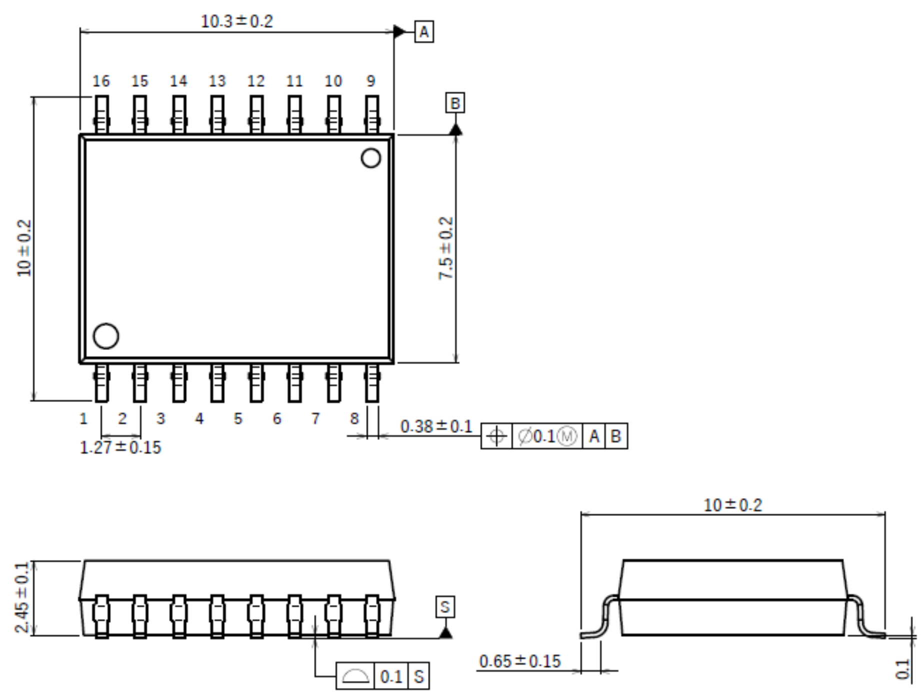
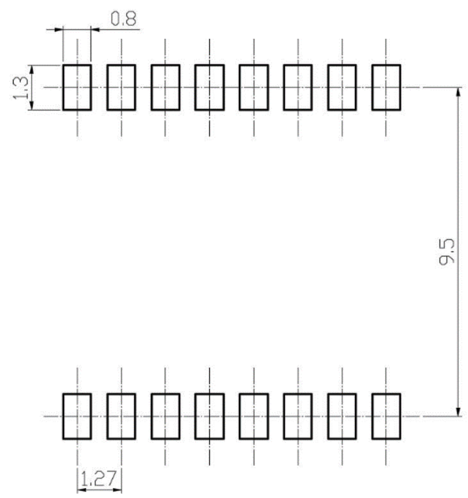


Fig. 14.2:Recommended Printed Circuit Board Layout

15. Package Information

Implementation category	Surface Mount
Pin Number	16
Weight (g)	0.426 (Typ.)
Package Dimension Width × Length × Height (mm)	10.3 × 10.0 × 2.45 (Typ.)
Package Dimension(mm) / Land Pattern Example (mm)	Package Dimension  Land Pattern Dimensions (for reference only) 

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