Features of third generation SiC MOSFET

1. Introduction

Power semiconductors, which serve to supply and control electric power, are indispensable for energy conservation and the realization of carbon neutral in all types of electrical equipment. The demand for power semiconductors is expected to continue to grow in the future as automobiles become electrically powered and industrial equipment become more efficient and smaller. In the context of the expanding demand mentioned above, Silicon Carbide(SiC) is attracting attention as a next generation power-semiconductor material that can withstand higher voltages and lower losses than conventional Silicon(Si).

Continuing from our second generation(2G), our third generation(3G) SiC MOSFET adopts a structure in which a Schottky barrier diode (SBD) is built in parallel with the PN diode that exists between the drain and source of the SiC MOSFET to solve the reliability problem of the device. In addition, by adopting the latest device structure, we have significantly improved the switching performance index R_{on}*Q_{gd} and the on-resistance per unit area $R_{on}A$, compared with our 2G products. The wide gate-to-source voltage (V_{GS}) rating and the high gate threshold voltage (V_{th}) make it less susceptible to the malfunction due to switching noise, which means it is an easy-to-use product with high capability to noise.

3G SiC MOSFET has the above-mentioned features, contributing to lower-power-dissipation and higher-output in the applications such as switching-mode power supplies, uninterruptible power supplies (UPS), solar inverters, and EV charging stations.

2. Product list

As shown in Table2.1, the 3G SiC MOSFET includes a lineup of TO-247 packaged products with 650V, 1200V withstand voltage.

Product	Package	V_{DSS}(V)	$R_{DS(ON)}$ typ. (mΩ)	I_D(A)	V_{th} (V)	Q_g typ. (nc)
TW015N120C	TO-247	1200	15	100	3.0 to 5.0	158
TW030N120C			30	60		82
TW045N120C			45	40		57
TW060N120C			60	36		46
TW140N120C			140	20		24
TW015N65C		650	15	100		128
TW027N65C			27	58		65
TW048N65C			48	40		41
TW083N65C			83	30		28
TW107N65C			107	20		21
TW015Z120C	TO-247-4L	1200	15	100	3.0 to 5.0	158
TW030Z120C			30	60		82
TW045Z120C			45	40		57
TW060Z120C			60	36		46
TW140Z120C			140	20		24
TW015Z65C		650	15	100		128
TW027Z65C			27	58		65
TW048Z65C			48	40		41
TW083Z65C			83	30		28
TW107Z65C			107	20		21

Table2.1 3G SiC MOSFET products

3. Features of 3G SiC MOSFET

3.1 Improvement of conduction loss and switching loss

Fig. 3.1(b) shows the structure of the 3G SiC MOSFET. Compared to the 2G SiC MOSFET structure (Fig. 3.1(a)), nitrogen is injected under the wide p-type diffusion region (p-well) to reduce the p-well bottom spreading resistance R_{spread} and increase the current capability of the SBD. In addition, by injecting nitrogen into the JFET [Note 1] region, the area of the JFET is reduced, thereby reducing the feedback capacitance without increasing $R_{on}A$.

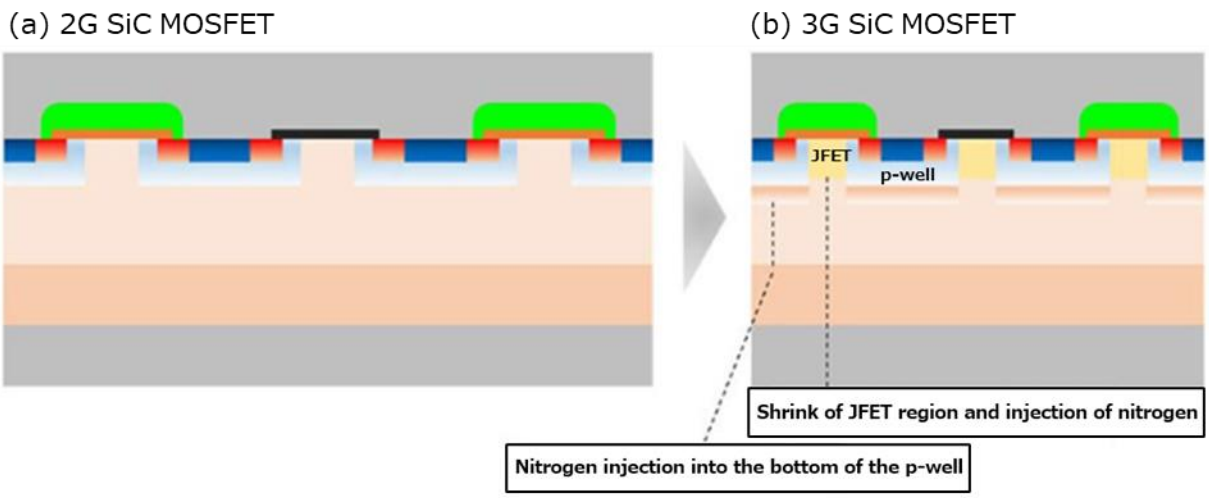


Fig. 3.1 Structure of 2G and 3G SiC MOSFET

Compared to the 2G product, as shown in Fig. 3.2, by applying this state-of-the-art device structure, the 3G SiC MOSFET of 1200V has a 43% reduction in on-resistance per unit area $R_{on}A$ and an 80% reduction in the switching performance index $R_{on}*Q_{gd}$. Fig. 3.3 shows the results of evaluating the switching loss of the 2G and 3G products. The switching loss of the 3G SiC MOSFET(1200V, 45mΩ (typ.)) is about 11% lower than that of the 2G SiC MOSFET(1200V, 70mΩ (typ.), even though the R_{on} is reduced by about 35%. Fig. 3.4 shows the inductance (L) load circuit for evaluating waveforms and losses during switching. Fig. 3.5 shows turn-on waveforms and turn-off waveforms.

Note1 JFET: An abbreviation for Junction Field Effect Transistor, which is a voltage-controlled transistor.

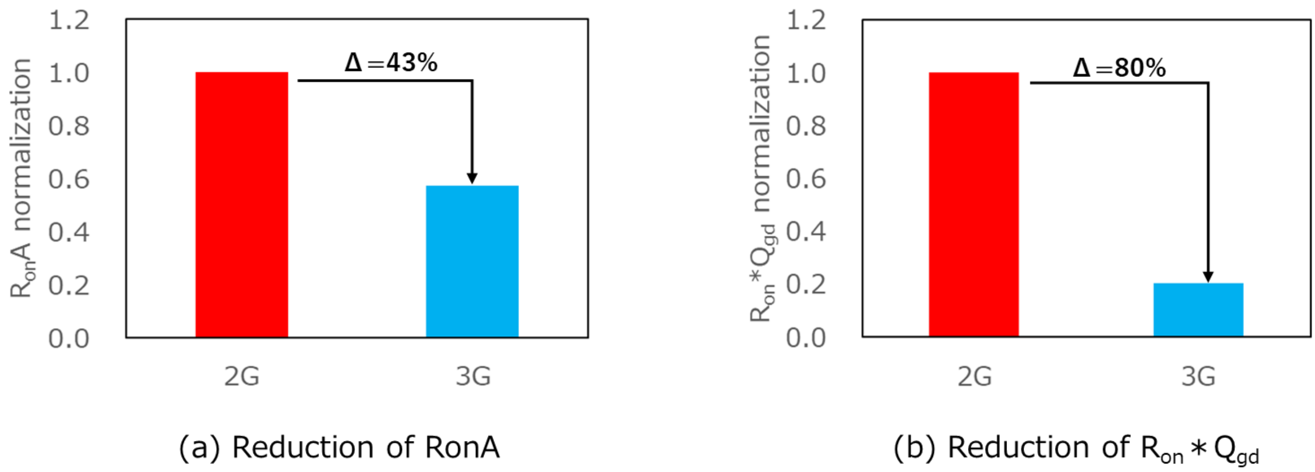


Fig. 3.2 Reduction results of 3G $R_{on}A$ and $R_{on}*Q_{gd}$ against 2G

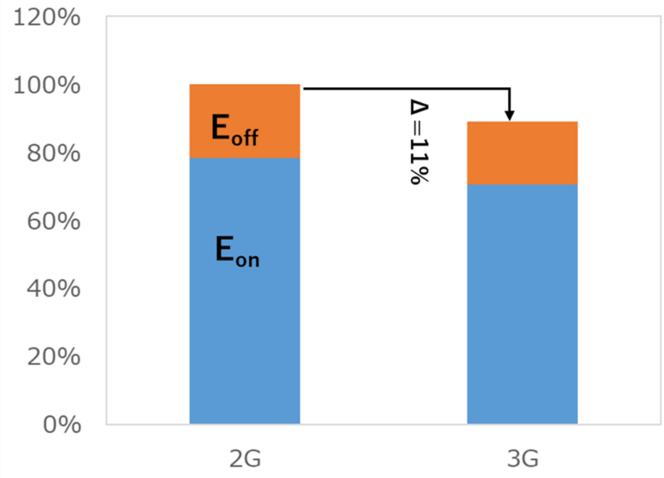


Fig. 3.3 Switching loss Comparison between 2G and 3G 1200V SiC MOSFET

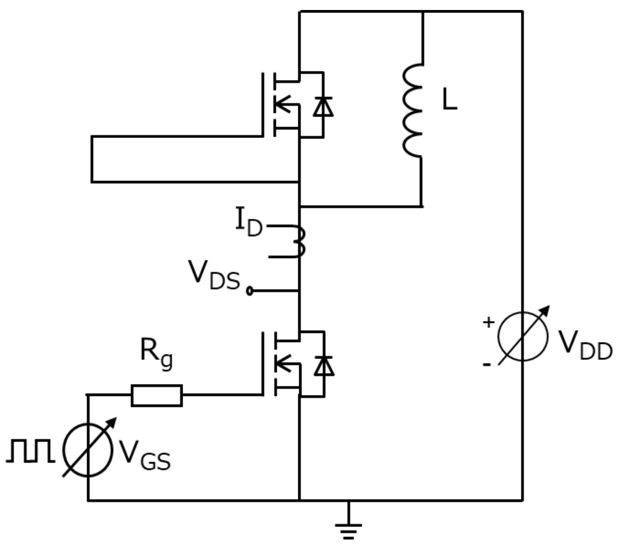


Fig. 3.4 L-load circuit for evaluating waveform and loss during switching

Measured conditions: V_{DD}=800V, I_D=20A, L=100μH, V_{GS}=18V/0V, R_g (external gate resistor) = 4.7Ω

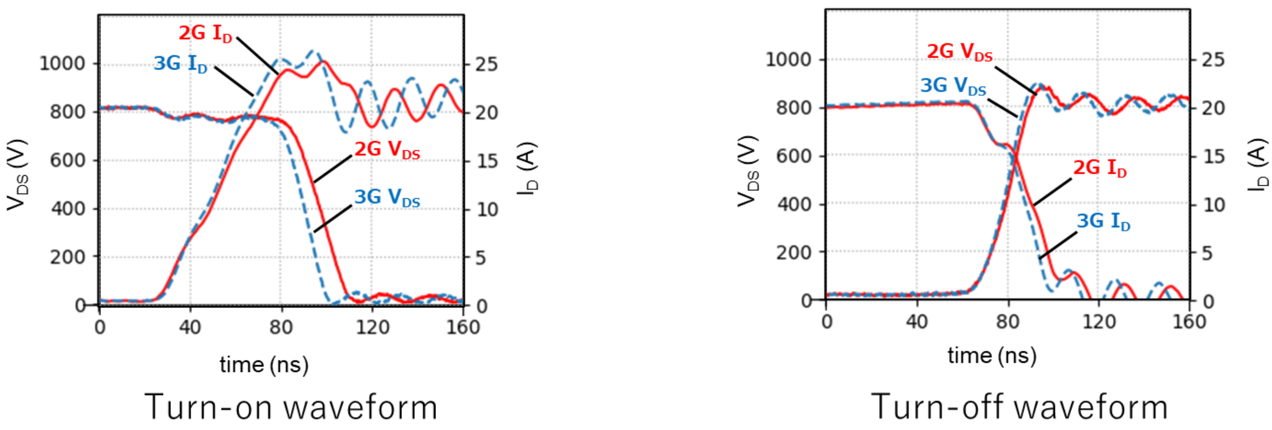


Fig. 3.5 Waveform comparison of L-load switching for 2G and 3G 1200V SiC MOSFET

3.2 Easier gate drive design by wider V_{GS} rating and higher V_{th}

As shown in Fig. 3.6, our 3G SiC MOSFET has a wider V_{GS} rating: (-10V(min) to 25V(max) and a higher V_{th}:3V(min) to 5V(max) over competitor's latest generation products, making it less susceptible to malfunction due to switching noise and easier to design gate drives.

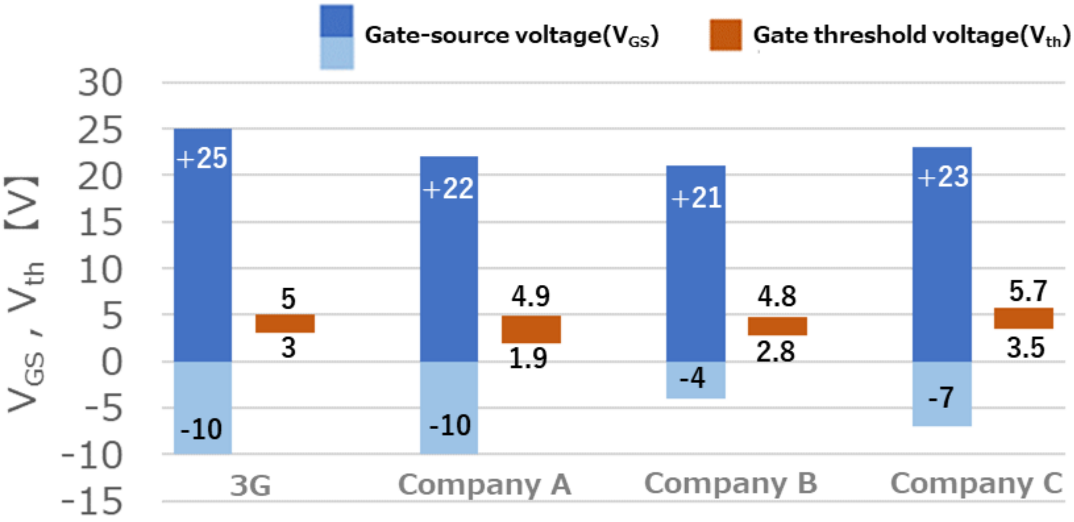


Fig. 3.6 V_{GS} ratings and V_{th} standards for our 3G product and the latest-generation products of other competitors

3.3 Built-in SBD achieves both low forward voltage(V_F) and high reliability

The 3G SiC MOSFET adopts a structure (Fig. 3.7) in which an SBD is built in parallel with the PN diode of the SiC MOSFET. This achieves low V_F characteristics and greatly suppresses R_{on} fluctuation due to defect expansion in the SiC crystal. Fig. 3.8 shows the on-resistance ($R_{DS(ON)}$) fluctuations of a conventional SBD non-integrated SiC MOSFET and our SBD built-in SiC MOSFET when current density of 250 A/cm2 is applied from source to drain for 1000 hours. In conventional SBD non-integrated SiC MOSFET, we have confirmed that the $R_{DS(ON)}$ fluctuates by up to 42% after 1000 hours of current conduction. On the other hand, we were able to suppress the $R_{DS(ON)}$ variation up to 3% with the SBD built-in SiC MOSFET that we have adopted. This is because the built-in SBD suppresses PN diode-operation up to a high current and prevents crystal-defect extension.

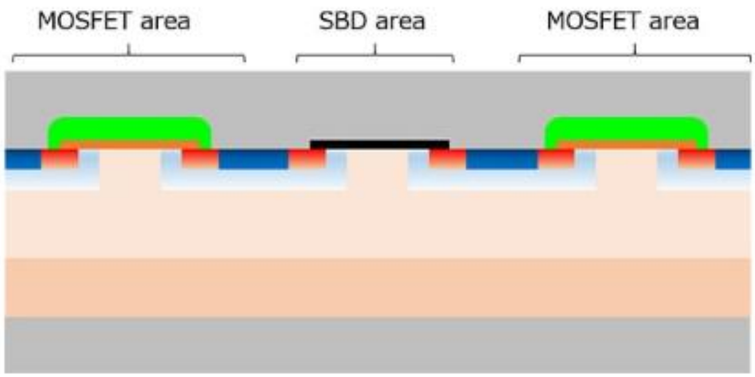


Fig. 3.7 Cross-sectional structure of a MOSFET with a built-in SBD

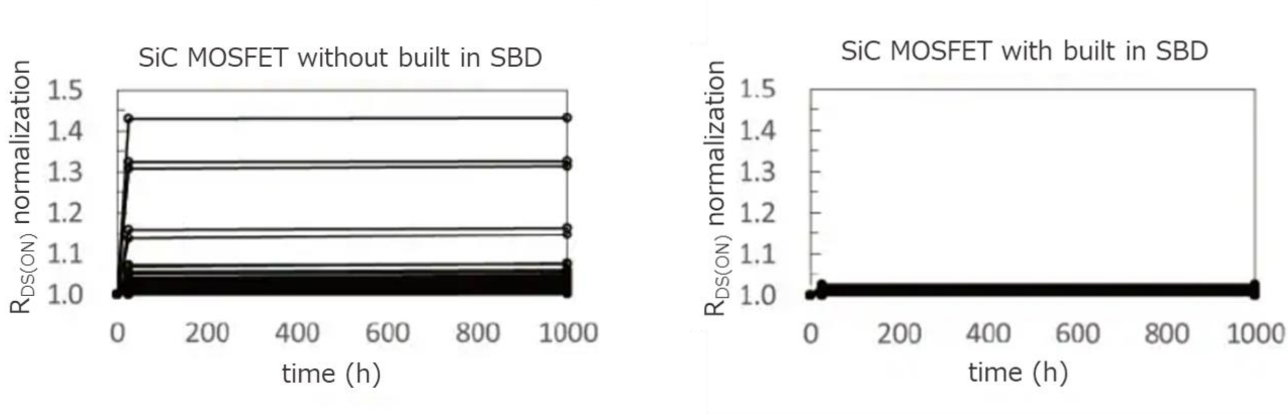


Fig. 3.8 $R_{DS(ON)}$ of 3G SiC MOSFET after drain reverse current flow

4. Superiority of 3G SiC MOSFET

4.1 Temperature characteristics of $R_{DS(ON)}$

The $R_{DS(ON)}$ temperature characteristics (Fig. 4.1) of our 3G product and competitor's latest generation products under the following measurement conditions are shown below. The higher the temperature, the higher $R_{DS(ON)}$ of each company's products. Taking the $R_{DS(ON)}$ at 25°C as 1, we confirmed that our 3G product has the lowest $R_{DS(ON)}$ increase rate at each temperature point. Even at Ta = 175°C, the $R_{DS(ON)}$ of our 3G product increased by only 17% compared to the $R_{DS(ON)}$ at 25°C, and the $R_{DS(ON)}$ of Company C which has the second lowest increase rate, increased by 43%. The temperature characteristics of $R_{DS(ON)}$ is found to be the advantage over all competitors.

Measured conditions: V_{GS}=18V, I_D=20A

Our measured sample: TW048N65C

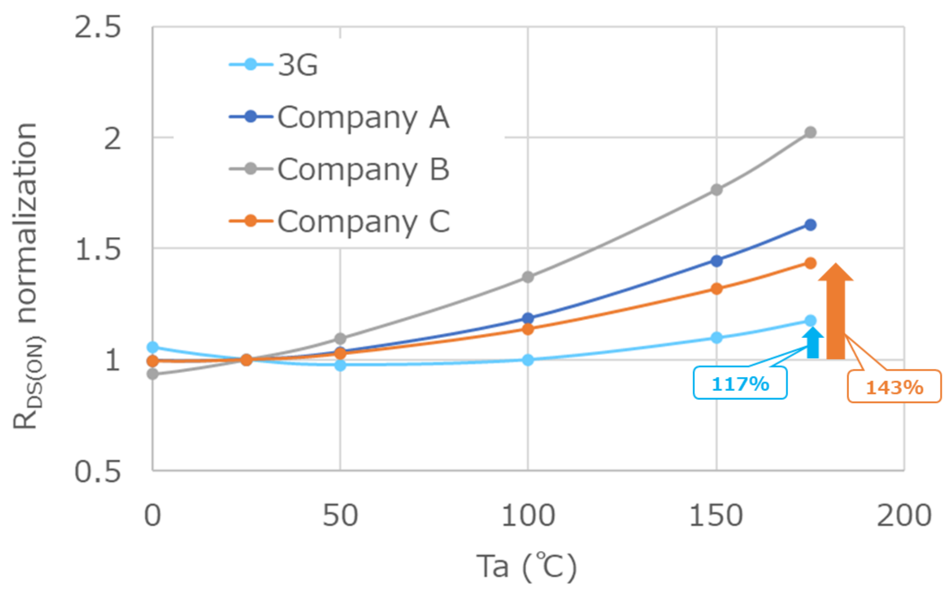


Fig. 4.1 Temperature dependence of $R_{DS(ON)}$

4.2 Switching characteristics

We conducted a comparative evaluation of turn-on switching loss (E_{on}) and turn-off switching loss (E_{off}) between our 3G product and the latest generation products of our competitors. Fig. 4.2 shows the R_g dependence curve of E_{on} loss and E_{off} loss. Since the 3G product has a built-in SBD, the output capacitance is slightly larger than the latest generation products of the competitors, and E_{on} is higher than the latest generation of competitors under the R_g conditions (4.7 Ω to 20 Ω) evaluated this time. On the other hand, we confirmed that our 3G product has faster current fall speed at turn-off, and the E_{off} is lower than the latest generation products of competitors in the entire R_g range. As shown in Fig. 4.3, we have confirmed that the total switching loss (E_{on}+E_{off}) of our 3G product is equal to or lower than that of competitor's latest generation products under the R_g conditions evaluated this time.

Measured conditions: V_{DD}=400V, I_D=20A, Ta=25°C, V_{GS}=20V/0V, L=100μH

The source-drain diode of each product is used as a freewheeling diode in parallel with the inductive load.

Our measured sample: TW048N65C

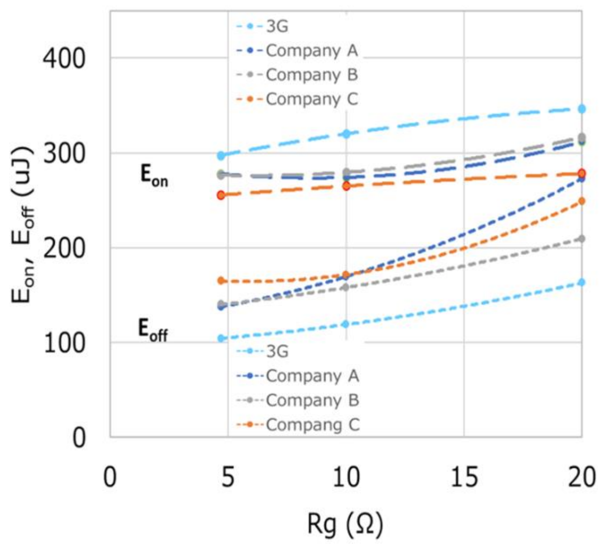


Fig. 4.2 R_g dependence of turn-on (E_{on}) and turn-off (E_{off}) switching Loss

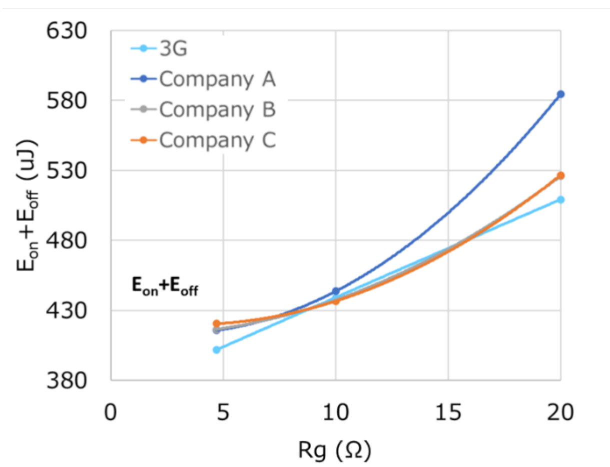


Fig. 4.3 R_g dependence of total switching loss (E_{on}+E_{off})

4.3 V_F of source to drain

Our 3G SiC MOSFET has a built-in SBD to achieve low reverse conduction loss due to low source to drain V_F. I_{DR}-V_F (V_{GS}=0V) curve in Fig. 4.4 shows that our 3G product has a lower V_F than the latest generation products of competitors in the entire I_{DR} region. When there is a reverse conduction period, for example, during the dead-time period in synchronous rectification mode, current flows between the source to drain, so the low V_F characteristics helps reduce the reverse conduction loss.

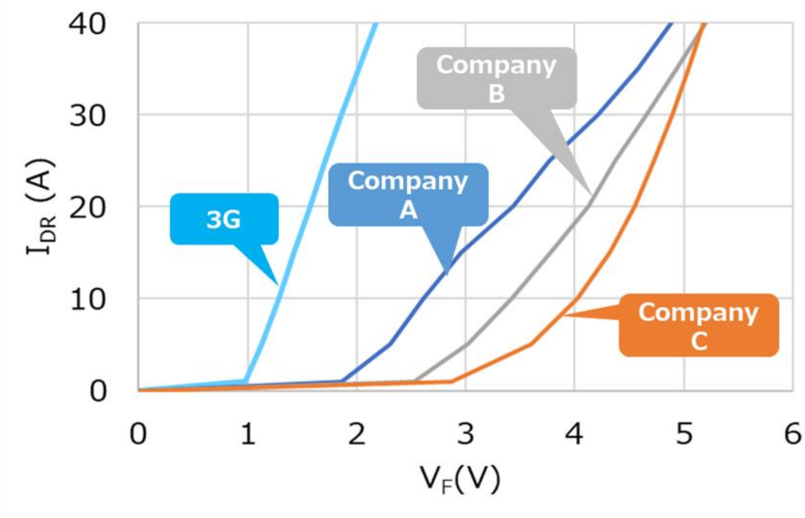
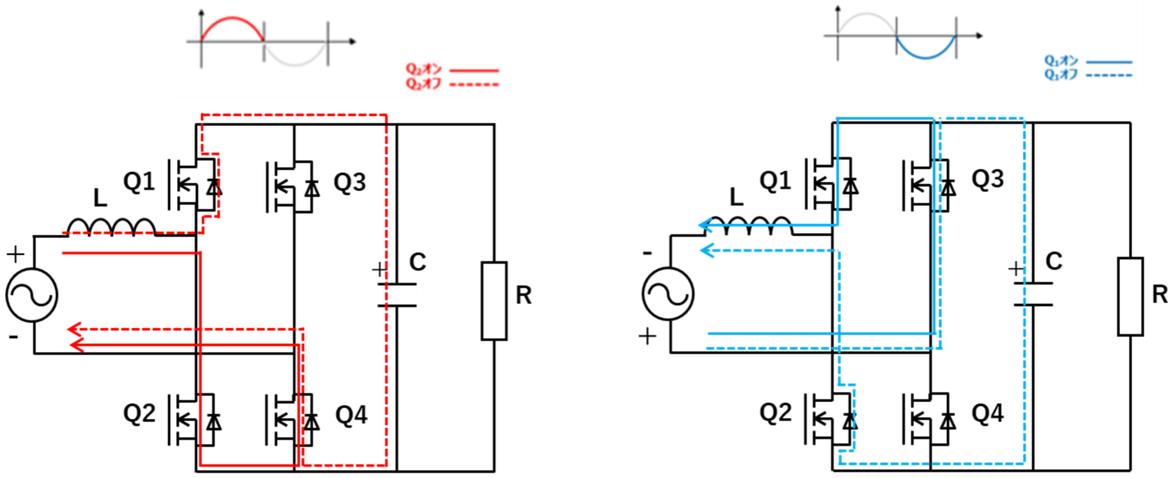


Fig. 4. 4 I_{DR}-V_F curve

4.4 Evaluation results with totem pole PFC evaluation board

Totem pole PFC is a power supply PFC circuit topology that can achieve both high efficiency and a small number of components and has been attracting attention in recent years due to the widespread use of SiC and GaN. Fig. 4.5 shows the totem-pole PFC and its operation. High-frequency leg (Q1,Q2) performs high-frequency (to hundreds of kHz or MHz) switching operations, and low-frequency leg (Q3,Q4) performs rectification operations at commercial frequency (50-60Hz). Because Q1 and Q2 perform hard-switching operation at high frequencies, a deadtime is provided to prevent Q1 and Q2 from turning on simultaneously. During this period, the body diode will be conducted, resulting in a loss due to reverse recovery current. Therefore, to reduce the loss of totem pole PFC, products with excellent reverse recovery characteristics such as SiC MOSFET and GaN should be used. In addition, Q3 and Q4 shown in Fig. 4.5 are alternately performed synchronous rectification every half cycle of the input AC power supply and the switching occurs at the zero-cross point. Therefore, a low $R_{DS(ON)}$ product can be selected without the need for the high-speed reverse recovery characteristics of a parasitic built-in diode.



(a) positive cycle (b) negative cycle

Fig. 4.5 PFC circuit of totem pole connection and explanation of the operation

This time, we installed our 3G SiC MOSFET (TW048N65C) in Q1 and Q2 for high frequency switching and compared the efficiency with that of our competitors. Table 4.1 shows the evaluation conditions for the totem pole PFC evaluation board.

input voltage	230VAC, 50Hz
output voltage	400V
output power	3600W(max)
switching frequency	72kHz

Table 4.1 PFC evaluation conditions

Fig. 4.6 shows the efficiency curve comparison between our 3G product (TW048N65C) and the latest generation products of competitors. We have confirmed that each company has achieved a high efficiency of 98% or more at 1.8 kW with a 50% load. Also, as shown in Fig. 4.7, under heavy load conditions of more than 1.8 kW(50% load) our 3G product is more efficient than the latest generation products of competitors, and the efficiency advantage is remarkable. This is believed to be the result obtained from the features of our 3G product, such as reduced conduction loss due to good temperature dependence of $R_{DS(ON)}$, reduced switching loss due to high-speed switching characteristics, and reduced dead time loss due to low V_F characteristics.

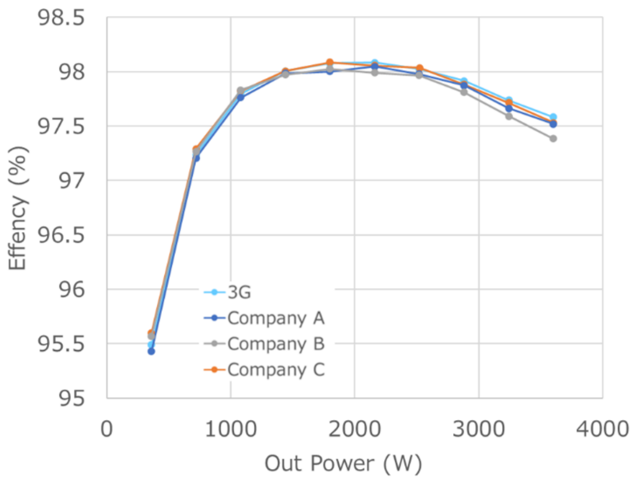


Fig. 4.6 Efficiency result of totem pole PFC evaluation board

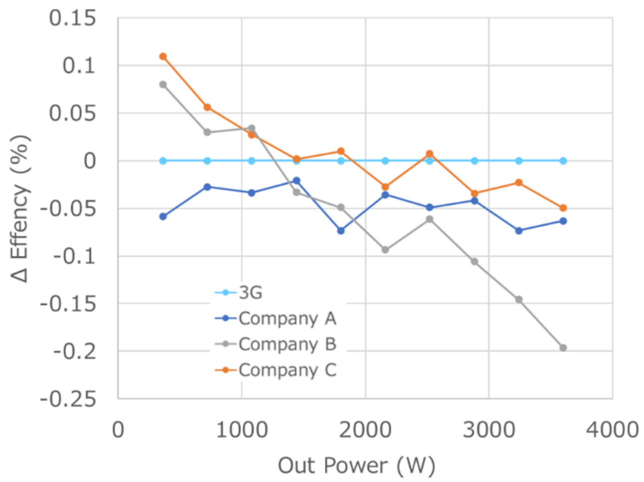


Fig. 4.7 Benchmark against other companies based on the efficiency of our 3G product

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